WCDMA Direct Conversion Front End in 0.13um digital CMOS

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***Abstract*—This project presents a direct-conversion 3G front end in 0.13um digital CMOS for use with the 2.1 GHz WCDMA frequency band. These receivers, widely used in 3G mobile telephony, require low power consumption and cost effective integration with other systems while maintaining high linearity and sensitivity. This project includes the design of a differential LNA, a double-balanced mixer and an on-chip quadrature VCO to realize a fully integrated front-end.**

I. Introduction

Direct Conversion (DC) architecture has recently become the topic of active research. Several reasons account for this renaissance: (1) DC lends itself to monolithic integration more easily than do heterodyne receivers and (2) DC suffers much less from mismatch-induced effects than do image-reject architectures.

The goal of this project is to describe the issues and tradeoffs in the design of an integrated direct-conversion receiver for a WCDMA standard operating in the 2110-2170 MHz range. A block diagram of the front-end presented is shown in Fig 1.

Section II discusses the design of the LNA. Section III discusses design of the mixer. Section IV describes a fully integrated Quadrature Voltage Controlled Oscillator (QVCO). Section V summarizes the entire receiver performance.

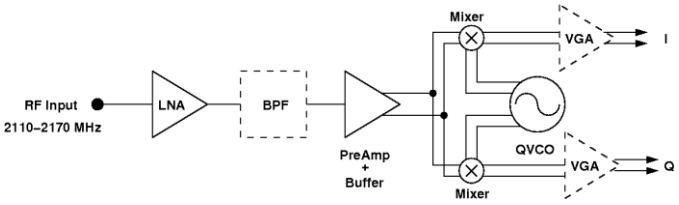

Figure 1 – System Block Diagram

II. Low Noise Amplifier and Preamplifier

The gain stages of the receiver consist of three cascaded amplifiers: (1) a single ended common source LNA with inductor degeneration, (2) a single ended to differential amplifier, and (3) a buffer stage consisting of a differential CMOS inverter with resistive feedback.

A single ended LNA was elected to reduce power and simplify the off chip filtering. The subsequent conversion from single ended to differential signaling is performed by a differential pair with one input AC grounded. A buffer is used between the differential conversion amplifier and the mixer to reduce distortion and to improve isolation from the QVCO.

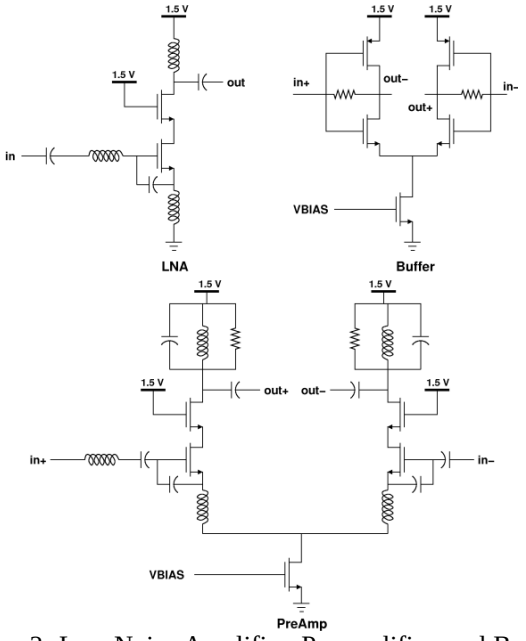

Figure 2- Low Noise Amplifier, Preamplifier, and Buffer

A. LNA Design

The common source LNA was designed using the model presented in [1]. Presented below are simplified versions of the models used:

$$Zin = j\left(\omega Lss - \frac{1}{\omega Cgs}\right) + gm\frac{Lss}{Cgs}$$

$$F = 1 + k\left(\frac{\omega_0}{\omega_T}\right)\frac{\gamma}{\alpha}\frac{1}{2Q} \quad Q = \frac{1}{2R_s\omega_0 C_{GS}} \quad k \equiv f(Q,\gamma,\alpha)$$

Using these models along with extracted data from the device models, the circuit parameters were iteratively solved using MATLAB. From these initial calculated values, the circuit components were systematically resized. By relating trends between the component sizes to trends in the magnitudes of the real and imaginary parts of the s-parameters, the s-parameters were manually adjusted towards the desired convergences.

B. Preamplifier and Buffer

The design of the single ended to differential amplifier was based on the design of the common source LNA. A true differential amplifier was first designed. An AC ground was then added to an input and one of the inductors was removed. Finally, the s-parameters were tuned.

Due to a delay path between the two inputs of the preamplifier through the degenerate inductors, however, the differential outputs of the preamp are not fully symmetrical. With this topology, a delayed version of the input signal shows up at the source of AC grounded input. This delayed signal distorts the output by driving the source of grounded input out of phase with the input signal.

Treating this delayed signal like a common gate perturbation on a fully symmetric circuit – and assuming resonance – the differential outputs can be approximated as follows:

$$out^- = -out^+ - gmR\left[1 + \omega^2 L_D C_{gs} - j\omega gm L_D\right]Vin$$

$$out^+ = \frac{gmR}{j\omega 2R_s C_{gs}}Vin$$

Because out+ is imaginary, whereas out- is both real and complex, the differential output cannot be balanced. The use of feedback in a differential configuration and proper component sizing reduces this distortion – however, feedback is not used directly in this stage in order to reduce the complexity of the input impedance matching. Feedback is achieved in the buffer.

Furthermore, the differential conversion stage was designed to drive the mixer impedance directly; however, coupling from the high amplitude oscillator signal onto the preamplifier corrupted the preamplifier output when directly connected to the mixer. The buffer provides the necessary isolation.

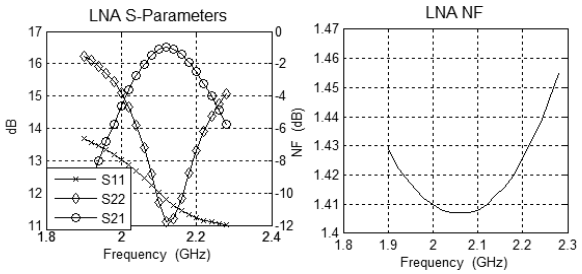

Figure 3 – LNA Simulation Plots

TABLE 1 – LOW NOISE AMPLIFIER PERFORMANCE TABLE

	Specification	Targeted	**Simulated**
LNA	NF	< 1.5 dB	**1.42 dB***
	Gain	> 15 dB	**16.5 dB**
	P1dB	> -15 dBm	**-9.33 dBm**
	IIP3	> -15 dBm	**-5.62 dBm**
	S11	< -10 dB	**-10 dB**
	S22	< -10 dB	**-12 dB**
	Current	< 5mA	**3.768mA**
PREAMP ***	NF	< 2 dB	**3.663 dB ***
	Gain	> 8 dB***	**11 dB*****
	P1dB	> -5 dBm	**-8.3 dBm**
	IIP3	> -15 dBm	**-0.9 dBm**
	S11	< -10 dB	**-8.6 dB**
	Current	< 8mA	**12.5mA**

* simulated values do not include correlated gate noise.
** simulated values include both Preamplifier and Buffer
*** measured differentially

III. MIXER

Mixers perform the crucial task of frequency conversion. The most popular architecture, the double-balanced Gilbert Cell, yields minimum LO-IF feed through and low even-order distortions while providing moderate gain.

The mixer presented in this project is a modified version of the double-balanced Gilbert Cell mixer. The mixer is illustrated in Figure 4. Transistors M1 and M2 convert the RF voltage to current and transistors M3-M6 multiply the RF signal with a square wave through commutating behavior.

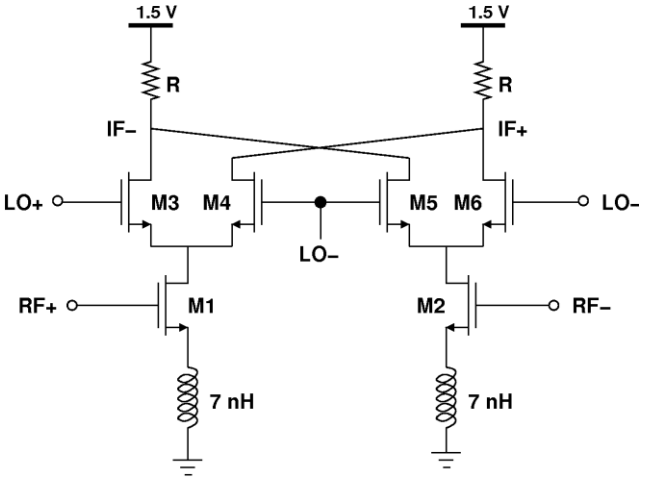

Figure 4 – Mixer Schematic.

In a CMOS process, it is possible to omit the tail current sources of traditional Gilbert Cell. The input now becomes a source-coupled pair instead of a differential pair. Although still balanced, this modified Gilbert Cell will only operate differentially when driven differentially at the RF inputs. The gain stage buffer helps to achieve this condition.

As shown in [3], balanced differential inputs and outputs will cancel the square law nonlinearity of the mixer when the tail sources are omitted. Therefore, the omission of the tail current source should improve the linearity of the mixer. Omitting the current source also improves the suitability of the mixer to low VDD digital processes; however, the common mode rejection now relies on the preceding gain stages.

A. Design Considerations and Methodology

The various tradeoffs encountered in the mixer design are highlighted in this section: conversion gain, linearity and noise. The mixer in this work was optimized for low noise and high linearity.

Down-conversion mixers must provide sufficient Conversion Gain (CG) to compensate for losses with minimal noise. However, too much gain will saturate later stages. The gain of the mixer is determined by the trans-conductance of the input

devices stages and the load impedance – the effect from the commutation switches is negligible. CG is defined as follows – where Gm,eff is the effective trans-conductance of M1/M2

$$CG = \frac{2G_{m,eff}R}{\pi}$$

Both the load resistance and transistors M1 M2 were initially sized to yield a gain near 15 dB – the extra gain was to provide an allowance for linearity trade-off. M1 M2 were sized to 100u/0.12u at 5 mA. The simulated CG and gm was 12dB and 40 mS respectively (without degeneration). The LO switches, M3-M6 were sized to provide fast switching with low ON resistance.

The linearity of the mixer depends on the linearity of the input pair trans-conductance [3]. Inductive source de-generation was used to improve the linearity at cost of high inductor area and a reduction in gain. Nevertheless, inductor degeneration preserves voltage headroom and minimizes the noise contribution. In addition, M1 M2 were biased in velocity saturation to linearize gm across the input voltage range.

Mixer noise is dominated by M1 M2 [3]. The output thermal noise contribution from M1 M2 is

$$v_n{}^2 = \frac{4kT\gamma}{gm_{1,2}}\left(\frac{2}{\pi}gm_{1,2}R\right)^2\left(1+\frac{1}{3^2}+\frac{1}{5^2}+\cdots\right)$$

Since noise is proportional to gm, reducing the gate overdrive and the bias current will reduce the effective Gm and reduce noise. Furthermore, a higher LO amplitude reduces the noise of the mixer.

TABLE 2 – MIXER PERFORMANCE TABLE

Specification	Targeted	**Simulated**
Conversion Gain	> 2 dB	**8 dB***
NF(dsb)**	< 15 dB	**10 dB**
P1dB	> -5 dBm	**-1.95 dBm**
IIP3	> 0 dBm	**2.54 dBm**
Current	< 10 mA	**10 mA**

* simulated with 5dBm oscillator amplitude
.** Dual Side Band, NF(ssb) = NF(dsb) + 3dB

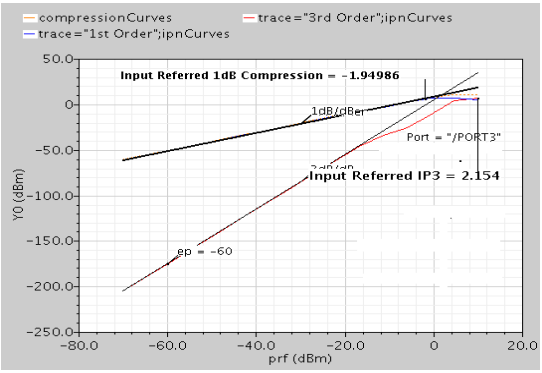

Figure 5 – Mixer P1dB and IIP3

IV. QUADRATURE VOLTAGE CONTROLLED OSCILLATOR

The QVCO presented in figure 6 is a tail current biased parallel LC QVCO. This topology provides rail-to-rail swing while allowing low VDD operation.

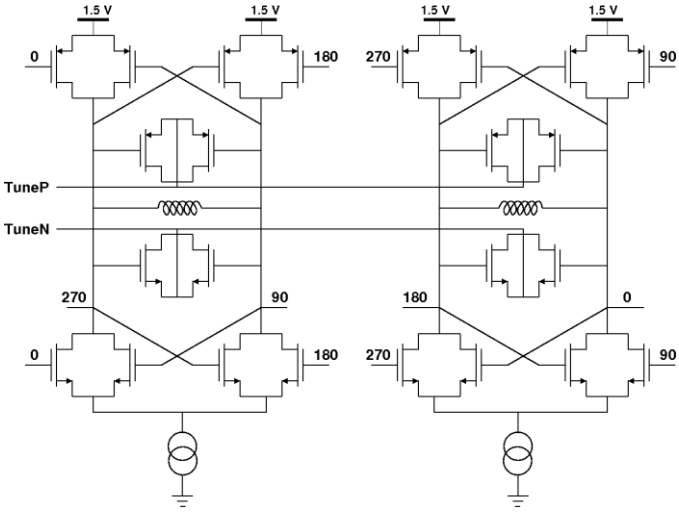

Figure 6 – QVCO Schematic

A. Design Procedure

Phase noise was the primary design concern .Using the linear phase noise model of a VCO provided by [5], phase noise can be minimized by increasing the signal swing and increasing LC tank quality. The model from [5] is as follows:

$$\mathcal{L} = 10\log[\frac{2FkT}{P_{sig}}(\frac{\omega_c}{2Q_{tank}\,\Delta\omega})^2]$$

Phase noise was reduced by designing for large swings and widening the inductor wires to improve the tank Q. To prevent excessive power consumption the bias of the QVCO was fixed using the methodology from [6]. Calculations recommended 7.5mA.

Furthermore, [6] reports how even-order noise harmonics can be up-converted into to phase noise. To reject this up-conversion, a pole was deliberately added between ω_0 and 2 ω_0 at the tail node with a properly sized capacitor.

To ensure stable oscillations, the parallel resistance of the LC tank was cancelled with a cross-coupled pair in positive feedback. According to the gm-id plots for this technology, a 50 um nfet biased at 10mA provided enough compensation without excessive over-sizing – excessive over-sizing of the cross-coupled transistors restricts the tunability of the VCO and introduces a dependence of the oscillation frequency on transistor sizing rather than the tank LC.

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Lastly, to ensure that the two LC oscillators remain injection locked, the aspect ratios of the injecting transistors were reduced relative to feedback path transistor sizes. [4] reports

how this approach to sizing improves phase noise. However, a large difference between the sizing of the injecting transistors and the feedback path transistors will cause phase mismatch between the two tanks. Calculations recommended a relative sizing of 2.5

TABLE 3 – OSCILLATOR PERFORMANCE TABLE

Specification	Targeted	**Simulated**	[7]	[8]
Frequency	2.11-2.17GHz	**2.10-2.28GHz**	1.1GHz	1.93GHz
Phase Noise*	< -113	**-124**	-120	-122
Power	< 30mW	**15mW**	5.4mW	27mW
FOM	-170	**-180.8**	-173.5	-171

* computed at 1MHz (dBc/Hz)

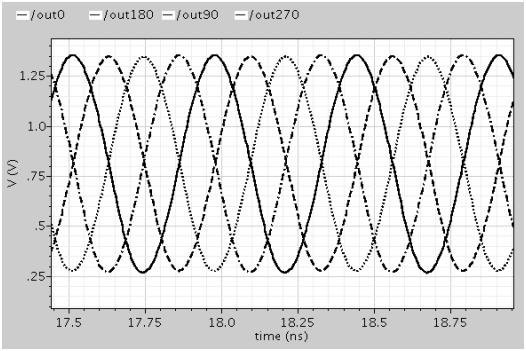

Figure 7 – QVCO Transient Output

V. SYSTEM PERFORMANCE

This section describes the performance. In this project, a fully integrate WCDMA including an LNA, mixer, and QVCO achiving a linearity of -0.98dBm IIP3 and gain of 44 was achieved.

TABLE 4 –SYSTEM PERFORMANCE TABLE

Specification	Targeted	**Simulated**	[9]	[10]	[11]
Process (um)	0.13	**0.13**	0.25	0.13	0.18
NF (dB)	< 6	**1.96***	8.92	--	--
NFdsb (dB)	--	**1.56**	--	6.5	5.6
Gain (dB)	> 25	**44 ****	16.92	34.8	4.7
P1dB (dBm)	> -25	**-4.39**	-21.1	-24	--
IIP3 (dBm)	> -25	**-0.98**	-15.04	-8.6	-10
Power (mW)		**58.2**	72.15	73	--
(w/VCO)	< 60	**73.2**	--	--	37.8
Phase Noise***	< -113	**-124**	--	--	-155

* computed using Friis equations -- provided for comparison purposes
** simulated with QVCO from transient analysis
*** computed at 1MHz (dBc/Hz)

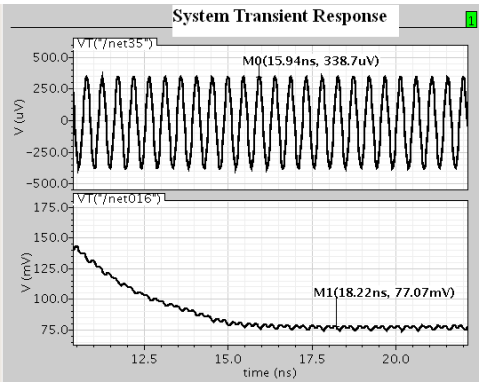

Figure 8 – System Transient Behavior (Single Mixer)

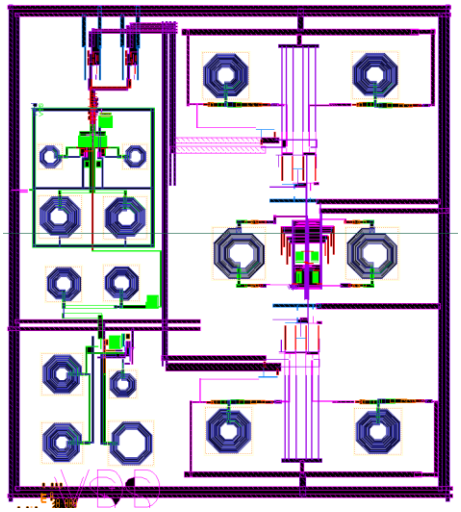

Figure 9 – Layout

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