An Energy Efficient 1 Gb/s, 6-to-10 GHz CMOS IR-UWB Transmitter and Receiver With Embedded On-Chip Antenna

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***Abstract*— We report a high data rate (upto 1 Gbps) Ultra-wideband (UWB) transceiver for very low power applications. The transmitter side, including pulse generator (PG), power amplifier (PA) and on-chip antenna, consumes only 7 pJ/b (3 pJ/b w/o PA). The novel UWB on-chip antenna has relatively low loss of 10 dBi and allows for a more compact overall system suitable for area constrained implantable and sensor node applications. The receive side includes an active band-select filter (ABSF) and an ultra wideband low-noise amplifier (LNA). The ABSF has more than 3.9 GHz bandwidth with less than 3 dB insertion loss. The low-voltage LNA consumes 2.56 mW and achieves a minimum noise figure of 3.35 dB with 10 dB power gain and an IIP3 better than -6.8 dBm. The total area of transmitter is 0.62 x 0.48 mm^2 and receive side covers an area of 1.9 x 0.94 mm^2. The system is implemented in IBM 0.13 µm standard CMOS process.**

***Index Terms*—UWB, miniaturized antenna, active band select filter, low-power, low-noise, power-amplifier**

I. Introduction

The growing interest in low-power transceivers for personal area networks (PAN), wireless sensor nodes (WSN) and implantable Microsystems (IMS) has motivated work on efficient communication systems. The major issues of concern are large area and high power consumptions in radio-front ends for moderate to high bandwidths. The low required power budget of these systems is either due to battery operation, or due to the fact that it needs a continuous means of external power delivery (example: the neural prosthesis and pacemaker). A careful study of these systems reveal that the major power consumption occurs at the data communication end, which usually requires several nano-Joules per transmitted bit in conventional (e.g., BPSK, QAM) implementations. Also, the compact area requirements preclude possibility of any overly complex system.

In recent years, ultra wideband communication (UWB) concept has opened new horizons for energy and area constrained systems by virtue of its low attainable energy levels down to tens of pico-Joules per transmitted bit [1]-[6]. An excellent feature of these UWB transmitters is nearly linear relationship between achievable data rates and resulting power consumption. This is extremely beneficial for battery operated and variable data-rate or adaptive systems. Although, the receive side for UWB systems does not possess the similar merits, it still can be designed with more relaxed requirements than narrow-band receivers, hence overall efficiency.

In this work, we propose an efficient impulse radio based ultra wideband (IR-UWB) transmitter and a receiver RF front-end. The transmitter (Tx) includes all-digital pulse generation, pulse shaping and modulation modules. A power amplifier with fully-integrated antenna is also designed for compactness. The receiver front-end includes an active band-select filter and a low noise amplifier. The system operates over the 6-10 GHz band of UWB spectrum.

The paper is organized as follows. Section II explains the full system architecture in brief followed by a detailed discussion of Tx design in section III. While, the design trade-offs for the receiver front-end is described in Section IV. The simulation results of the fully integrated system, both transmitter and receiver, are given in section V followed by the conclusion in section VI.

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II. Overall System Architecture

Fig. 1 shows the overall system architecture of the proposed implementation of UWB transceiver with on-chip antenna. The implemented blocks are highlighted in a color different from the rest. The various considerations and design trade-offs will be the topic of discussion for next two sections.

III. UWB Transmitter

A. Transmitter Architecture

The proposed ultra-wideband (UWB) transmitter can be operated in two distinct modes namely –with On-Chip Antenna (OnCA), or –with Off-chip Antenna (OfCA). In order to maintain same communication distance during OnCA mode a power-amplifier (PA) is required. The prime reason is the higher losses in the CMOS substrate, hence antenna, as compared to its Off-chip counterpart. On the other hand, the On-chip antenna compacts the transmitter architecture making it ideal choice for applications where space is conserved e.g., biomedical implants where the goal is to minimally intrude the normal body functions. A performance comparison between these two operating modes is also carried out to evaluate the feasibility of such architectures.

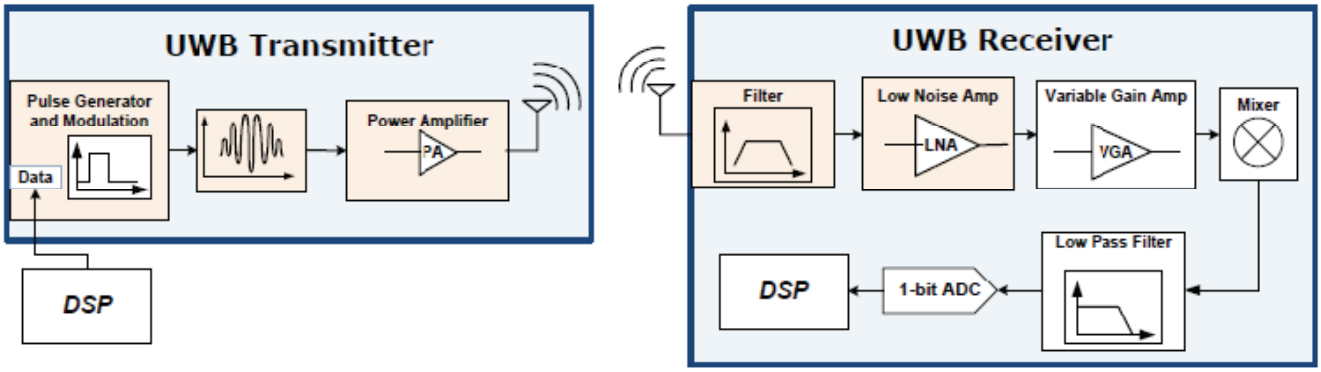


Fig. 1. Overall System Architecture

The design for IR type communication systems involves the selection of modulation type, pulse-design for desired spectral behavior and, most importantly, suitable operating frequency from the available 3.1-10.6 GHz band for IR-UWB applications. The following sections highlight the design choices made in this work to maximize performance.

B. Frequency Band and Modulation Type

The higher benefits of trading SNR with bandwidth, as discussed in Section-I doesn't come free. The added price is the closer to noise-level signals (<-41.3dB$_m$/MHz) which are harder to detect if not modified (modulated) properly. It also makes the detection at receive side a challenging task in the presence of strong interferers operating nearby frequency bands. Therefore the center frequency selection should be such as to minimize the impact of any known interferers. Another factor is the fact that relatively higher available fractional bandwidths (~0.8 f_c) at lower UWB spectrum (<5 GHz) results in less efficient front-ends.

In order to overcome these difficulties a relatively higher operating band (6-10 GHz) was selected. By avoiding the strong 5.5 GHz WLAN interference, it's possible to attain more communication range for same transmit power. The selection of bi-phase modulation scheme was due to its smoother spectral properties [4]. Also, the orthogonal signal nature helps in signal detection [5].

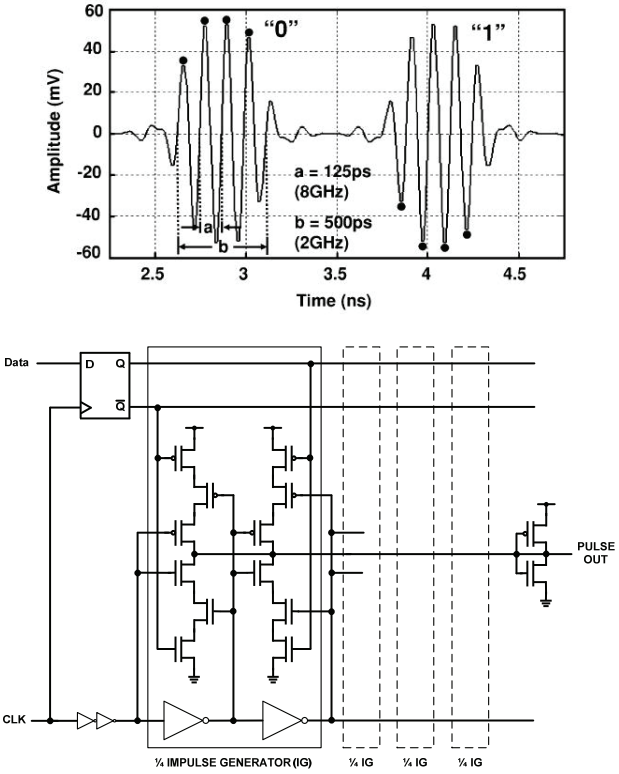


Fig.2. Pulse design and CMOS implementation [1]

C. Pulse Design and Digital Shaping

The selected pulse shape shown in Fig. 2 is similar to the one proposed in [1]. The duration of the pulse 0.5 ns results in 4 Ghz of bandwidth around the center frequency of 8 GHz. This is achieved by the 125 ps duration of one cycle in pulse which contains four of them. The individual cycles are weighted to follow a Gaussian like envelope which results in smoother spectral density.

The salient feature of this work is to achieve this spectral shaping without any bulky filters after the pulse generator. The all digital CMOS implementation is shown in Fig. 2. The bottom inverters, two per stage, ensure the duration of the single cycle to be around 125ps. At the same time the stacked PMOS and NMOS control the amplitude of the output pulse turn by turn. The D-latch controls the polarity of the output waveform resulting in an effective bi-Phase modulation. The last coupled PMOS-NMOS pair gives a fixed common mode to the output pulse to be fed either to the External Antenna or the PA preceding the embedded antenna.

D. On-Chip Antenna

To realize a complete RF system in CMOS, embedded on-chip antenna is integrated in the design. Monopole topology is chosen due to the tradeoffs between bandwidth, efficiency and required area. The tapered width increases the bandwidth in order to cover the whole band from 6 GHz to 10 GHz. The antenna is fully characterized using Ansoft HFSS^{TM}, as shown in Fig. 3, the antenna occupies an area of 1.2 mm^2, with a

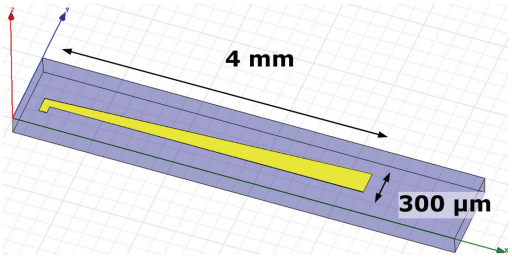


Fig. 3. Dimension of the on-chip tapered monopole antenna

TABLE I
SUMMARY AND COMPARISONS OF UWB ON-CHIP ANTENNA

Reference	[1]	**This Work**
Center Frequency	9.0 GHz	**7.7 GHz**
Bandwidth	2.2 GHz	**4.0 GHz**
Efficiency	0.6 %	**4.2 %**
Directivity Gain	5 dBi	**-10 dBi**
Area	4.4 mm^2	**1.2 mm^2**

bandwidth of 4 GHz shown in Fig. 4, and the radiation pattern plot is shown in Fig. 5. Also, the input impedance of the antenna is designed to match the maximum power transfer output impedance of the power amplifier. This not only saves an extra matching network but also reduces the overall loss of the system. A comparative performance summary of the on-chip antenna is listed in Table I.

E. Power Amplifier

Fig. 6 shows the schematic of proposed UWB power amplifier. Here M represents the mutual inductance of the transformer. A transformer feedback technique is adopted for a wideband input matching and simultaneous linearity improvement. A Comparison with conventional source-degenrated common source input stage with gate inductance matching could be carried out by way of Z_{in} analysis. The resulting input impedance for CS stage is:

$$Zin = \frac{gmLs}{Cgs} + j\left[\omega(Lg+Ls) - \frac{1}{\omega Cgs}\right] \quad (1)$$

While the input impedance of the proposed topology is

$$Zin = \frac{gm(Ls-M)}{Cgs} + j\left[\omega(Lg+2Ls-2M) - \frac{1}{\omega Cgs}\right] \quad (2)$$

The real part of input impedance in (2) has an extra factor M resulting from the mutual inductance. As both Ls and M are varying with frequency, an optimum value for M exists to ensure wider frequency matching range. The transformer design for such arrangement is shown in Fig. 7, using top metal of 6 µm width and 5 µm spacing between the two coils.The chosen dimensions for Ls (0.32 nH), and M (0.13 nH) at 8 GHz gives a coupling coefficient of 0.4. The simulation result by Ansoft HFSS™ shows that from 6 GHz to 10 GHz, the mutual inductance M is monotonically increasing alongwith Ls, giving a constant real-part over a wide range of frequencies than the conventional input topology. Fig. 8 shows the S_{11} comparison of both schemes.

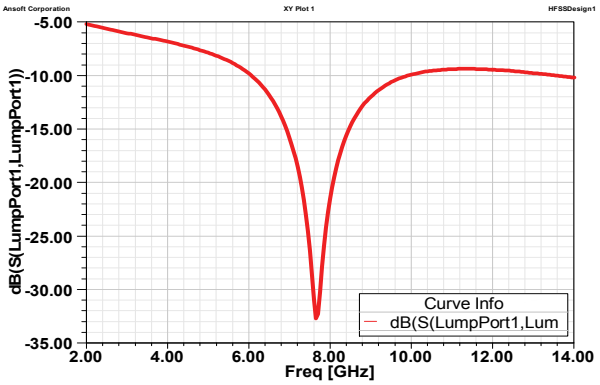


Fig. 4. S_{11} of the on-chip tapered monopole antenna

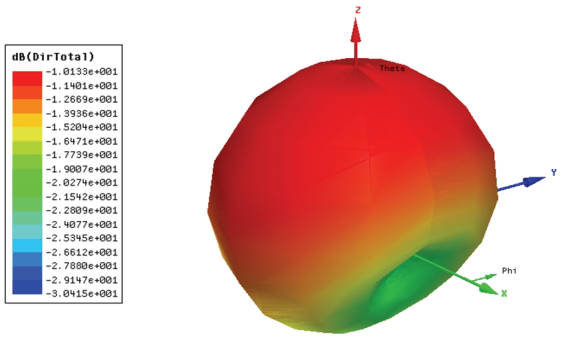


Fig. 5. Radiation Pattern of the on-chip tapered monopole antenna

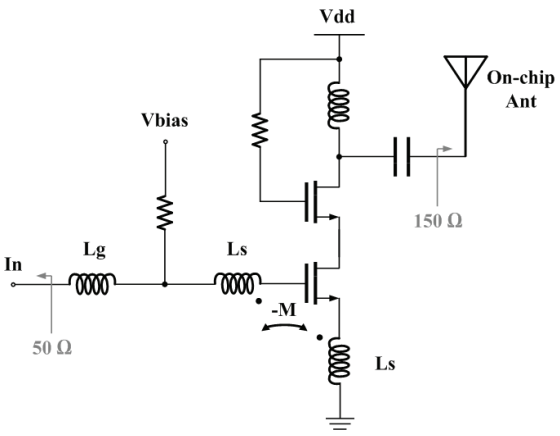


Fig. 6. The proposed UWB PA topology

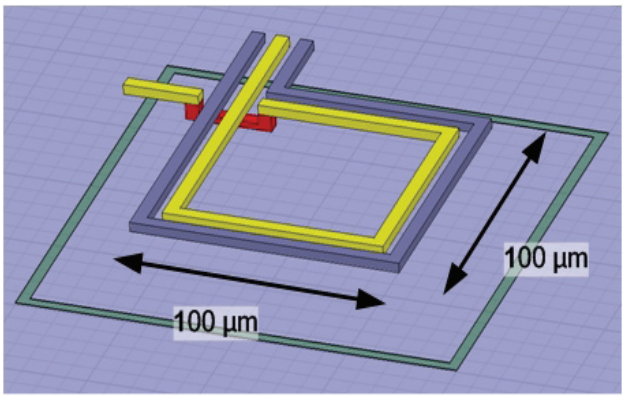


Fig. 7. The transformer for the wideband power amplifier

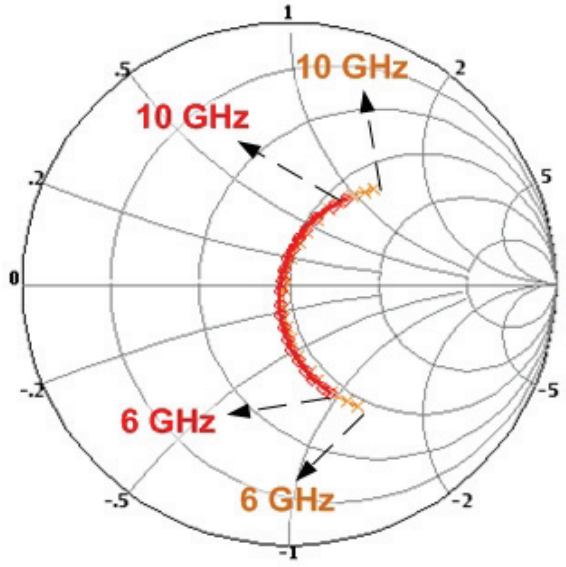


Fig. 8. S_{11} comparison of conventional input matching network and the proposed transformer feedback technique

IV. UWB Receiver

A. Low-Power, Low-Noise Amplifier

Fig. 9 shows the designed common-gate cascoded low-noise amplifier (CG-CLNA). Te proposed design is optimized to attain minimum noise and power levels while relaxing the linearity requirement to some extent. The transistor was biased to match g_m with 50 Ω source resistance. The input transistor dimensions were chosen to minimize the impact of gate-induced noise by increasing the transit frequency of the device (g_m to C_{gs} ratio). Since this noise component is proportional to $(\omega_o / \omega_t)^2$, a ratio of less than 0.03 is selected to insure near theoretical noise figure of 3.1 dB (determined by the CG topology). Table II shows the numerical values for all circuit components. The bias circuit has off chip provision and the design takes into account pad and bond wire parasitic through practical models published by MOSIS.

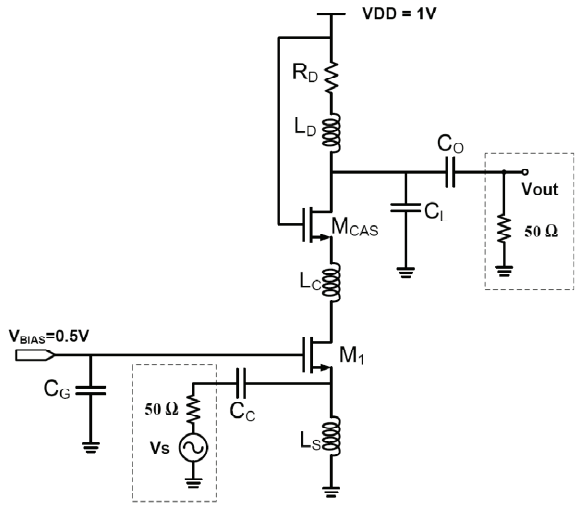


Fig. 9. Common-Gate cascoded low-noise amplifier

TABLE II
DEVICES DIMENSIONS FOR CG-CLNA

M_1 [µm/µm]	M_2 [µm/µm]	L_S [nH]	L_C [nH]	L_D [nH]	C_C [pF]	C_G [pF]
80/0.19	130.2/0.12	6.68	2.96	2.17	2.4	44

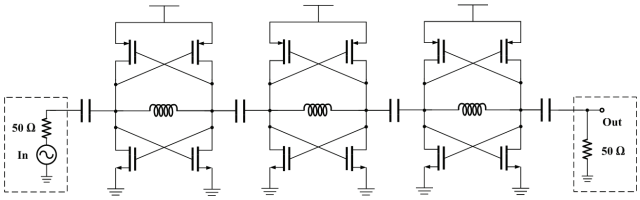


Fig. 10. Schematic of the active bandpass filter

B. On-Chip Active Bandpass Filter

The schematic of the active bandpass filter is shown in Fig. 10, a three-order shunt-type resonance capacitive coupled topology is implemented with complementary cross-coupled pairs to compensate the loss of on-chip inductor, thus for a higher Q-factor for the resonance. The center frequency is 8.02 GHz with 3.96 GHz bandwidth. The mid- band insertion loss is 2.9 dB and the return loss is all less than -10 dB from 6 GHz to 10 GHz. The noise figure is 6.6 dB at center frequency, while the power consumption is 0.42 mW.

V. Simulation Results

Fig. 11. shows the layout of all proposed blocks. The S-parameter simulation results for PA are given in Fig. 12, while the comparative performance results of UWB PA are summarized in Table III. Fig. 13 and Fig 14 along with Table IV depict the performance metrics of the UWB transmitter. Fig. 15 to 17 show the performance results of the receiver front end. Table V summarizes the performance of the LNA and compares it with published work.

TABLE III
SUMMARY AND COMPARISONS UWB-PA PERFORMANCES

Reference	CMOS Tech.	Freq. Range	Avg. Gain	Avg. OP_{1dB}	Group Delay Variation	Power Consumption)	Avg. PAE
[1]	0.18 µm	8 - 10 GHz	13.2 dB	N/A	N/A	20 mW	N/A
[9]	0.18 µm	6 - 10 GHz	8.5 dB	5 dBm	N/A	18 mW	14.4 %
[8]	0.18 µm	3.1 – 4.8 GHz	19 dB	-4.2 dBm	N/A	25 mW	1.5 %
This Work	**0.13 µm**	**6 – 10 GHz**	**10.1 dB**	**0.1 dBm**	**18.6 % from 90ps**	**4.2 mW**	**21.6 %**

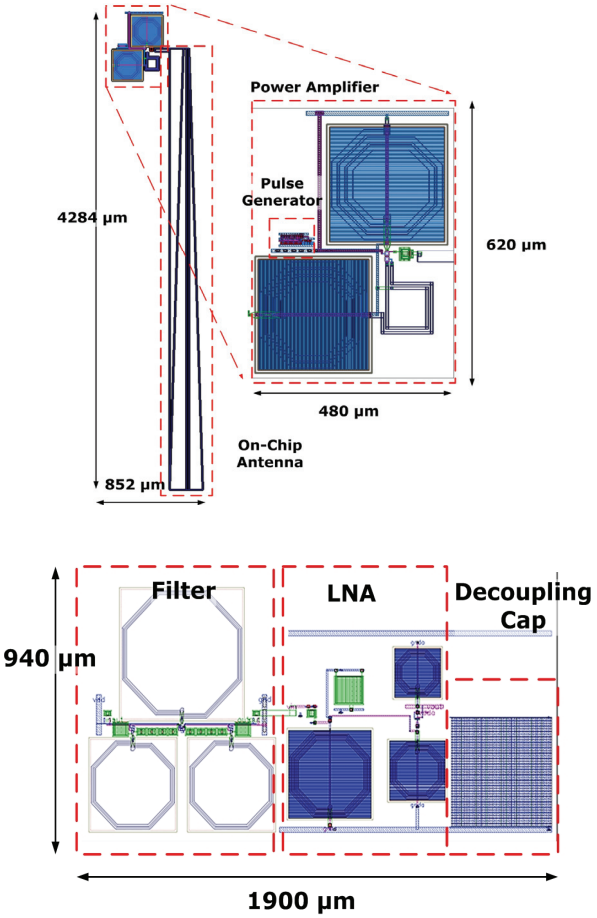


Fig. 11. Layout view of the UWB transmitter and receiver front end

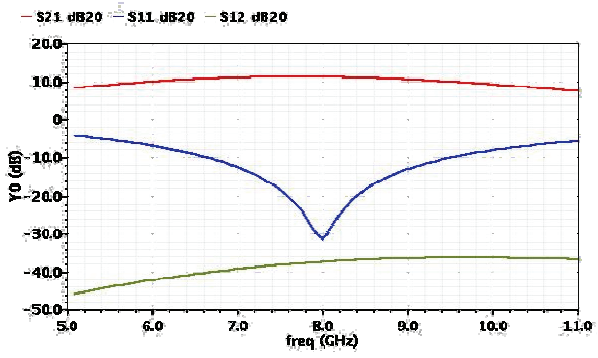


Fig. 12. S-parameters of the power amplifier

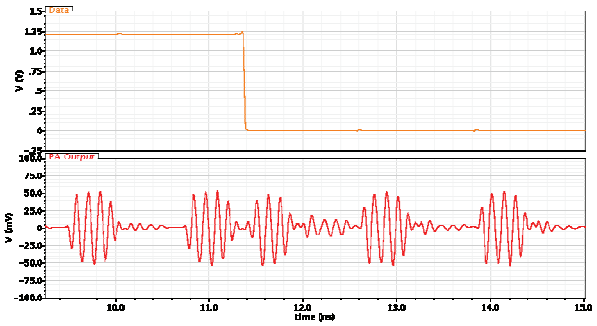
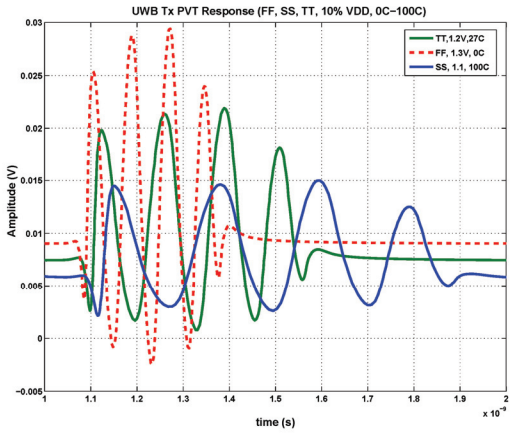


Fig. 13. Output transient signal of the UWB transmitter (pulse generator and power amplifier @ 750Mbps)



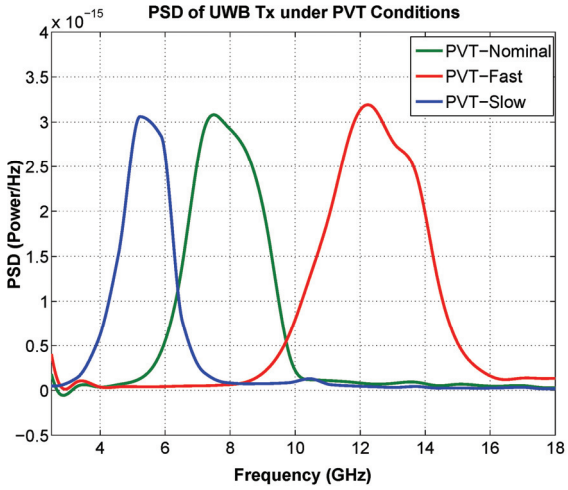


Fig. 14. Transient and spectrum simulation under PVT variations of UWB pulse generator

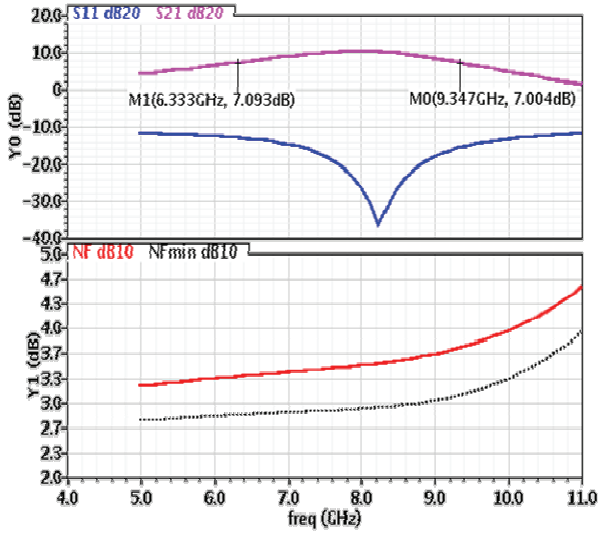


Fig. 15. S11, S21, NF and NFmin of LNA

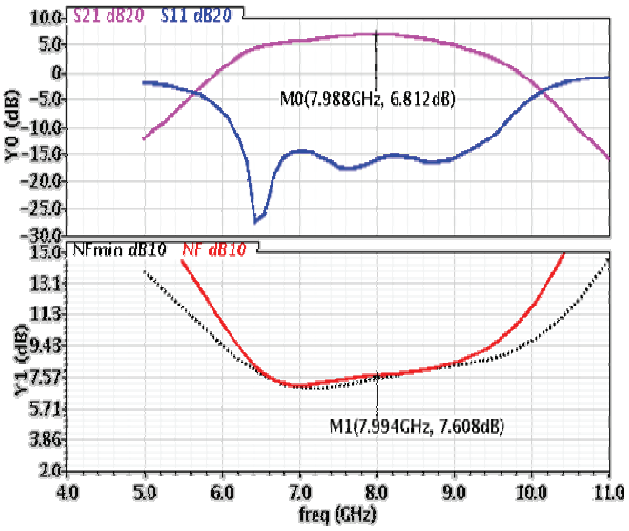


Fig. 17. S11, S21, NF and NFmin of LNA combined with the BPF

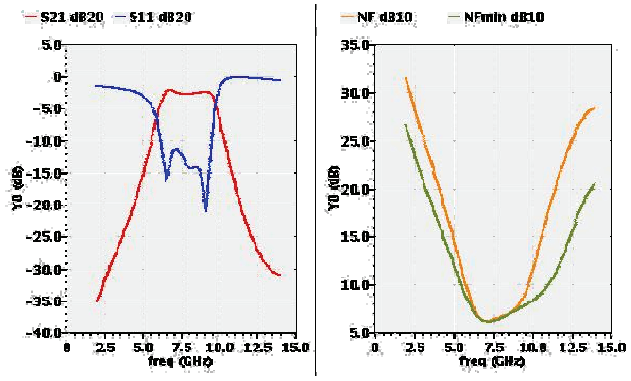


Fig. 16. S11, S21, NF and NFmin of the BPF

TABLE IV
SIMULATED PERFORMANCE AND SUMMARY OF UWB TRANSMITTER

Antenna	External	Embedded
Center Frequency	8.0 GHz	8.0 GHz
Energy Consumption	3 pJ/bit (@ 1Gbps)	7 pJ/bit (@ 1Gbps)
Technology	0.13µm CMOS	
Supply Voltage	1.2 V	
Maximum Data Rate	1 Gbps	
Operation Band	6-10GHz	

VI. CONCLUSION

We have proposed a very low power UWB transmitter and receiver for energy constrained applications. This architecture can support high data rates (up to 1 Gbps) while consuming only 7 pJ/bit. An on-chip antenna is designed for more compact size and more self-contained approach which is critical for miniaturized sensing nodes. A power amplifier is designed to support 6-to10 GHz operation. The receive side includes an efficient low noise amplifier and an active band pass filter. We successfully demonstrated fully functional simulation results for the transmitter and the designed part of the receiver. The future work includes a PLL design to minimize the variability of the transmitter performance parameters. The completion of the full receiver in the 6-10 GHz band is also a topic of interest for future work.

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TABLE V
SIMULATED PERFORMANCE AND COMPARISON OF WIDEBAND LNAS

Reference	Technology	BW [GHz]	NF [dB]	S_{21} [dB]	S_{11} [dB]	IIP3 [dBm]	Supply [V]	Power [mW]	Area [mm^2]
[10]	130 nm	3-5	3.5 ~ 5.5	6.4 ~ 9.5	< -10.0	-0.8	1.2	16.5	~ 1.08
[11]	90 nm	0.5-5	2.3-2.6	21-22*	< -10.0	-8.8	1.8	12	0.012
[12]	180 nm	6-10	4.75	11.6	<-9	1.15	1.8	11.6	0.81
This Work	**130 nm**	**6.3-9.4**	**3.3-3.7**	**7~10**	**<-13**	**-6.8**	**1**	**2.56**	**0.51**

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