A Software Defined Radio Receiver for the AM Frequency Band

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# Software Defined Radio Receiver

<table>
<thead>
<tr>
<th>SDR Receiver</th>
<th>Typical Receiver</th>
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<tbody>
<tr>
<td>Multiple wireless protocols</td>
<td>One wireless protocol</td>
</tr>
<tr>
<td>Multiple channels</td>
<td>Single channel</td>
</tr>
<tr>
<td>All demodulation performed in DSP</td>
<td>Mix down to IF and Baseband</td>
</tr>
<tr>
<td>Tunable Band-pass filter</td>
<td>Tunable Local Oscillator</td>
</tr>
<tr>
<td>Digitally programmable gain amplifier</td>
<td>Analog automatic gain control</td>
</tr>
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</table>

- **Note:** For the scope of this project, the receiver is limited to the AM frequency band.
Common Gate Low Noise Amplifier

- \( \frac{1}{g_m} \approx R_{\text{antenna}} \) (300 Ω)
- \( A_v \approx g_m R_{\text{load}} \)
  \( \approx 3.33 \text{ mS} \times 3 \text{ kΩ} \)
  \( \approx 20 \text{ dB} \)
- N-well resistor for a balance of high process tolerance and low noise figure
- 333 mV gate bias with 1 kΩ impedance
CGLNA Results

Gain over 3 Process Variation Corners

Noise Figure over 3 Process Variation Corners
OTA-C Band-Pass Filter

- 2\textsuperscript{nd} order tunable filter allows variation in:
  - Gain
  - Band width, Q
  - Center Frequency

\[ A = \frac{V_o}{V_i} = \frac{(gm_0 \times C_1 \times s)}{C_1 \times C_2 \times s^2 + C_1 \times gm_3 \times s + gm_0^2} = \frac{gm_0 \times s}{s^2 + \frac{gm_3}{C_2} \times s + \frac{gm_0^2}{C_1 \times C_2}} \]

\[ \omega_0 = \frac{gm_0}{\sqrt{C_1 \times C_2}} \]

\[ Q = \frac{gm_0}{gm_3} \times \sqrt{\frac{C_2}{C_1}} \]

\[ BW = \frac{\omega_0}{Q} = \frac{gm_0}{\sqrt{C_1 \times C_2}} \times \frac{gm_3}{C_2} \]

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Software Defined Radio Receiver
OTA

- Fully Differential, Fully Balanced
  - Cancels common mode signals, noise, supply variations
  - Eliminates even order distortion
- OTA outputs DC bias following Gm stages
- Low bias current and PMOS transistor input to reduce $1/f$ noise
Bandpass Filter Performance

- Power - 150μW
- Tunable - 500kHz to 1.7MHz
- Variable bandwidth - 50kHz – 200kHz
Programmable Gain Amplifier

- Stage 1: Source Follower Buffer
- Stage 2: Resistive feedback amplifier
  - Stage 2a: Common Gate amplifier
  - Stage 2b: Common Source amplifier
Programmable Gain Amplifier

\[ i_{in} = \frac{v_{in}}{2R_{in}} + \frac{v_{out}}{2R_{f}} \]

\[ \frac{v_{out}}{2A} = \frac{v_{in}}{2R_{in}} + \frac{v_{out}}{2R_{f}} \]

\[ v_{out} \left( \frac{1}{2A} + \frac{1}{2R_{f}} \right) = v_{in} \left( \frac{1}{2R_{in}} \right) \]

\[ \frac{v_{out}}{v_{in}} = \frac{1}{\frac{1}{2A} - \frac{1}{2R_{f}}} \]

\[ \frac{v_{out}}{v_{in}} \approx -\frac{R_{f}}{R_{in}} \quad \text{when } A \gg R_{f} \]
Gain Linearity

- Linear Gain improves DSP control accuracy
- Linearity degrades at lower gain
Resistor Array

- Digitally controllable
- Large FETs
- Linear resistors equal in size
Overall Gain

- System performance at max and min frequencies
Overall Noise Figure

- Flicker noise dominates at AM frequencies
## SDR System Level Results

<table>
<thead>
<tr>
<th>Specifications</th>
<th>1750 kHz Simulation</th>
<th>500 kHz Simulation</th>
<th>Target</th>
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</thead>
<tbody>
<tr>
<td>Peak Gain (dB)</td>
<td>66.04</td>
<td>69.72</td>
<td>40</td>
</tr>
<tr>
<td>3 dB Bandwidth (kHz)</td>
<td>120</td>
<td>166</td>
<td>100</td>
</tr>
<tr>
<td>Settling Time (ns)</td>
<td>12</td>
<td>9</td>
<td>20</td>
</tr>
<tr>
<td>Noise Figure at Peak Gain (dB)</td>
<td>6.197</td>
<td>13.64</td>
<td>7</td>
</tr>
<tr>
<td>Highest Noise Figure (dB)</td>
<td>13.92</td>
<td>13.64</td>
<td>7</td>
</tr>
<tr>
<td>Output Voltage Swing (mV)</td>
<td>6</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>2.94</td>
<td>2.90</td>
<td>4</td>
</tr>
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Questions?