A Software Defined Radio Receiver for the AM Frequency Band

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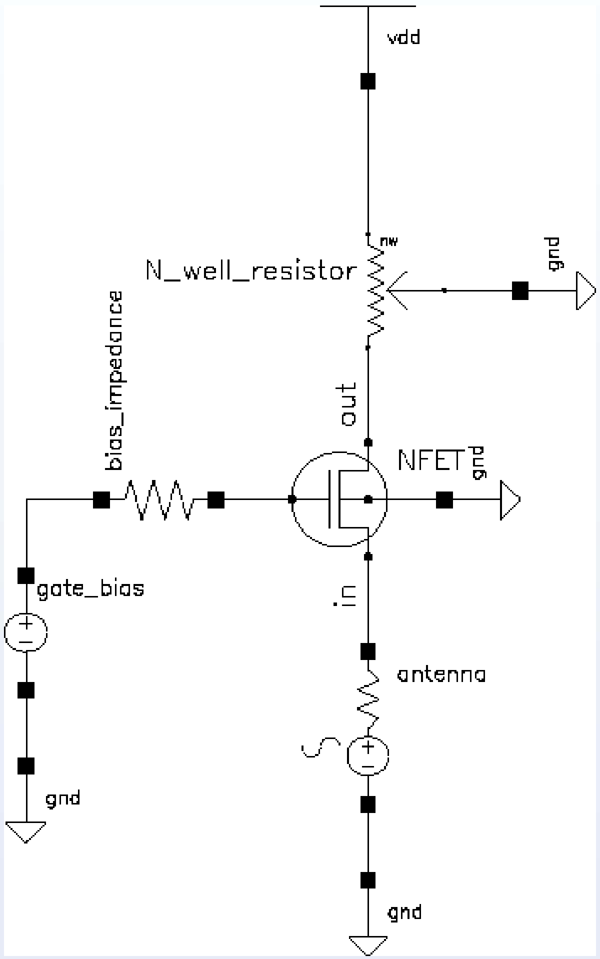
Software Defined Radio Receiver

SDR Receiver	Typical Receiver
Multiple wireless protocols	One wireless protocol
Multiple channels	Single channel
All demodulation performed in DSP	Mix down to IF and Baseband
Tunable Band-pass filter	Tunable Local Oscillator
Digitally programmable gain amplifier	Analog automatic gain control

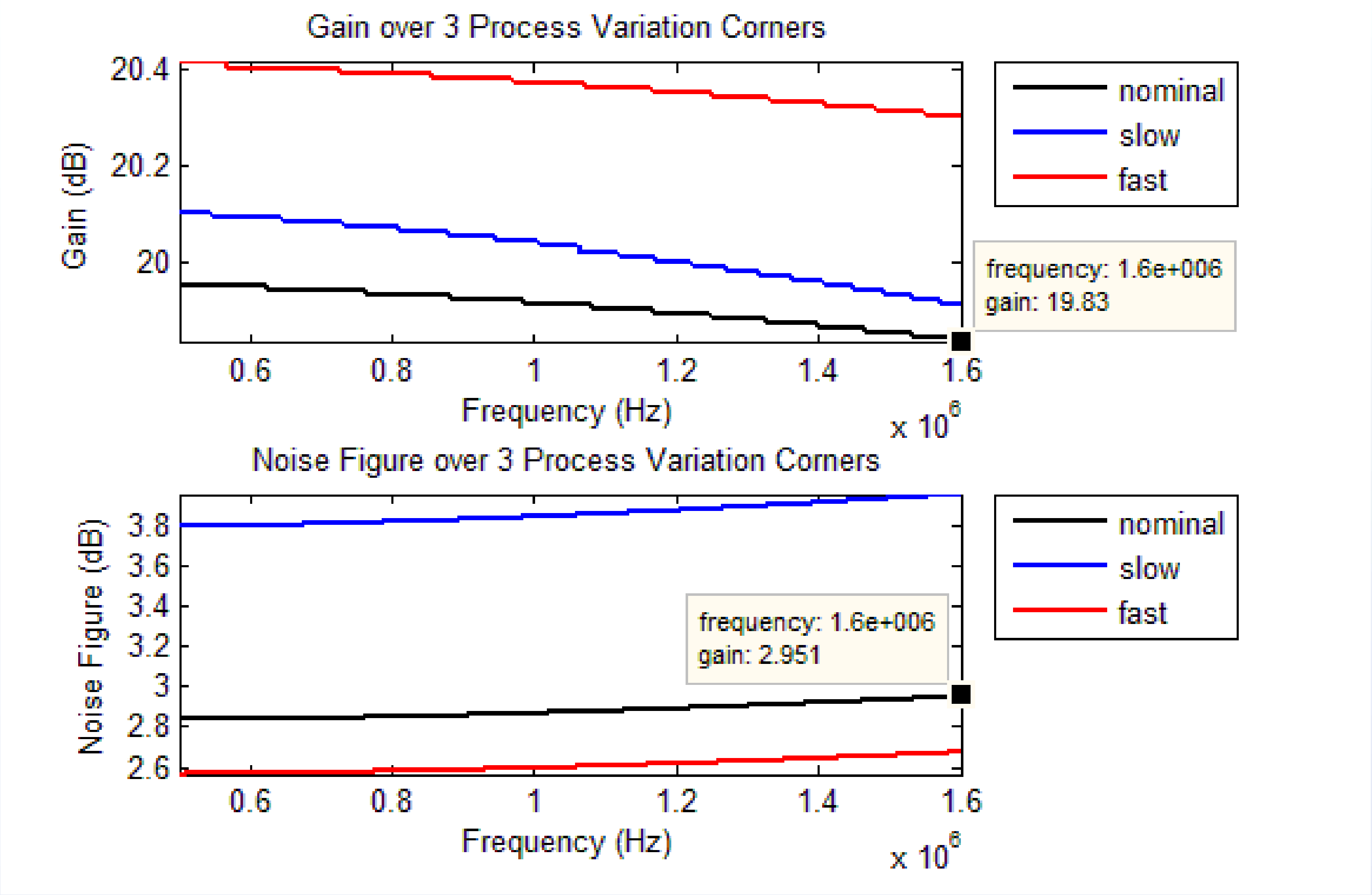
- Note: For the scope of this project, the receiver is limited to the AM frequency band.

Common Gate Low Noise Amplifier

- $1/g_m \approx R_{antenna}$ (300 Ω)
- $A_v \approx g_m R_{load}$
  $\approx 3.33\text{ mS} \times 3\text{ k}\Omega$
  $\approx 20\text{ dB}$
- N-well resistor for a balance of high process tolerance and low noise figure
- 333 mV gate bias with 1 kΩ impedance

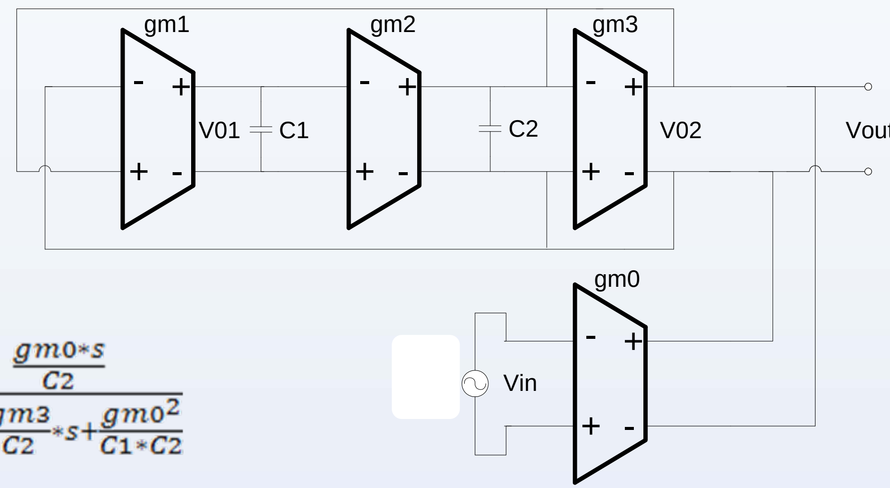


CGLNA Results



OTA-C Band-Pass Filter

- 2^{nd} order tunable filter allows variation in
  - Gain
  - Band width, Q
  - Center Frequency



$$A = \frac{Vo}{Vi} = \frac{(gm0*C1*s)}{C1*C2*s^2+C1*gm3*s+gm0^2} = \frac{\frac{gm0*s}{C2}}{s^2+\frac{gm3}{C2}*s+\frac{gm0^2}{C1*C2}}$$

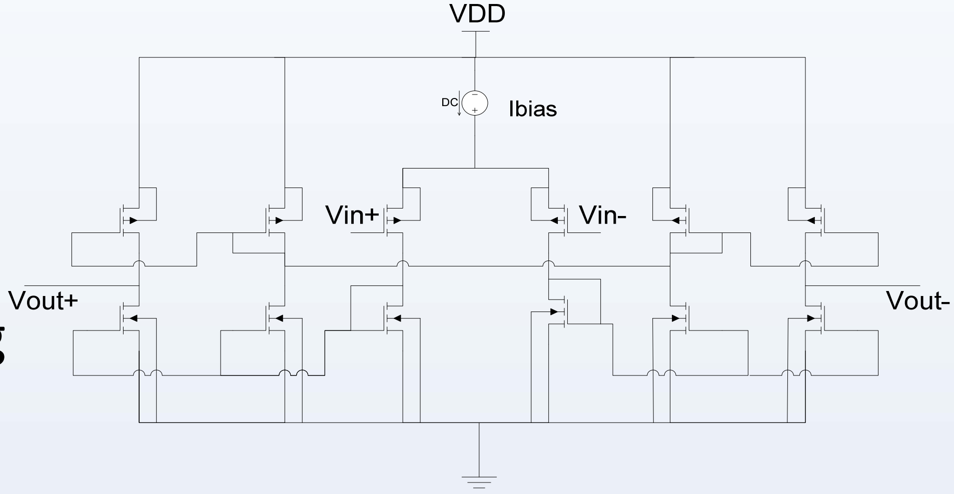
$$\omega_0 = \frac{gm0}{\sqrt{C1*C2}}$$

$$Q = \frac{gm0}{gm3}*\sqrt{\frac{C2}{C1}}$$

$$BW = \frac{\omega 0}{Q} = \frac{\frac{gm0}{\sqrt{C1*C2}}}{\frac{gm0}{gm3}*\sqrt{\frac{C2}{C1}}} = \frac{gm3}{C2}$$

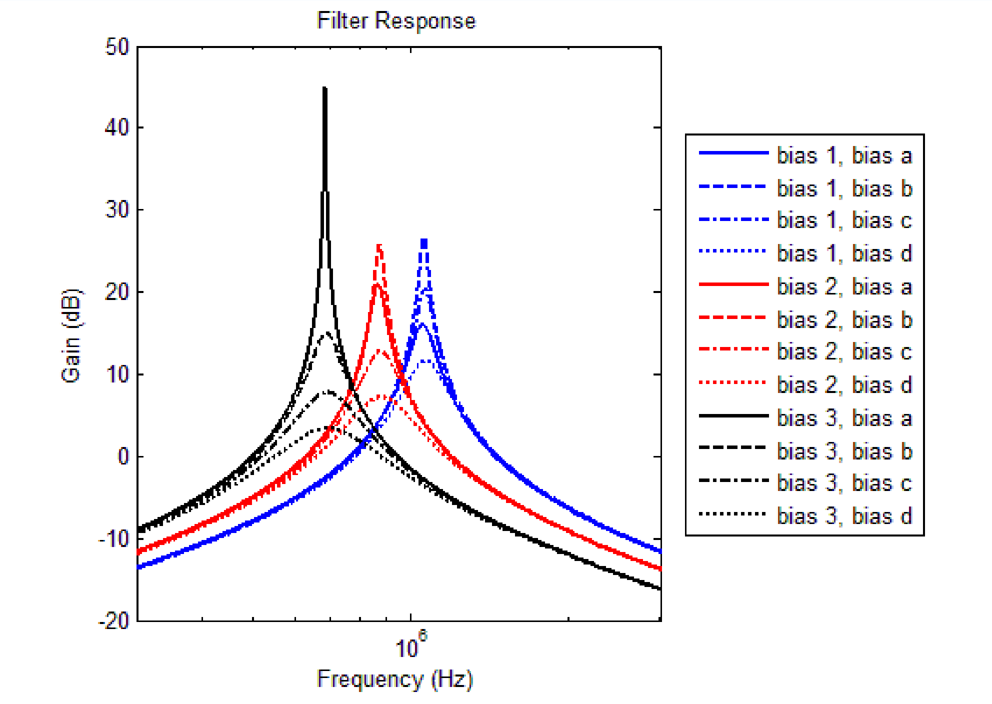
O T A

- Fully Differential, Fully Balanced
  - Cancels common mode signals, noise, supply variations
  - Eliminates even order distortion
- OTA outputs DC bias following Gm stages
- Low bias current and PMOS transistor input to reduce 1/f noise



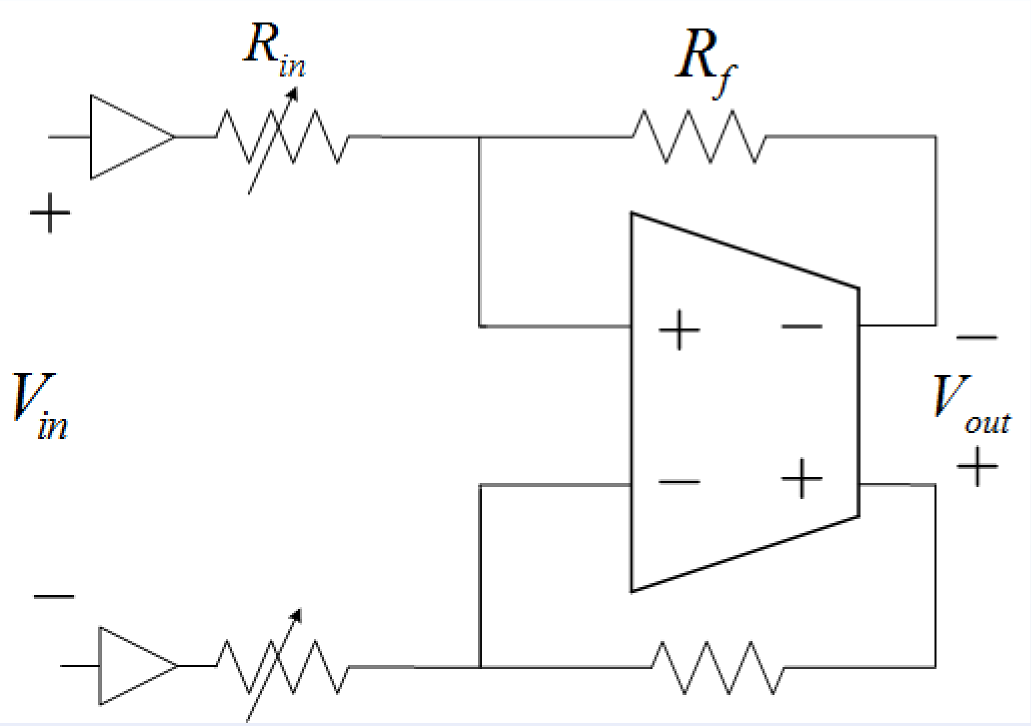
Bandpass Filter Performance

- Power - 150µW
- Tunable - 500kHz to 1.7MHz
- Variable bandwidth - 50kHz – 200kHz



Programmable Gain Amplifier

- Stage 1: Source Follower Buffer
- Stage 2: Resistive feedback amplifier
  - Stage 2a: Common Gate amplifier
  - Stage 2b: Common Source amplifier



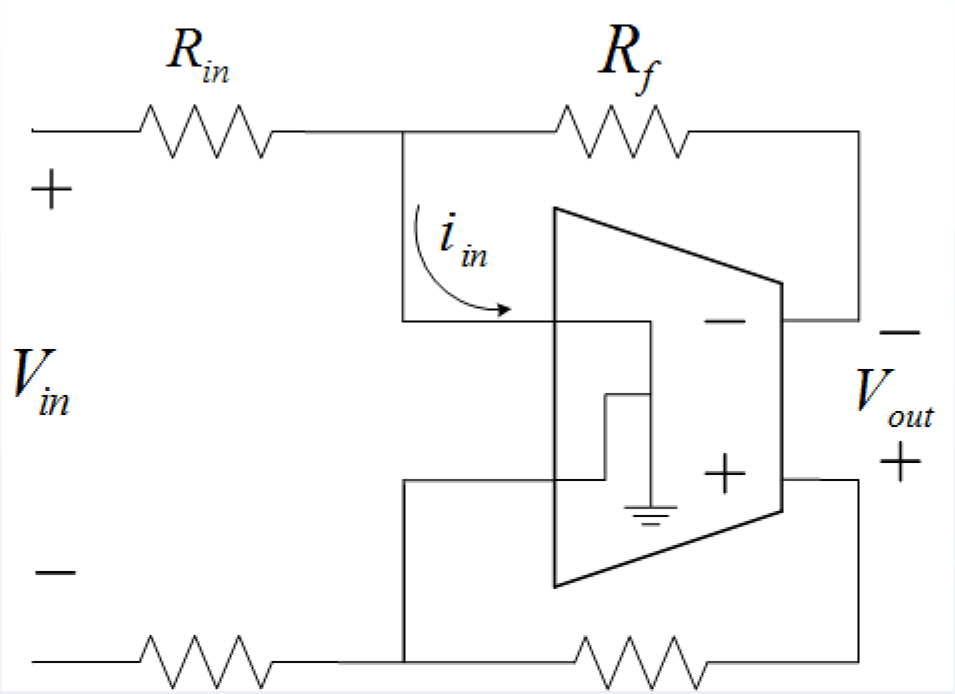
Programmable Gain Amplifier

$$i_{in} = \frac{v_{in}}{2R_{in}} + \frac{v_{out}}{2R_f}$$

$$\frac{v_{out}}{2A} = \frac{v_{in}}{2R_{in}} + \frac{v_{out}}{2R_f}$$

$$v_{out}\left(\frac{1}{2A} + \frac{1}{2R_f}\right) = v_{in}\left(\frac{1}{2R_{in}}\right)$$

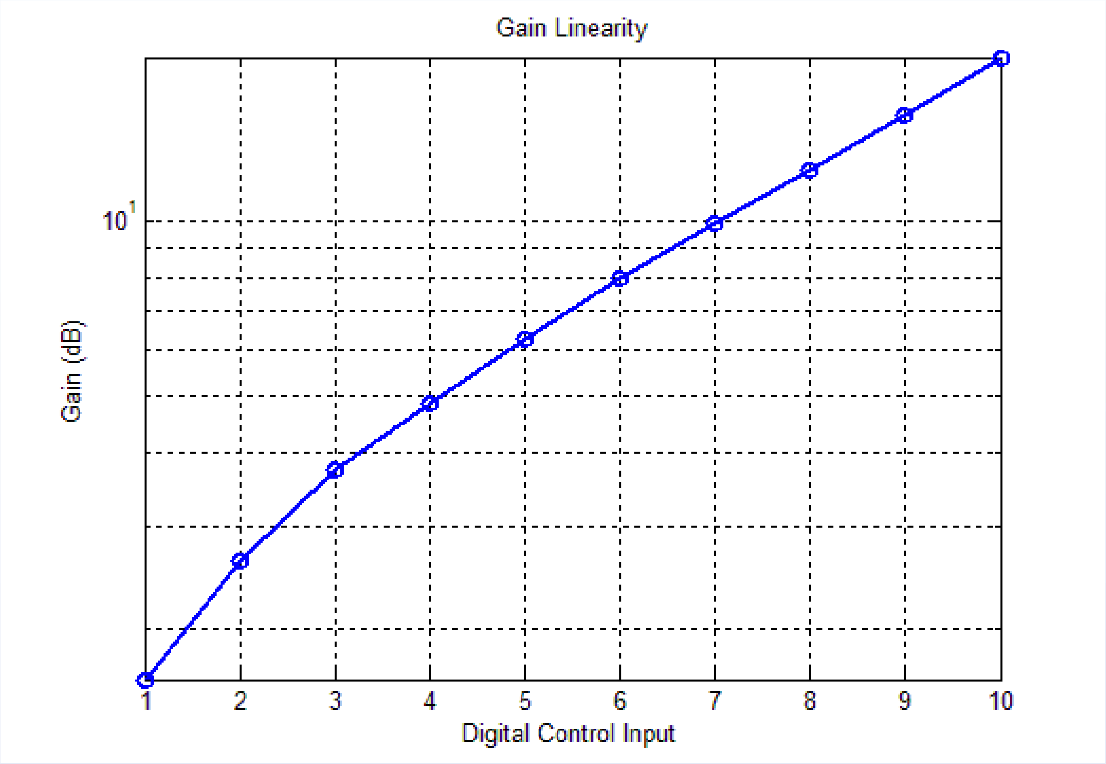
$$\frac{v_{out}}{v_{in}} = \frac{\frac{1}{2R_{in}}}{\frac{1}{2A} - \frac{1}{2R_f}}$$



$$\frac{v_{out}}{v_{in}} \approx -\frac{R_f}{R_{in}} \qquad when\ A \gg R_f$$

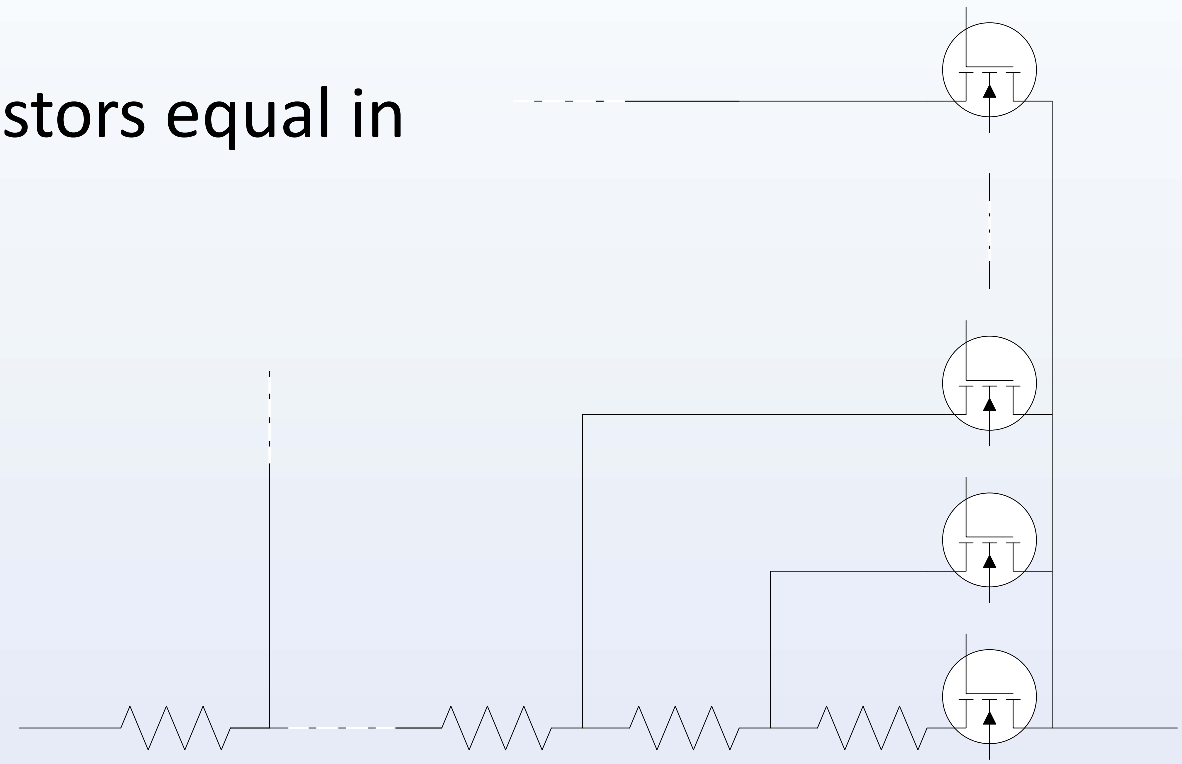
Gain Linearity

- Linear Gain improves DSP control accuracy
- Linearity degrades at lower gain



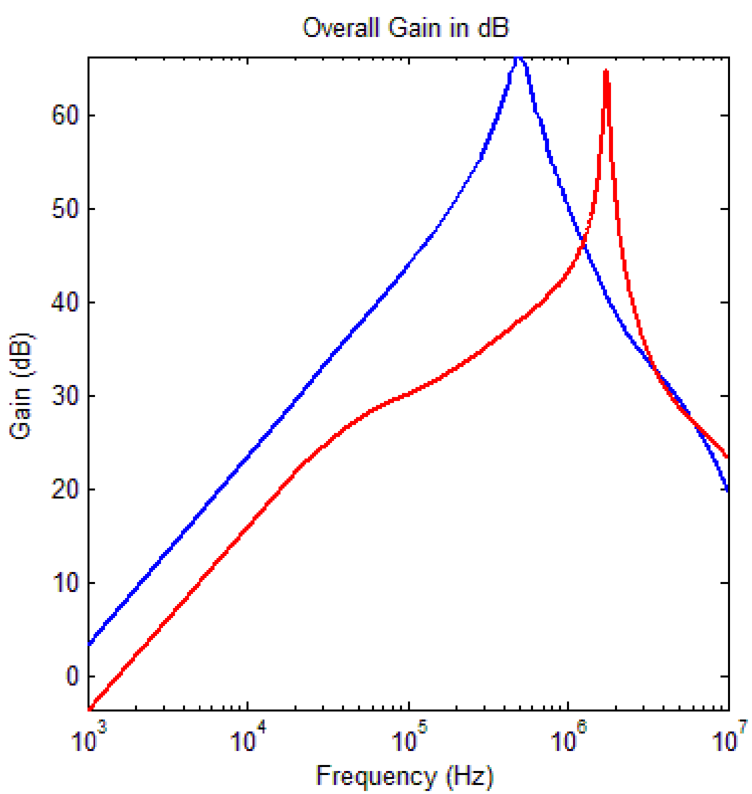
Resistor Array

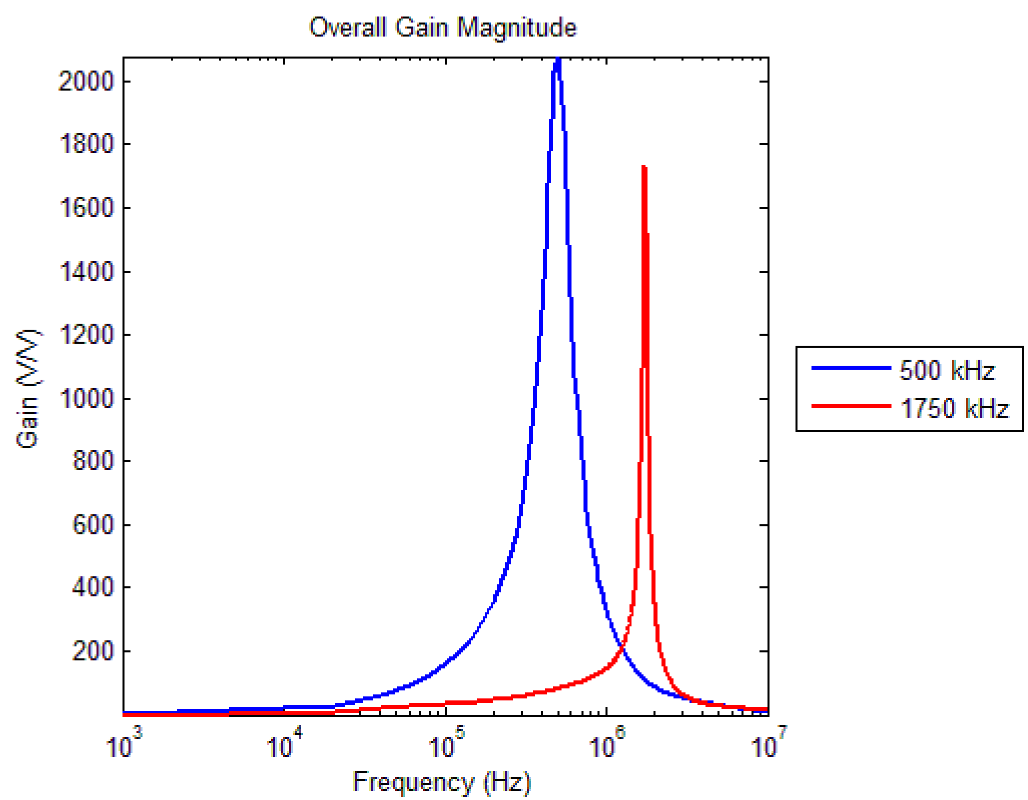
- Digitally controllable
- Large FETs
- Linear resistors equal in size



Overall Gain

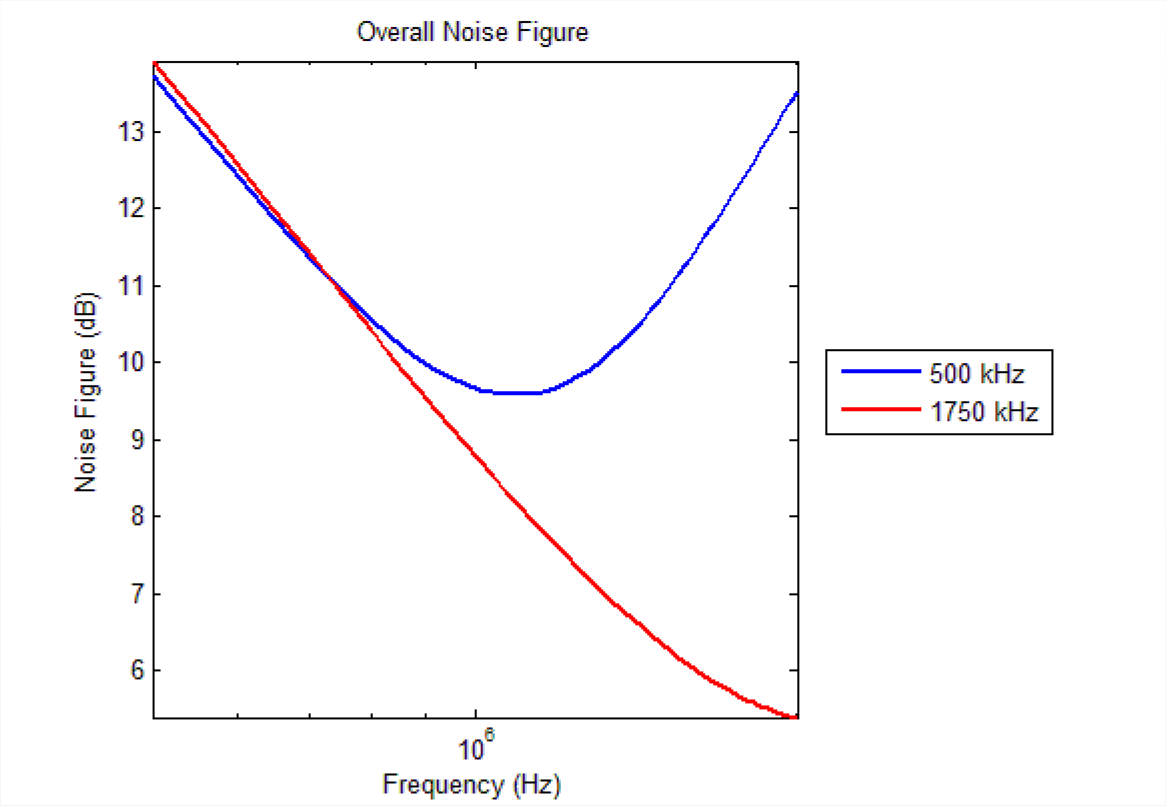
- System performance at max and min frequencies





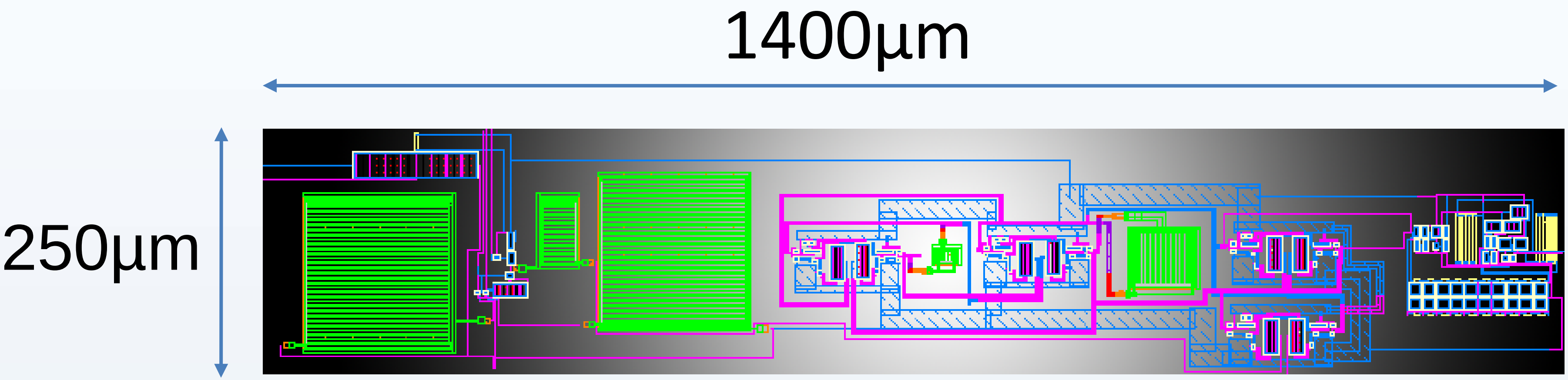
Overall Noise Figure

- Flicker noise dominates at AM frequencies



SDR System Level Results

Specifications			
Specification	**1750 kHz Simulation**	**500 kHz Simulation**	**Target**
Peak Gain (dB)	66.04	69.72	40
3 dB Bandwidth (kHz)	120	166	100
Settling Time (ns)	12	9	20
Noise Figure at Peak Gain (dB)	6.197	13.64	7
Highest Noise Figure (dB)	13.92	13.64	7
Output Voltage Swing (mV)	6	6	3
Power Consumption (mW)	2.94	2.90	4



Questions?