A Software Defined Radio Receiver for the AM Frequency Band

Veselin Dimitrov, Eui Min Jung, Daniel Prince

***Abstract*—A software defined radio receiver architecture is presented for the AM frequency band. The architecture is comprised of a common gate low noise amplifier, a tunable band-pass filter, and a digitally programmable gain amplifier. The topology uses a .13µm CMOS technology and 1.2V supply. A total gain of 60dB is achieved.**

***Index Terms*—Software Defined Radio, AM Radio, Low Noise Amplifier, Tunable Band-Pass Filter, Programmable Gain Amplifier**

I. Introduction

Software defined radio (SDR) classifies a device that performs some or all of its function in digital circuitry. This technology provides limitless possibilities for wireless communication. With purely hardware systems, devices can only communicate with other devices that transmit over the same wireless channels. When all functions are performed in a digital signal processor (DSP), software can easily handle multiple channels.

On the push to develop SDR, varying levels have been achieved. One source [3] defines a five tier system starting with a purely analog radio as tier 0 and progressing up to tier 4 where an antenna is connected directly to a DSP chip. To this point, tier 4 is only theoretical and no systems have been developed that fit this classification. The system discussed in this paper is classified under tier 3, which is defined as a topology where digital processing starts at the RF range [3].

II. Circuit analysis

A. Overall System

The challenges associated with tier 3 SDR are much different than a typical receiver. First, typical receivers tune a local oscillator to select the channel frequency. In the tier 3 system, analog demodulation has been removed, so there is no mixer or local oscillator to tune. To solve this problem, a tunable band-pass filter was implemented. Second, typical receivers select one channel and use automatic gain control to regulate various power levels of the input signal. Tier 3 systems must adjust the gain according to the strongest power channel in the chosen band. This requires a digitally programmable gain amplifier (PGA) to be included in the receiver path. With this block, the DSP can determine if the signal is reaching the full swing in the analog-to-digital converter (ADC), and feedback a digital bit to the PGA to adjust accordingly. A third challenge in this project, which has nothing to do with SDR, but more to do with the AM frequency band, is overcoming flicker noise. Flicker noise is the dominate noise source for these frequencies by a considerable margin. In order to reduce this noise contributor, the Low Noise Amplifier (LNA) has to be planned for flicker noise reduction.

B. Low Noise Amplifier

As the first component of the wireless receiver, the input of the LNA is an AM band loop antenna, and the output of the LNA is the input of the differential filter. Thus the LNA could either be single ended in favor of lower noise figure, or be differential to attenuate noise in the supply voltage. If it were to be single ended, the negative input of the filter would necessarily be connected to a DC bias voltage, and if it were to be differential, the negative input of the LNA would necessarily be connected to ground. Because an ideal voltage supply is available as part of the simulation tool, a single ended implementation was chosen to better understand the project's performance potential. The common gate topology was chosen for its low theoretical noise figure of 2.2dB, the schematic of which is shown in Fig. 1.

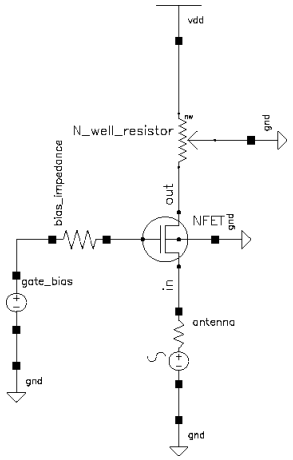

Fig. 1. LNA circuit topology

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The common gate configuration has an input impedance of approximately $1/g_m$ and gain of approximately g_m*R_D. In order to power match with the antenna with an assumed impedance of 300Ω, the transistor was sized to give a $1/g_m$ value of approximately 333mS. To meet the initial gain target of 20dB, the resistor value was set to approximately 3kΩ. An N-well resistor was chosen for its high tolerance to process variation (about 17% for the dimensions chosen) and good noise figure and gain performance. The gate bias of the transistor was set relatively high at 333 mV for low noise figure.

C. *Tunable Band-Pass Filter*

For the tunable band-pass filter in this project an OTA-C architecture was used. The OTA-C topology allows for tuning of Gain (A), Center frequency (ω_o), bandwidth (BW) and Q of the filter. The chosen structure employs four operational transconductance amplifiers (OTA) and two capacitors, therefore, providing four degrees of freedom. A block diagram of the filter is shown below in Fig. 2.

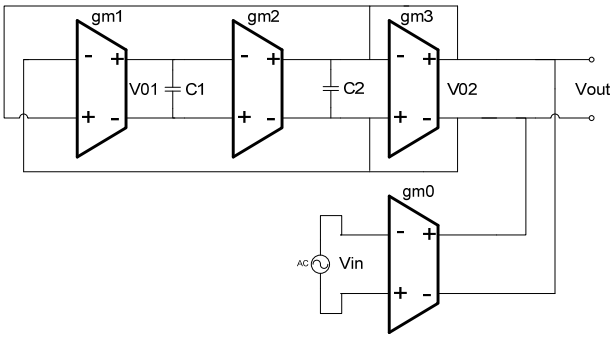

Fig. 2. Block diagram of OTA-C band-pass filter

The available four degrees of freedom allow, with careful biasing of the OTAs, independent control over all of the filter parameters. Analysis of the filter circuit yields very complex equations that are very impractical. In order to simplify the resulting governing formulas one can assume that $g_{m0} = g_{m1} = g_{m2}$. Making this assumption limits the flexibility of the filter, but still provides enough variability so that one can change the bandwidth and center frequency of the filter to all desirable values. The formulas that govern this filter are as follows:

$$A = \frac{Vo}{Vi} = \frac{(gm0*C1*s)}{C1*C2*s^2+C1*gm3*s+gm0^2} = \frac{\frac{gm0*s}{C2}}{s^2+\frac{gm3}{C2}*s+\frac{gm0\hat{}2}{C1*C2}} \quad (1)$$

$$\omega_0 = \frac{gm0}{\sqrt{C1*C2}} \quad (2)$$

$$Q = \frac{gm0}{gm3} * \sqrt{\frac{C2}{C1}} \quad (3)$$

From (2) and (3), using the crude approximation for Q equal to the center frequency divided by the bandwidth, one could estimate BW as:

$$BW = \frac{\omega 0}{Q} = \frac{\frac{gm0}{\sqrt{C1*C2}}}{\frac{gm0}{gm3}*\sqrt{\frac{C2}{C1}}} = \frac{gm3}{C2} \quad (4)$$

If tuning of bandwidth is required a change in the bias current for the g_{m3} stage should be sufficient to provide us with the desired BW. As the bias current increases, so does g_{m3} and the BW is increased. Increase in the bias current for the g_{m0}, g_{m1}, and g_{m2} stages increases g_{m0}, g_{m1}, and g_{m2} and therefore the center frequency is increased, as is evident from (2). A DSP, having higher algorithm capabilities will be able to supply independent variation in the bias currents for all four g_m stages. Doing this makes the above formulas invalid, but the additional complexity in setting BW, Q, A and ω_0 will result in much greater flexibility of the entire system. For an even greater expansion of the capabilities of this filter one could build each transconductor as a combination of sub-OTAs that are connected in parallel. In that case if changing the bias current does not provide sufficient parameter variation additional sub-OTAs can be turned on or off. The OTA chosen is a symmetrical, fully differential OTA. This topology cancels even order distortion, common mode noise, and common mode signals. The circuit implementation has inherent common mode feed forward (CMFF). Some of the more important characteristics are the use of PMOS transistors and small bias currents for the input differential pair. These two characteristics were important during the design phase as they allow for minimization of flicker noise, which, as previously mentioned, dominates the circuit at the frequencies of interest.

D. *Programmable Gain Amplifier*

The programmable gain amplifier topology shown in Fig. 3. has been chosen for linearity across the gain range [4].

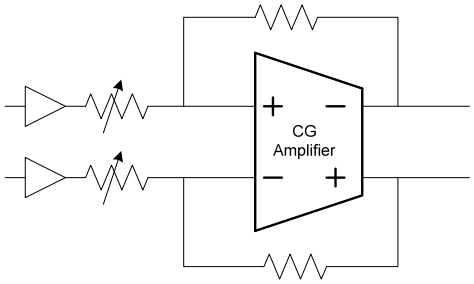

Fig. 3. The Programmable Gain Amplifier block diagram uses resistive feedback to amplify the signal. Digitally programmable input resistors vary the gain according to digital input bit settings.

In this topology, a digitally programmable input resistor, as shown in Fig. 4., alters the gain according to (5):

$$\text{Gain} = R_{f1}/R_1 \quad (5)$$

While altering the gain, the feedback factor remains constant through the use of a current gain amplifier.

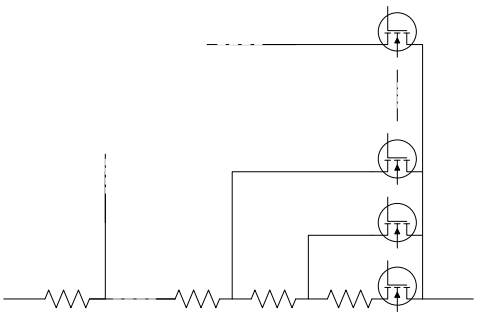

Fig. 4. The resistor array allows individual digital control lines to linearly alter the gain. The switches, implemented as NFET transistors, have a large channel cross section to reduce parasitic resistance.

This type of amplifier has low input impedance; as a result, the inputs act as a small signal ground. The additional ground between the resistors changes the feedback factor from (6) to (7).

$$\beta = \frac{R_1}{R_{f1}+R_1} \quad (6)$$

$$\beta = 1/R_{f1} \quad (7)$$

A source follower (SF) buffer stage was added before the input resistor array to provide high input impedance as seen by the band-pass filter.

Now that general impedance targets have been selected an amplifier topology can be determined. As a low input impedance topology, a common gate (CG) input is used. The input resistance of the CG topology is approximately $1/g_m$ of the input transistor. Therefore, the g_m should be boosted as high as possible to reduce input resistance. The output of the CG amplifier is fed into a common source (CS) differential pair to further increase gain of the amplifier and increase output impedance. [4]

The digitally programmable resistor network is a series array of ten resistors shown in Fig. 4.; each has a value of 100Ω. Between each pair of resistors, a tap wire connects to a switch to short the node to the amplifier input. In this way digital inputs can close switched one at a time to set the gain of the amplifier.

III. Results

A. Low Noise Amplifier

The plot of gain and noise figure versus frequency over nominal, slow, and fast process corner models is shown in Fig. 5. Under nominal conditions, the LNA achieves its lowest gain of 19.83dB and the highest noise figure of 2.951dB both at 1.6MHz. Gain improves at both the slow and the fast process corners, while the noise figure improves at the fast corner and worsens at the slow corner with an increase of approximately 1dB. It consumes approximately 240µW of power.

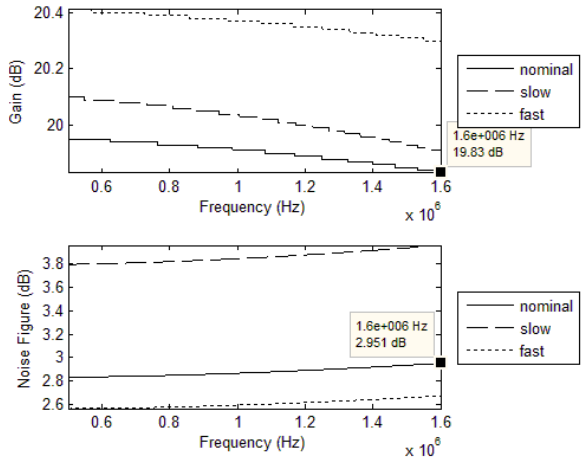

Fig. 5. LNA gain and noise figure versus frequency over nominal, slow, and fast process corner models. Under nominal conditions, the worst gain and noise figures are 19.83 and 2.951 dB, respectively.

B. Tunable Band-Pass Filter

As currently designed the filter maximum power consumption, needed to achieve the highest frequency of 1.7MHz, is approximately 150µW. The center frequency can be set anywhere in the band of interest from 500kHz to 1700kHz, as shown in Fig. 6., without the use of additional switched capacitors or addition of parallel OTAs to boost G_m, Q, and BW of the filter can also be independently adjusted to the desired value for any center frequency in the above mentioned bandwidth. This filter is a second order filter and if higher order filtering is desired OTA-C filters can be cascaded.

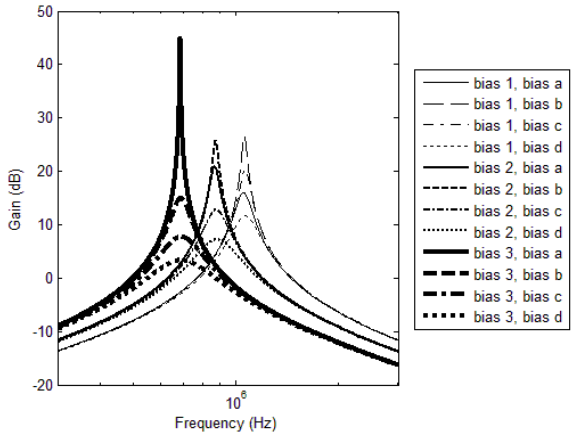

Fig. 6. The band-pass filter can independently vary center frequency and Q.

C. Programmable Gain Amplifier

The PGA was tested with a 100uV differential input to determine the performance of the block. The maximum power consumed was 431µW. As outlined in the initial system description (Section II Part A), a 20dB gain range was required to make the system flexible to inputs of variable power. The resulting PGA has a maximum gain of 19.06dB and a minimum gain of 1.44dB. Fig. 7. shows the range of gain levels and their corresponding digital control input.

Linearity of the gain is essential for the DSP to have precise control over the input. And, despite a small tail-off at the lower end of the gain range, a suitable linearity is achieved.

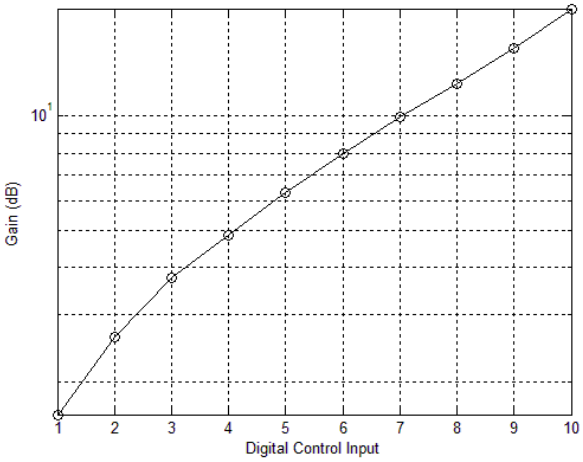

Fig. 7. The Gain of the PGA in decibels is linear with a slope near 2dB per control input increase. With linearity in PGA, the DSP is able to tune the proper gain for maximum signal input.

D. System Results

TABLE I
Specifications

Specification	1750 kHz Simulation**	500 kHz Simulation*	Target
Peak Gain (dB)	66.04	69.72	40
3 dB Bandwidth (kHz)	120	166	100
Settling Time (ns)	12	9	20
Noise Figure at Peak Gain (dB)	6.197	13.64	7
Highest Noise Figure (dB)	13.92	13.64	7
Output Voltage Swing (mV)	6	6	3
Output CM Voltage (mV)	435	381	600
Power Consumption (mW)	2.94	2.90	4

*Tested with a 1µV, 500kHz input source.
**Tested with a 1µV, 1750kHz input source.

The system test was performed with a 1µV source and a 300Ω series resistance fed into the input of the LNA. At the output, two 500fF capacitors were connected as a conservative estimate load of the ADC. The filter was then tuned to 500kHz followed by 1750kHz. These tests simulated the lower and upper bounds of the AM radio band. The performance at these frequencies is shown in Table I.

As evidence from the table, several of the specifications were not achieved. Most notably, the noise figure specification was not met. As previously stated, flicker noise is a major issue at such low frequencies. One suggested improvement upon this design is to use a BJT in the LNA, because bipolar transistors do not add flicker noise to the system. Another specification, not so critical to the system, but still not satisfied, was the common mode output voltage. Adding a PMOS source follower stage to the output can bring this voltage up. Also, using AC coupling capacitors can effectively isolate the common mode voltage of the PGA from that of the ADC.

Despite missing the previous two specifications, many other specs did meet and surpass the target figures. First, the overall system gain far exceeded the target of 40dB. This extra gain can be used to reduce the requirements on the ADC preamplifier. Second, the output voltage swing was double that of the minimum requirement. This is also a benefit to the ADC as it can now tolerate a reduced level of sensitivity. Finally, the power consumed by the system is much less than the target mostly due to lower power levels in the band-pass filter than expected.

Fig. 8. shows a view of the chip layout.

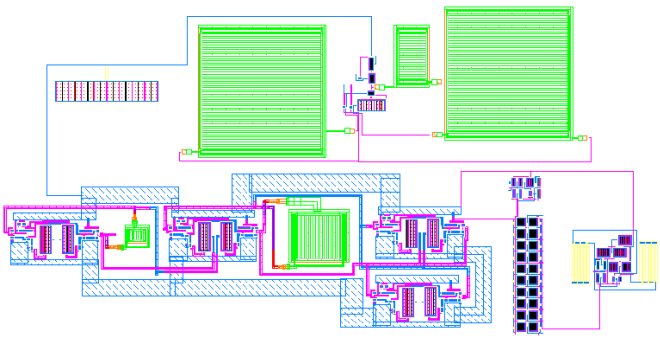

Fig. 8. Layout of the Software Defined Radio Sytem

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