

A Low Power Integrated UWB Transceiver with Solar Energy Harvesting for Wireless Image Sensor Networks

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- **Introduction**

- **Circuit Description**

- UWB transceiver architecture
- Low Drop-Out voltage regulator
- Pulse generator
- LNA

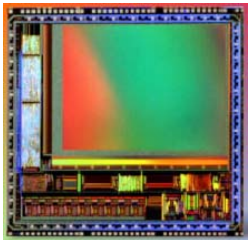
- **Conclusion**

- Summary of specification
- Layout view

- **Q & A**



CMOS imager



Sensor node



100 Mbps (@ VGA, 30 fps, 10-b)

Power consumption: < 100 mW

Need low-power integrated transceiver

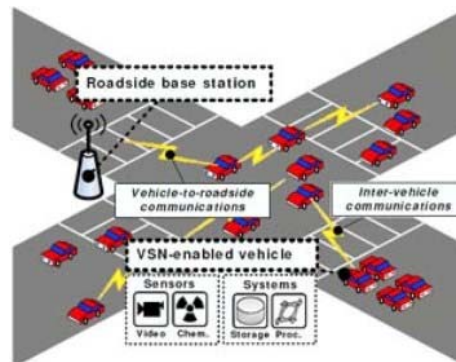
→ *low-power, short-range transceiver*

→ *UWB*

Environment monitoring



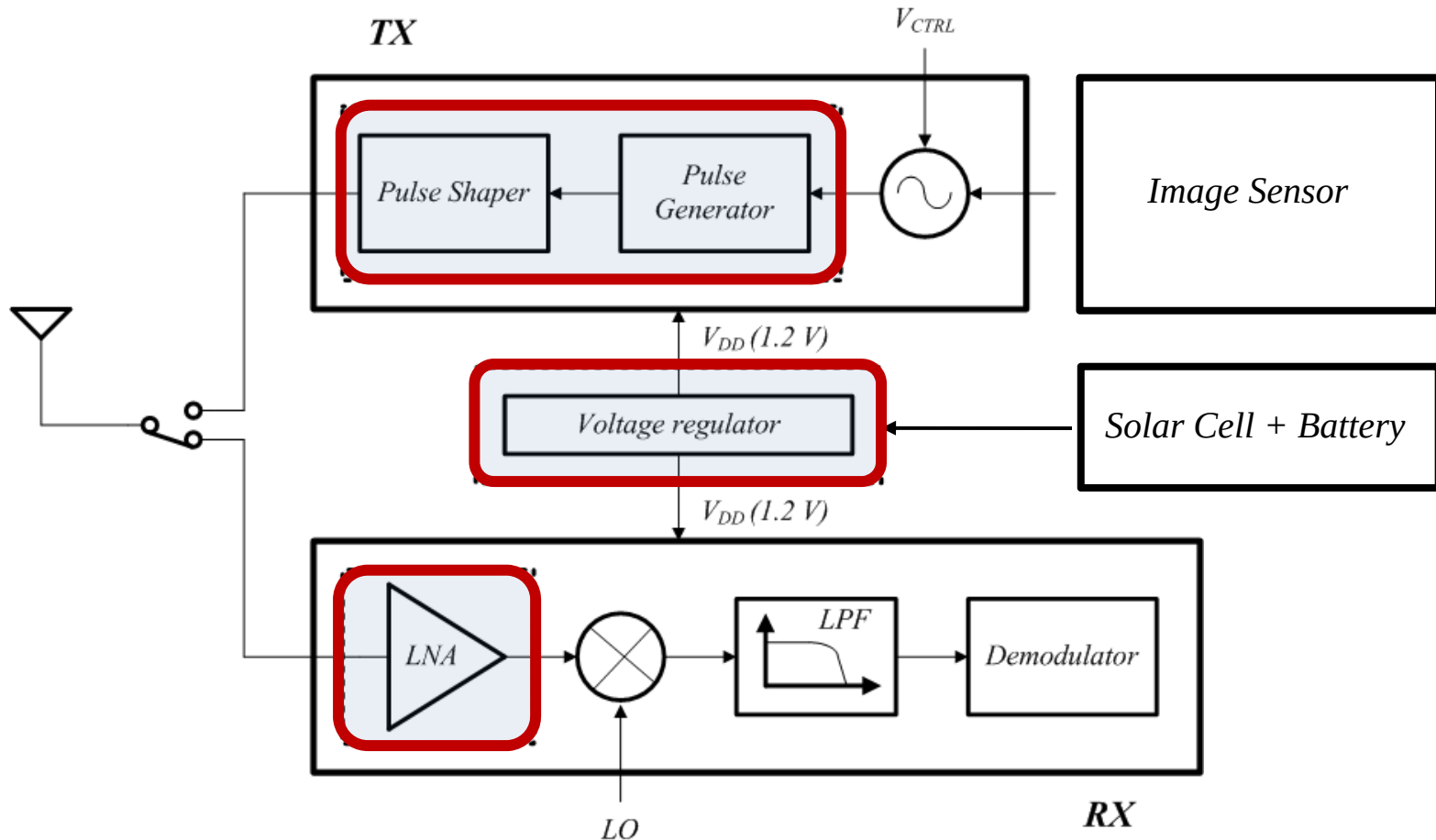
Traffic management



Military surveillance



Proposed UWB transceiver architecture

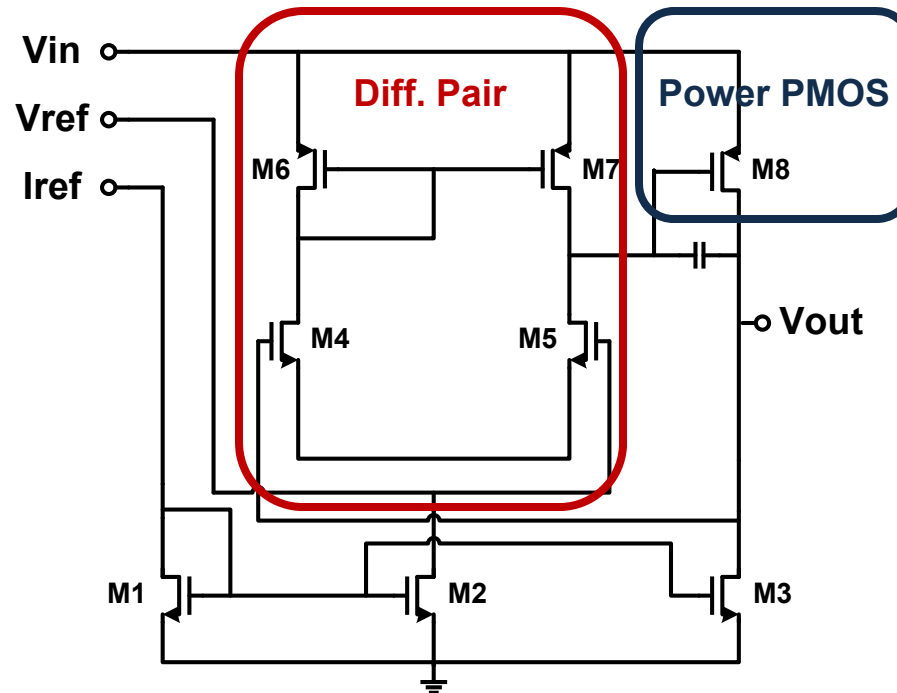


LDO Voltage Regulator Circuit Description

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Features

- To regulate voltage from solar cell and provide stable 1.2V supply voltage
- Low Drop-Out Design by using PMOS in output stage
- Unity gain feedback Amplifier in small signal aspect

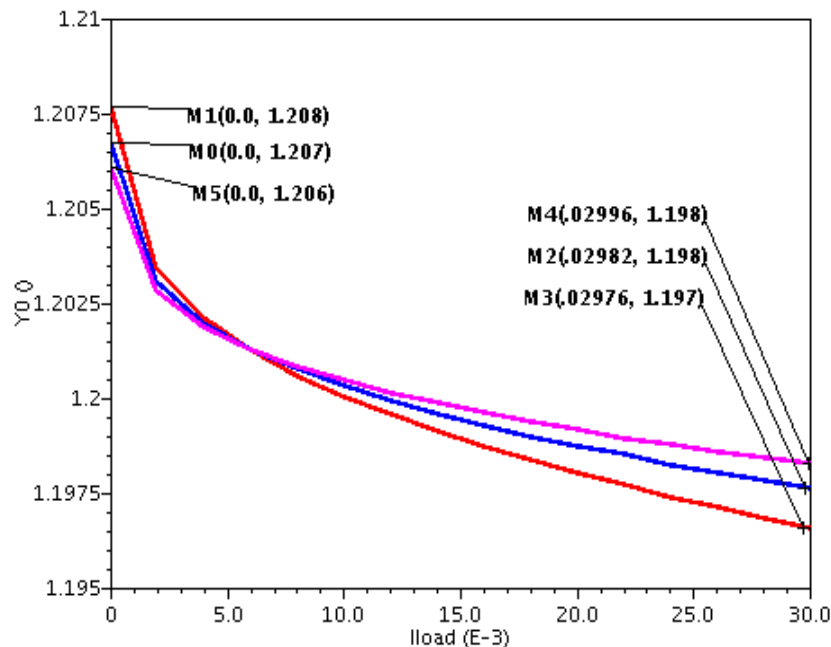


LDO Voltage Regulator Simulation Results

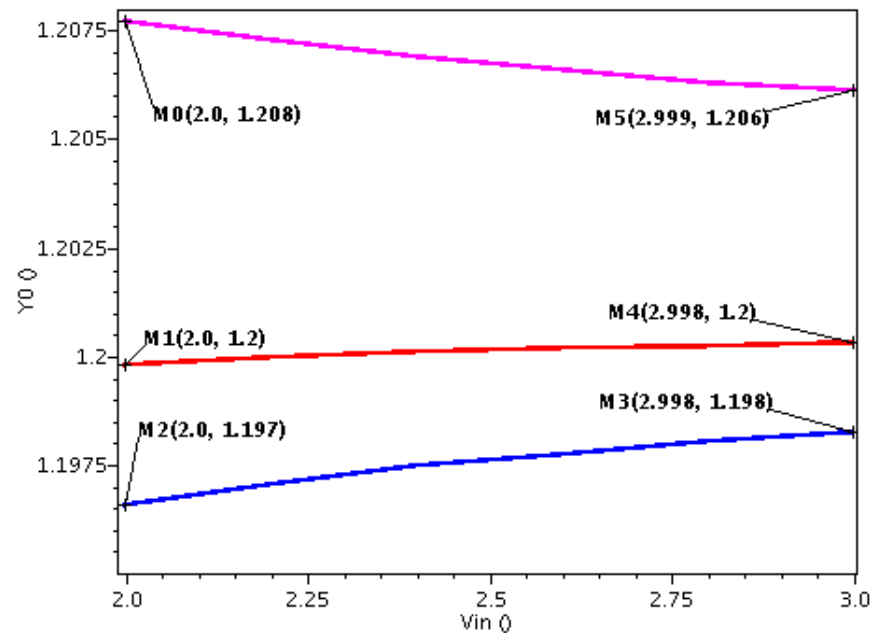
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Key performance

- $V_{in} = 2 \sim 3V$; $V_{out} = 1.2V$
- $I_{load} = 0 \sim 30mA$
- Load regulation = 0.304mV/mA
@ 2.5V nominal supply voltage



- Line regulation = 0.517mV/V
@ 11mA nominal load current

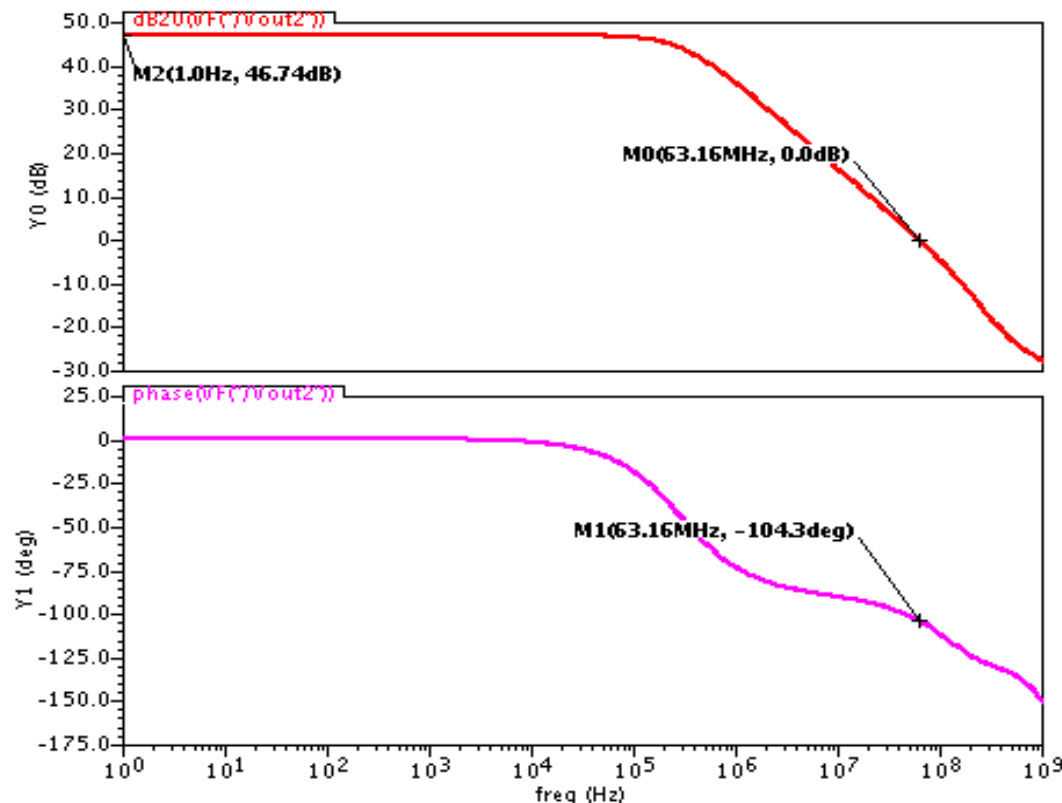


LDO Voltage Regulator Simulation Results

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Frequency response

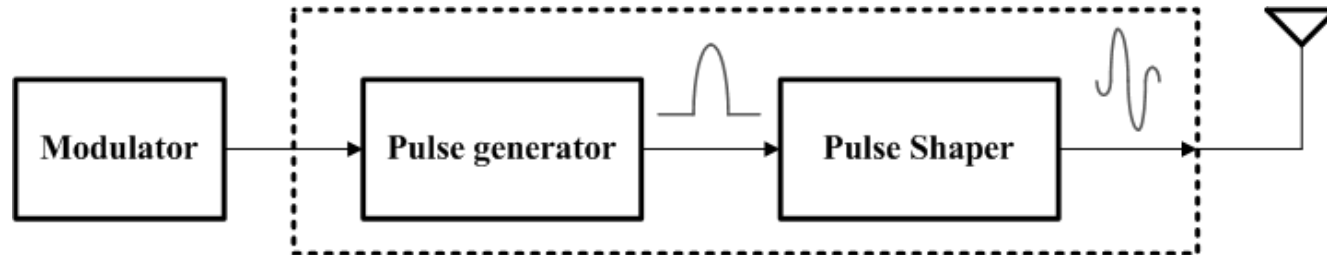
- Open loop gain= 46.74 dB
- Phase margin= 76°



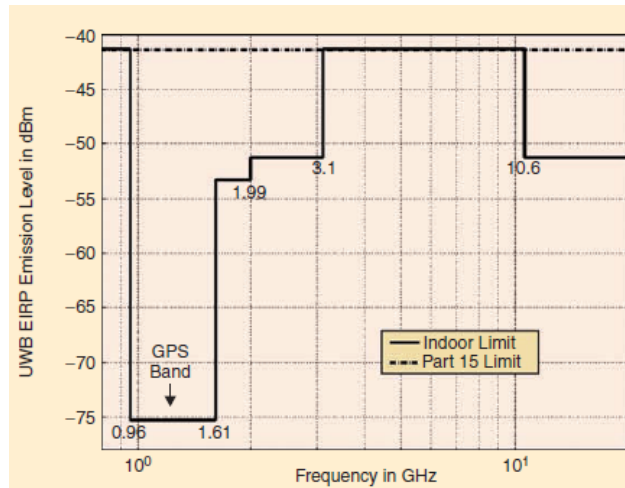
UWB Pulse Generator Circuit Description

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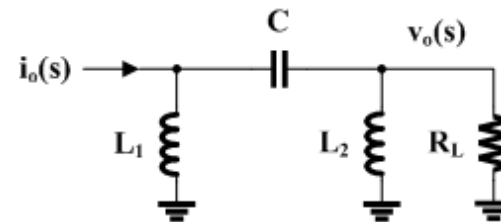
- UWB pulse-based transmitter system



- UWB spectral mask (defined by FCC)



- 3rd order Gaussian pulse shaping



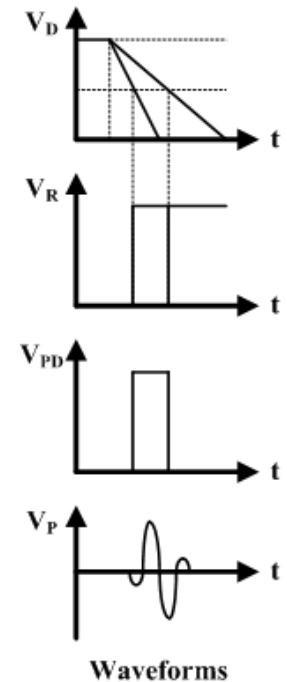
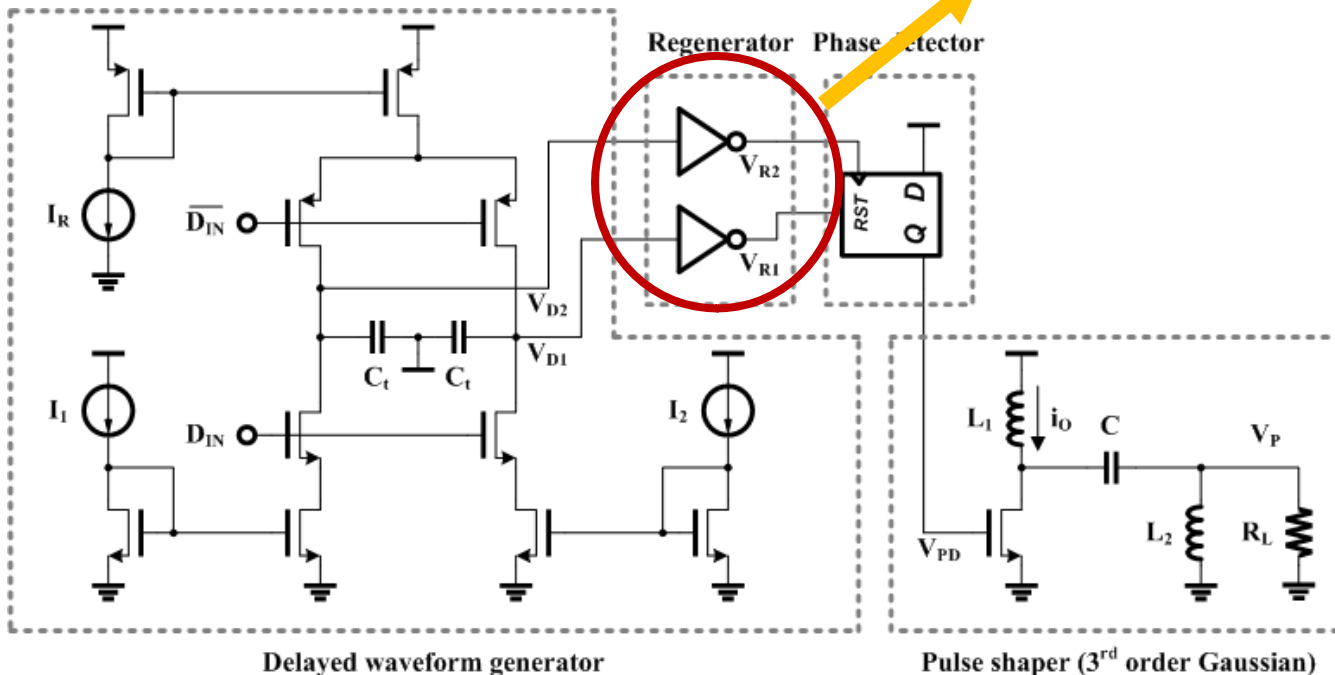
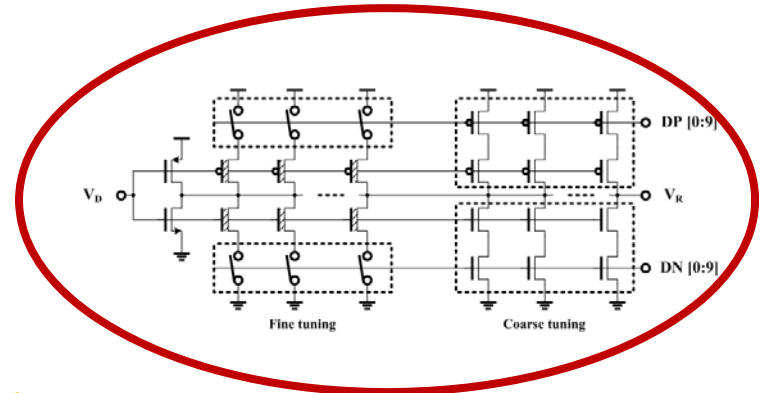
$$T(s) = \frac{v_o(s)}{i_o(s)} = \left\{ (R_L \parallel sL_2) + \frac{1}{sC} \right\} \parallel sL_1$$

$$= s^3(L_1L_2C)$$

UWB Pulse Generator Circuit Description

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- Delayed waveform generation
- Phase detection
- Pulse shaping



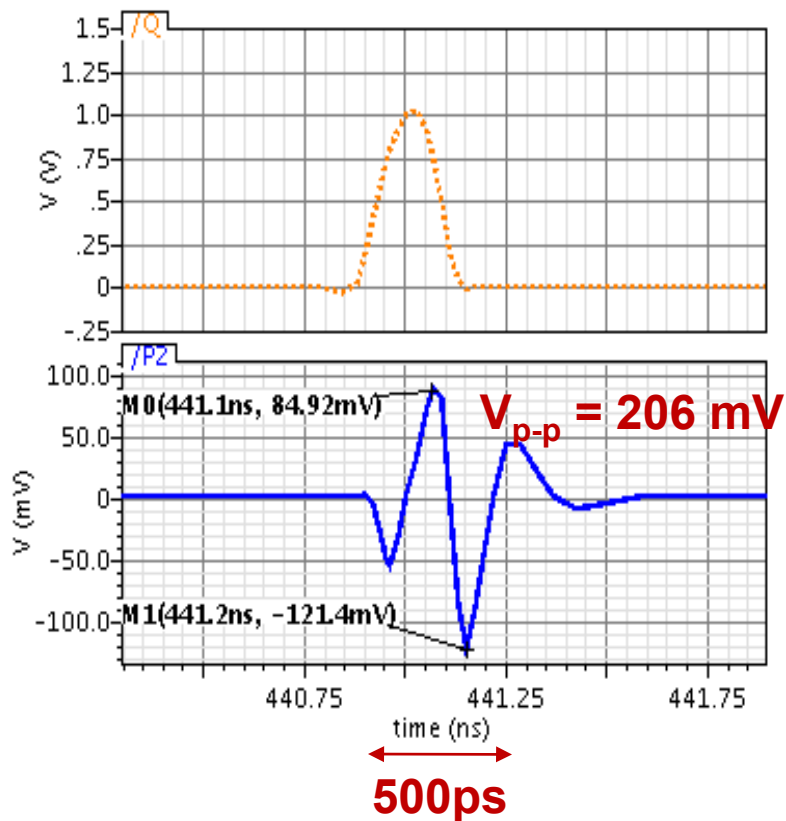
UWB Pulse Generator Simulation Results

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Key performance

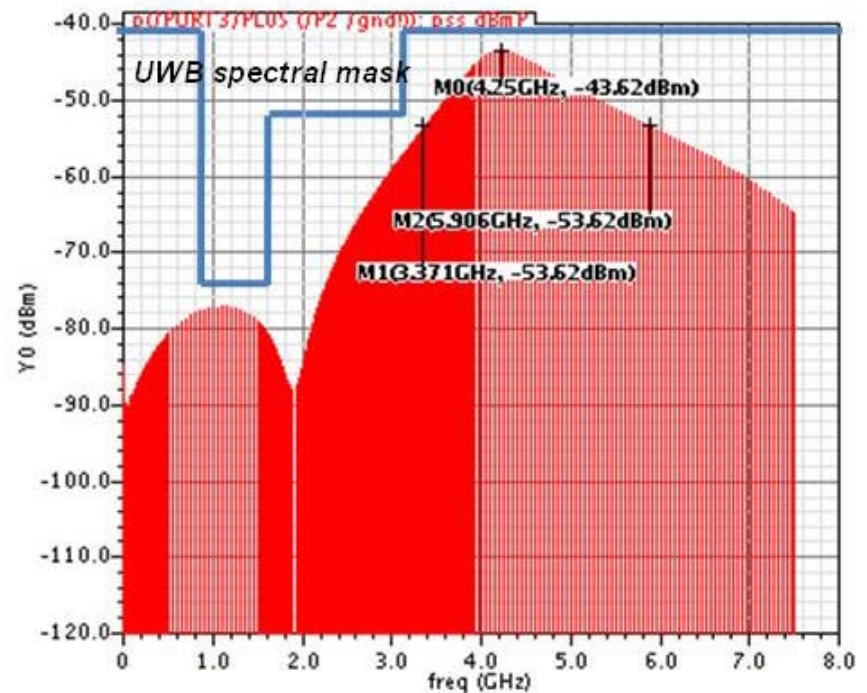
- Pulse output (transient)

$$V_{p-p} = 206 \text{ mV}$$

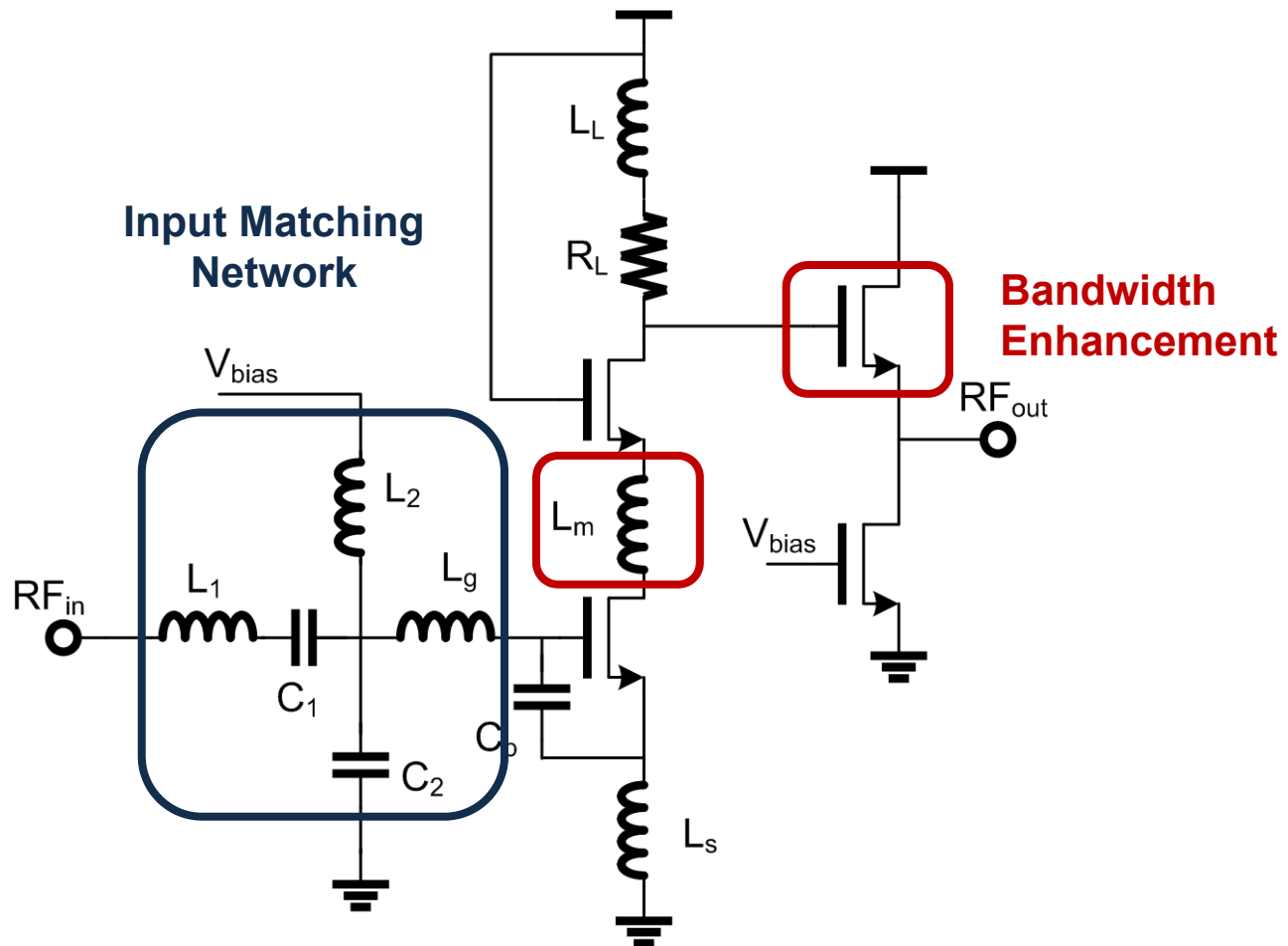


- Power spectral density

$$\text{Bandwidth (10dB)} = 3.37 \sim 5.9 \text{ GHz}$$

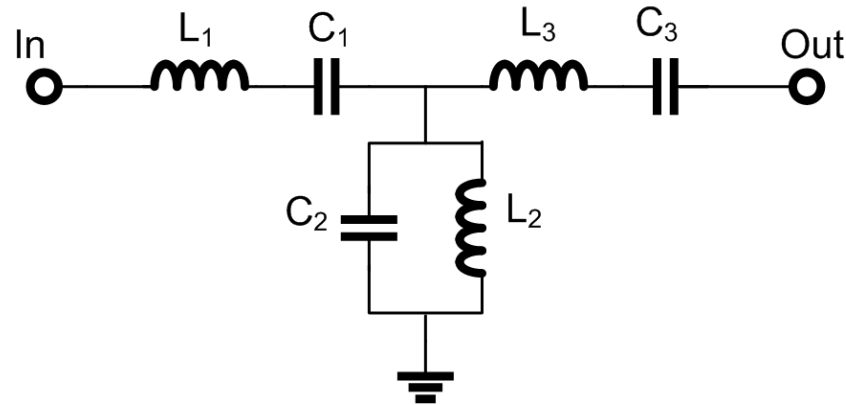


Proposed LNA architecture



Input matching

- 3rd order Chebyshev filter for broadband matching

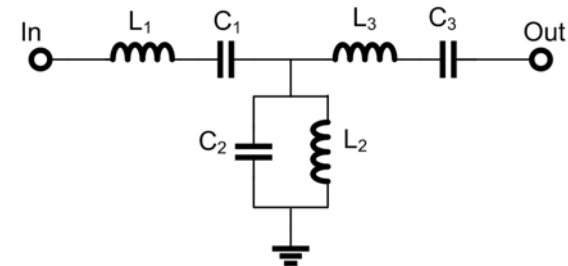


- For ground output

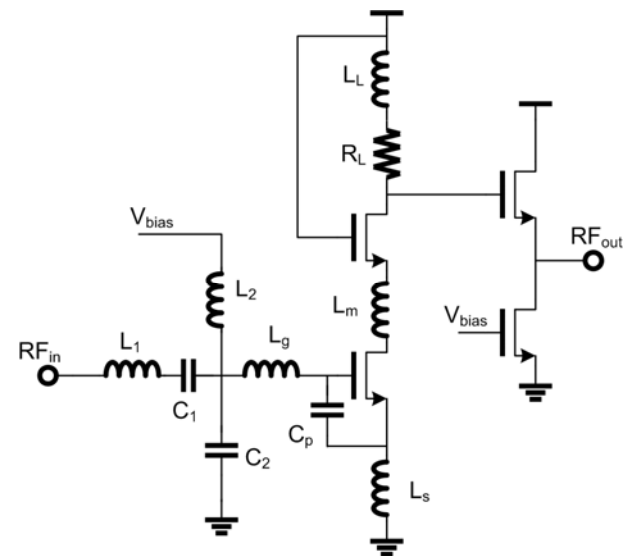
$$Z_{IN} = \frac{(s^2 LC + 1) \left[(s^2 LC + 1)^2 + s^2 LC \frac{C_1 + C_3}{C_2} \right]}{sC_1 \left[(s^2 LC + 1)^2 + s^2 LC \frac{C_3}{C_2} \right]}$$

Gain

- Tradeoff
 - Large $C_1 + C_3$: More matching bandwidth
 - Small C_3 : Less gain loss @ high frequency
- Bandwidth enhancement
 - L_m cancels inter-cascode node capacitance
 - Buffer reduces C_{out} of gain stage



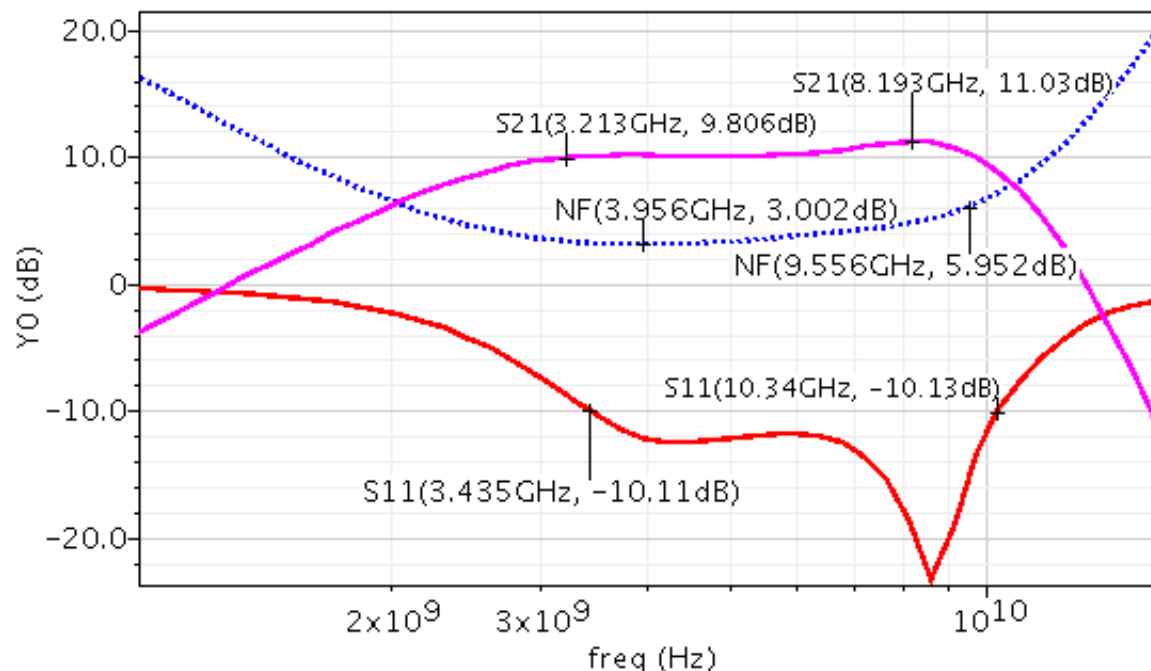
Chebyshev filter



Proposed LNA

Key performance

- $S_{21} > 9.8\text{dB}$ @ 3.5GHz ~ 9.7GHz
- $S_{11} < -10\text{dB}$ @ 3.4GHz ~ 10.3GHz
- 3dB Bandwidth @ 3.2GHz ~ 10.6GHz



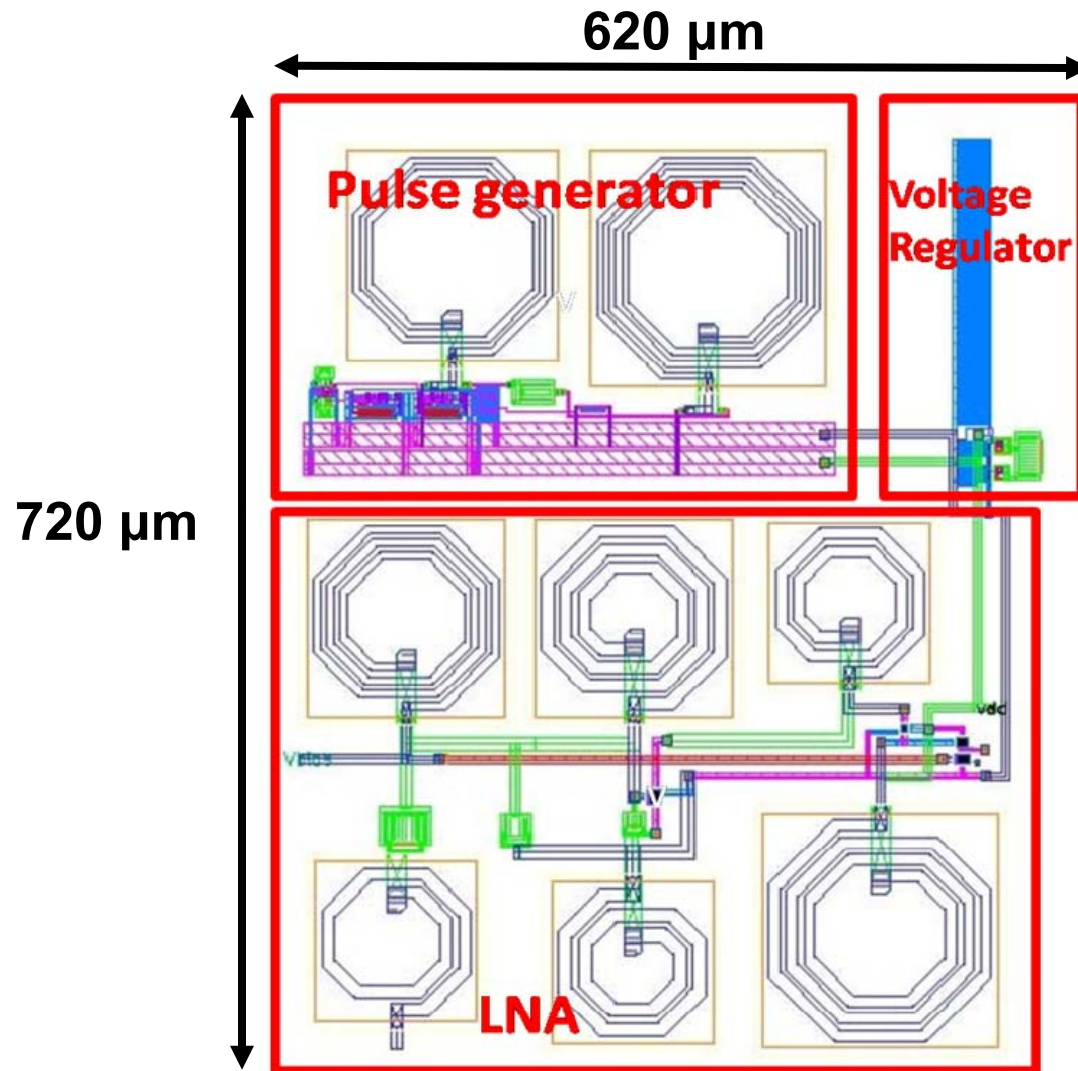
Summary of Specification Conclusion

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	Parameter	RESULTS
LDO Voltage Regulator	Line Regulation	0.517mV/V
	Load Regulation	0.304mV/mA
	Output voltage	300mV-1.2V
	Maximum Load current	30mA
	Power Consumption	1.22mW (No Load) 76.2mW (Full load)
Pulse Generator	Pulse amplitude	208 mV
	Pulse duration	500 ps
	Bandwidth (10 dB)	3.37 / 5.9 GHz
	Power Consumption	249.6 μ W
LNA	S_{11}	-10 dB (3.4-10.3GHz)
	S_{21}	9.8 dB (3.5-9.7GHz)
	3dB bandwidth	3.2-10.6GHz
	NF	< 6 dB (3.2-9.6GHz)
	Power Consumption	8.4 mW



Layout View Conclusion



THANK YOU !

