A Low Power Integrated UWB Transceiver with Solar Energy Harvesting for Wireless Image Sensor Networks

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***Abstract*— This paper presents the core 3 blocks of a Ultra –Wideband (UWB) transceiver with solar energy harvesting for wireless image sensor network. A Low Drop-out voltage (LDO) regulator regulates 2.5V±0.5V which is varied supply voltage from battery and solar cell to stable 1.2 V and supply 1.2V to a pulse generator and a Low Noise Amplifier (LNA). A pulse generator generates a 3rd order Gaussian pulse with > 200 mV amplitude, 500 ps duration. In 3.5-10GHz band, the LNA has NF < 6.5 dB, input matching S_{11} < -10 dB, and gain S21 > 9.3 dB.**

***Index Terms*—Low noise Amplifier (LNA), Pulse Generator, Low Drop-Out (LDO) voltage regulator, Ultra-Wideband (UWB)**

I. Introduction

Wireless image sensor networks (WISN) are expected to offer a vast variety of applications such as office environmental control, warehouse inventory, smart homes, interactive toys, and data collection. An integrated imager provides digital image signals (> 8 bit) of entire pixel array (> 1 Megapixels normally), which entails large bandwidth and power consumption for wireless data transmission.

Due to the large bandwidth and high data rate requirement, UWB transmission can be one of the best solutions for ISN. As shown in Fig.1, A UWB transceiver consists of a transmitter and a receiver. Another critical issue mentioned above is the large power consumption. In order to reduce power, generating short pulses at discrete time interval instead of continuous sinusoidal signals can reduce power consumption of data transmission. Furthermore, power harvesting by solar cell integrated to battery can enhance lifetime of the sensor node.

In this paper, an integrated UWB transceiver with solar energy harvesting applicable to WISN is proposed. The LDO voltage regulator which regulates the varied voltage from solar cell arrays and battery of 2.5V±0.5V provides the power supply of 1.2 V to the UWB pulse generator and LNA.

II. Circuit Description

A. Low Drop-Out Voltage Regulator

The supply voltage block of wireless image sensors in this paper includes solar cell for power harvesting purpose. Solar cell is greatly useful for power harvesting, but it can cause more fluctuation of supply voltage. Thus, voltage regulation is significantly needed to guarantee stable circuit operation.

We targeted less than 1mV/V line regulation and 1mV/mA load regulation with supply voltage of 2.5V. The voltage regulator consists of Op-Amp, Power PMOS in output stage.

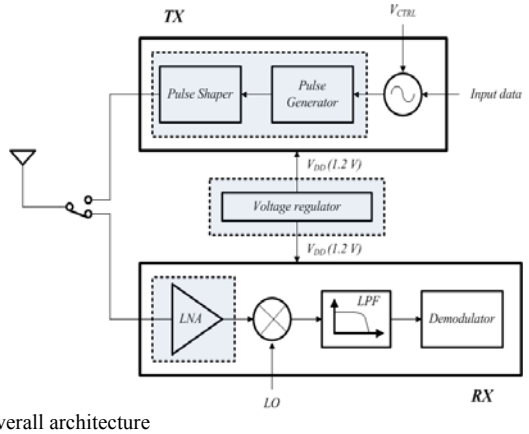

Fig.1. Overall architecture

1) Op-Amp Design

The operational amplifier is a single stage differential pair with current mirror load. The open loop gain of the amplifier along with the output stage is 46dB which is good enough to reduce the error by less than 1%.

Load regulation is equal to the output resistance of the regulator. The regulator yields better load regulation performance as the open-loop gain increases. However, the gain is limited by the closed-loop bandwidth of the system.

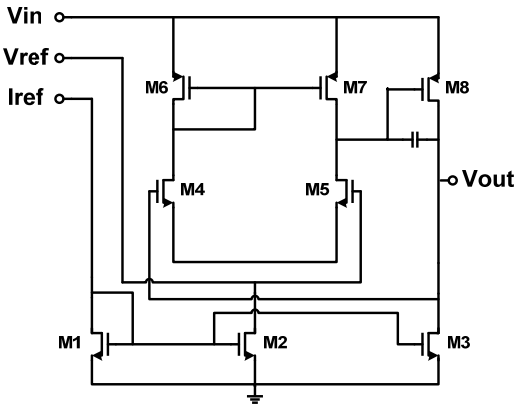

Fig.2 Schematic of Low drop out voltage regulator.

2) Power PMOS Design

One essential characteristic of this voltage regulator is to have a low drop-out voltage, because this voltage regulator is designed to work with supply voltage of 1.5V and to provide an output voltage of 1.2 V.

To minimize drop-out, a PMOS transistor is used, because it does not suffer from threshold voltage drop.

When sizing the power PMOS, in order to have large value of maximum load current and low drop out voltage, this requires the output PMOS device to be large which in turn

requires large quiescent current to reduce the output impedance of the amplifier node. In addition, change of load current from minimum to maximum value should not cause significant variation of gate voltage. If the gate voltage varies significantly, then either transistor M5 or M7 in Op-Amp can enter the triode region. From basic I-V equation of saturation region

$$\frac{W}{L} = \frac{30mA}{\frac{1}{2}\,\mu_p C_{ox}(V_{GS} - V_{th})^2} = 16283$$

With this ratio, W= 3.9mm, L=240nm. By simulation around calculation results, we get the value of W=4mm, L= 240nm.

B. Pulse generator

Fig.3 shows the circuit schematic of the pulse generator. It consists of the delayed waveform generator, regenerator, phase detector and pulse shaper. In the delayed waveform generator, two capacitors with same capacitance are initially charged and are discharged by two DC currents I1 and I2 which have different magnitude. Then delayed waveforms are generated according to the following relationship.

$$\Delta t = t_1 - t_2 = \frac{C\Delta V}{I_1} - \frac{C\Delta V}{I_2} = C\Delta V\left(\frac{1}{I_1} - \frac{1}{I_2}\right)$$

A regenerator regenerates delayed waveforms. Since the trip voltage has severe effect on the pulse width, tunable inverter is used as the regenerator as shown in Fig. y. It provides fine tuning (minimum 1mV) as well as the coarse tuning. Fine tuner consists of minimum size driving transistor with high resistance switches (with various L) in order to change the trip voltage slightly. Switches are controlled by digital signals D and P externally. A phase detector outputs the short pulse which has the duty cycle as much as the phase difference (i.e., delay) of regenerated waveforms. In order to meet the FCC spectral mask specification, a pulse shaper should be included. The pulse shaper provides 3rd order Gaussian pulse while driving the 50-ohm antenna. The transfer function of the pulse shaper is shown as follows:

$$T(s) = \frac{v_O(s)}{i_O(s)} = \left\{(R_L||sL_2) + \frac{1}{sC}\right\}||sL_1$$

$$\cong \frac{(RL_1L_2)s^2}{\frac{R}{sC} + \frac{L_2}{C}} = \frac{(RL_1L_2C)s^3}{R + sL_2}$$

C. Wideband LNA

The schematic of the implemented LNA is shown in Fig. 5. The main challenge of designing a wideband LNA is maintaining the input matching and constant gain throughout the whole bandwidth. For input matching, 3rd order Chebyshev filter is used to achieve the broadband matching [1]. The impedance of the LC ladder is described as

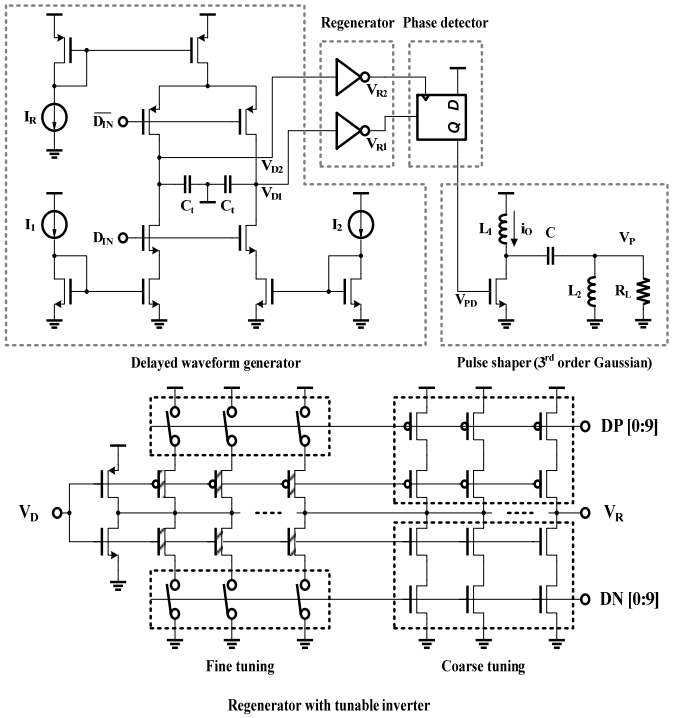

Fig.3. Circuit schematic of pulse generator

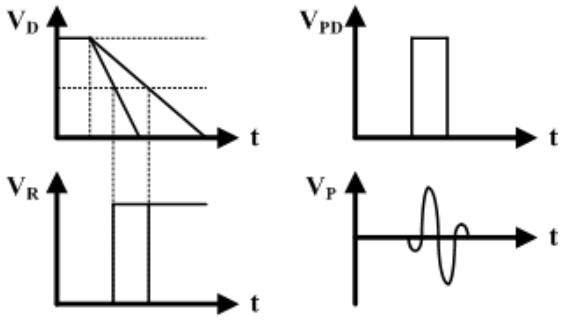

Fig.4. Waveform

$$Z_{LC} = \frac{\left(s^2LC + 1\right)\left[\left(s^2LC + 1\right)^2 + s^2LC\,\frac{C_1 + C_3}{C_2}\right]}{sC_1\left[\left(s^2LC + 1\right)^2 + s^2LC\,\frac{C_3}{C_2}\right]}$$

where LC is defined by center frequency. By increasing the capacitor ratio, the bandwidth of matching can be raised. As for gain, attenuation at high frequency because of the smaller V_{gs} due to lower impedance from C_{gs}(or C_3) becomes a critical issue. It can be alleviated by reducing the capacitance of C_3 (or C_{gs}//C_p), but this trades off against the matching network which needs larger $(C_1+C_3)/C_2$ to gain more bandwidth. As an alternative, adding an extra inductor L_m between cascode FETs increases the bandwidth of the amplifier stage [2]. After cancelling out the cascode node capacitance, a buffer stage, which reduces the capacitance at the output of gain stage, is also used to pull up the high frequency gain.

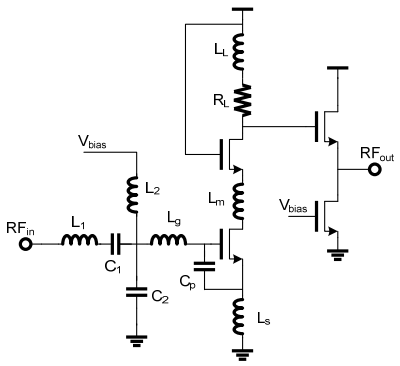

Fig.5. LNA schematic

III. RESULTS

A. *Low Drop-Out Voltage Regulator*

A load regulation is the change in the regulated output voltage with respect to a change in the load current. With output current range of 0-30mA, 0.011 mV/mA of load regulation was achieved.

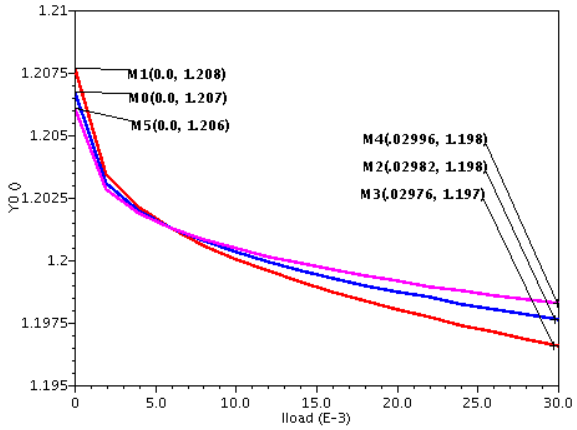

Fig.6. Simulated load regulation over an output current range of 30mA, showing a change in output voltage of only 1.1 mV.

The line regulation is the change in the regulated output voltage with respect to a change in the supply voltage.. To test this condition, we swept supply voltage around ±15% of its nominal value and measured the change in the output voltage. Fig. 5 shows 0.833 mV/V of line regulation.

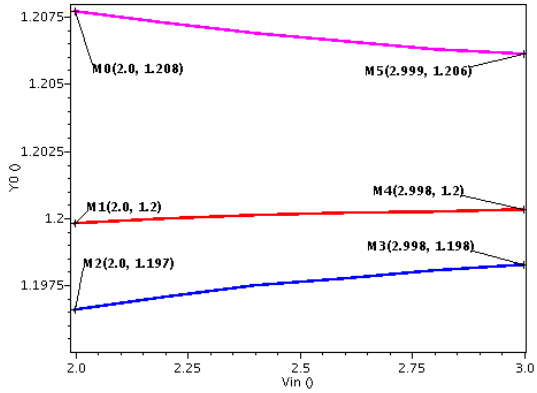

Fig.7. Simulated line regulation over a supply voltage variation of ±20% from nominal value, showing a change in output voltage of 0.1 mV.

For stability measurement, we measured the loop gain to find the unity-gain frequency and determine the phase margin of the regulator from a plot of the phase. Fig. 6 shows a phase margin of 80°.

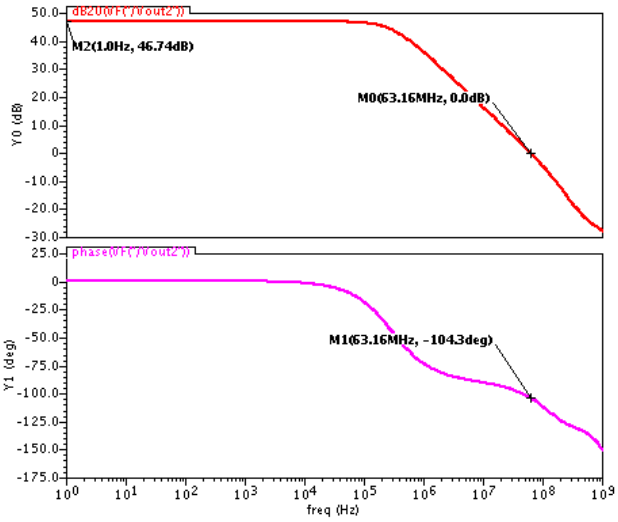

Fig.8. Open Loop Gain and Phase plot

B. *Pulse generator*

The pulse output with the waveforms are shown in Fig.9. The peak-to-peak voltage of the pulse is 208 mV, the pulse width is 150 ps. In Fig. 10, output power spectral density (in dBm) is shown. The peak point (@ 4.25 GHz) is under -41.4 dBm which satisfies the FCC mask requirement. The 10dB bandwidth is measured as 2.317 GHz. The power consumption is 249.6 uW (@ 25MHz). The simulation results are summarized in Table I.

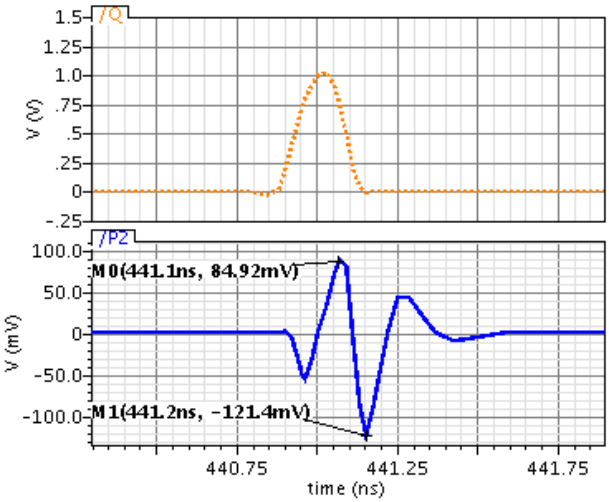

Fig. 9. Pulse waveform

C. *Wideband LNA*

For LNA, as shown in Fig.11., S_{11} is achieved to less than -10 dB in the frequency range of 3.5-10.1GHz. NF is less than 6 dB from 3.5GHz to 9.5GHz with the minimum of 3 dB. As for the gain S_{21}, it is larger than 9.8 dB within the 3.2-9.7GHz range and reaches its maximum of 11 dB at 8.2GHz.

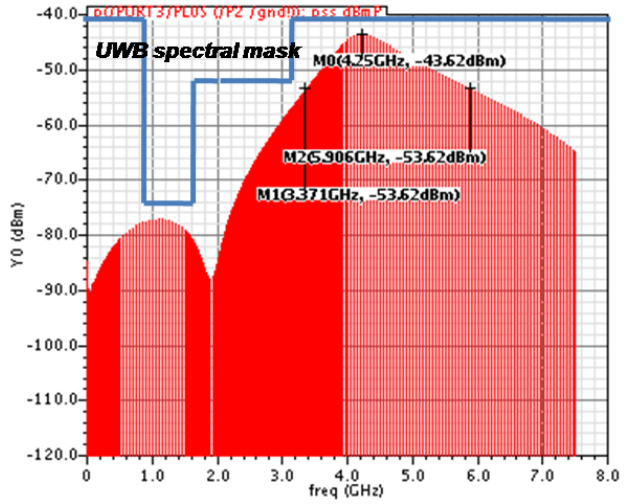

Fig. 10. Power Spectral Density

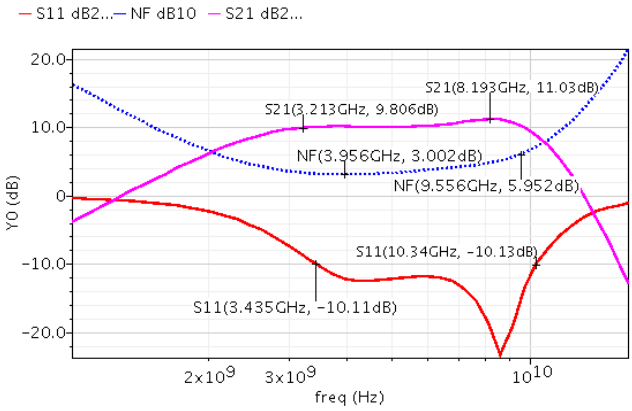

Fig. 11. LNA simulation result: NF, S11, S21

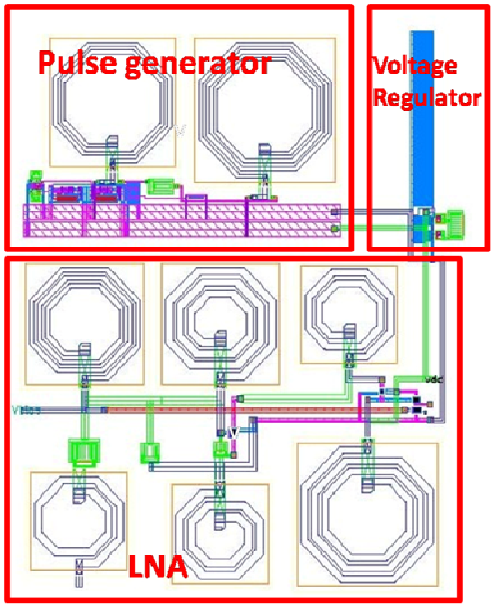

Fig12. Layout view

TABLE I
SPECIFICATION SUMMARY

	Parameter	Results
LDO Voltage Regulator	Line Regulation	0.517mV/V
	Load Regulation	0.304mV/mA
	Output voltage	300mV-1.2V
	Maximum Load current	30mA
	Phase Margin	76°
	Power Consumption	1.22mW (No Load) 76.2mW (Full load)
	Current Efficiency	98.4%
	Layout Area	164 x 97 um^2
Pulse Generator	Pulse amplitude	208 mV
	Pulse duration	500 ps
	Bandwidth (10 dB)	3.37 / 5.9 GHz
	Power Consumption	249.6 µW
	Layout Area	420 x 270 um^2
LNA	S_{11}	-10 dB(3.4-10.3GHz)
	S_{21}	9.8 dB(3.5-9.7GHz)
	3dB bandwidth	3.2-10.6GHz
	NF	< 6 dB(3.2-9.6GHz)
	P_{1dB}	-21dBm
	IIP_3	-8dBm
	Power Consumption	8.4 mW
	Layout Area	590 x 450 um^2

IV. CONCLUSION

In this project, we designed a UWB transceiver for wireless image sensor network. An integrated regulator which interfaces with the solar cell drives the transceiver by providing 1.2 V power supply with > 30 mA load current capacity. A pulse generator generates a 3rd order Gaussian pulse with > 200 mV amplitude, 500 ps duration. In the receiver block, we designed LNA which has 9.8 dB gain for 3.2 to 10 GHz UWB bandwidth. The overall power consumption of the three designed blocks is 27 mW and total area is 0.47 mm^2.

V. REFERENCES

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