A Dual-Band CMOS Receiver for IEEE 802.11n Wireless LAN

Victor C. Lee, Seyit A. Sis, Xiao Zhu

***Abstract* — In this paper, the design of the front end of a concurrent dual-band receiver is presented. The receiver has center frequencies of 2.44 GHz and 5.25 GHz and consists of a dual-band low noise amplifier (LNA), a dual-band mixer, and a quadrature voltage controlled oscillator (QVCO). The architecture for the receiver is designed for image frequency rejection.**

Index Terms — Dual-band, IEEE 802.11n, low noise amplifier (LNA), mixer, quadrature voltage controlled oscillator (QVCO), RF receiver, wireless local area network (WLAN)

I. Introduction

ONE of the most widely used wireless communication standards is the IEEE 802.11 wireless local area network (WLAN) standard. WLAN access points are commonly found in the business as well as home environment. As their popularity increases due to the increase in the number of WLAN capable devices, user capacity and communication bandwidth become a concern.

IEEE 802.11 is an actively evolving standard that involves the collaboration of many different entities which work together to overcome arising problems in the wireless communication protocol. IEEE 802.11n is the next amendment to be ratified. It includes changes in the communication protocol which drastically increase maximum theoretical communication bandwidth to 600 Mbps as well as increase communication range, reliability, and number of simultaneous clients [1]. The demand to achieve higher bandwidth in wireless communication is so great that even before the 802.11n amendment gets ratified, manufacturers are already selling them to eager consumers. Analyst firm ABI Research forecasts that 802.11n chipset shipments in the 802.11n chipset will increase from 93 million units in 2007 to about 1.1 billion units in 2012, dominating overall Wi-Fi shipments of 1.2 billion units [2].

The drastic increase in the wireless communication protocol comes from many different factors. One reason for the increase in maximum throughput is because the channel bandwidth has been increased from 20 MHz to 40 MHz. The new protocol connects more simultaneous users because it utilizes the 5 GHz industrial, scientific, and medical (ISM) radio band in addition to the 2.4 GHz ISM band, which is being used for the latest ratified protocol. The addition of the 5 GHz band is one of the drastic changes to the protocol and requires new hardware to implement it. However, much works needs to be done in simultaneous dual-band wireless communication.

In this paper, we report the design and simulation results of a concurrent dual-band receiver system for application in the IEEE 802.11n communication protocol which can simultaneously receive 2.4 GHz and 5 GHz transmissions.

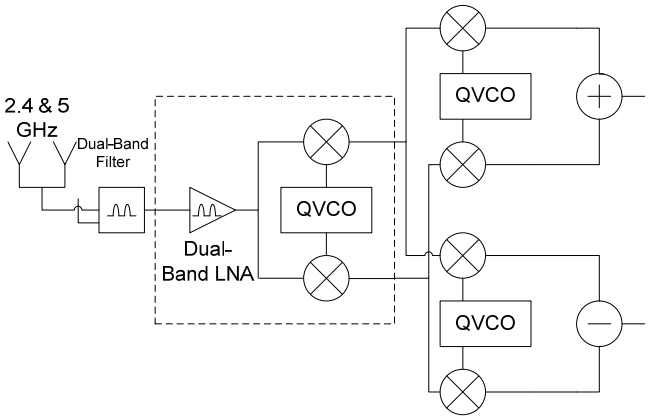

Fig. 1: Receiver architecture.

II. System Level Design

A. Overview

The entire receiver architecture is shown in Fig. 1. Only the components of the front-end of the total receiver are designed in this project. The total receiver is concurrent and dual-band. It is primarily designed for the IEEE 802.11n wireless communication standard.

As indicated in Fig. 1, a dual-band LNA, a mixer and a QVCO are designed in this project. A dual-band antenna, dual-band filter and a dual-band balun is assumed to be available as off-chip components for the receiver. This architecture provides good image rejection compared to the single band and other dual band architectures [3]. The local oscillator frequency is chosen such that image frequencies of both low and high bands are in the high attenuation region of the frequency response of the front end components. Therefore, the antenna, off-chip filter and LNA's frequency responses should be consistent with the frequency plan of the receiver for best image rejection. In Fig. 2, f_{LO} is local oscillator frequency, f_{ImB} is image frequency of 5 GHz band and $f_{Im,low}$ is the image frequency of 2.4 GHz band. The frequency plan for this project is given in Table I.

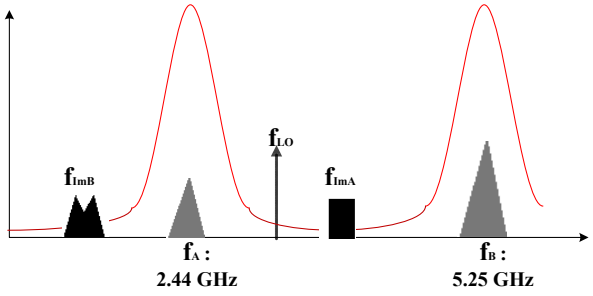

Fig. 2: Receiver frequency plan.

TABLE I
FREQUENCY PLAN

Specification	Value	
Lower Band	2.44	GHz
Upper Band	5.25	GHz
f_{LO}	3.14	GHz
$f_{Im\ high}$	1.037	GHz
$f_{Im,low}$	3.83	GHz
IF_1	0.702	GHz
IF_2	2.106	GHz

B. LNA Design

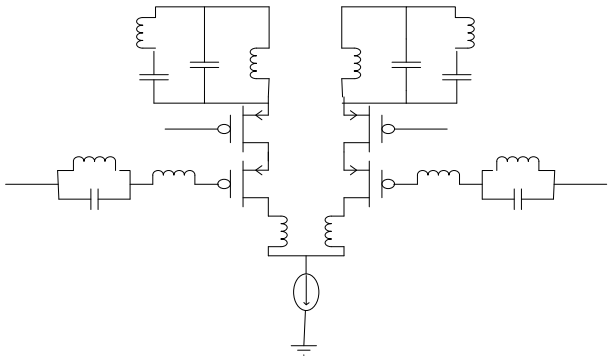

Fig. 3: Dual-band differential LNA schematics.

In LNA design, trade-offs must be made between gain, noise figure and power consumption. WLAN 802.11 a/b/g/n concurrent dual band wireless receivers require enough gain at both bands with low or moderate power consumption. An important property of dual band LNA is that the transistor's transconductance can still be enough to give sufficient gain at both bands without any power consumption penalty [4]

The LNA designed in this project is optimized for high gain efficiency. A differential architecture is chosen, as for the whole front-end, for common mode noise rejection and good linearity. But, differential circuits require twice area and power consumption while increasing the output power or 1 dB compression point. The bias circuit is designed by using a current mirror. A cascode structure is chosen for better input-output isolation. It is basically due to the gain reduction in the first transistor, which then decreases the effect of C_{gd} at the input.

The transistor is optimized for maximum $g_m * f_t$ for a fixed power consumption (drain current, I_d). At this point, maximum gain efficiency is obtained. Long channel DC current-voltage relations can be used to understand g_m and I_d variation as a function of the transistor width, W.

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 \quad (1)$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th}) \quad (2)$$

As g_m increases for a fixed I_d, W increases and the overdrive voltage (V_{gs}-V_{th}) decreases, but with different ratios. Due to the decrease in V_{gs}, transistor gets into weak inversion and subthreshold region. But, f_t of the transistor decreases as W increases, so $g_m * f_t$ is a good figure of merit for a fixed current.

Input matching network is designed to resonate at both bands for 50 Ω input impedance [5]. Fig. 4 shows the input matching circuit of the LNA. There are two extra components in dual-band LNA's input compared to single band LNA. These two extra components form a parallel resonance series to L_g, L_s and C_{gs}. At the resonance frequency, this tank is open and provides a notch at the gain of the LNA.

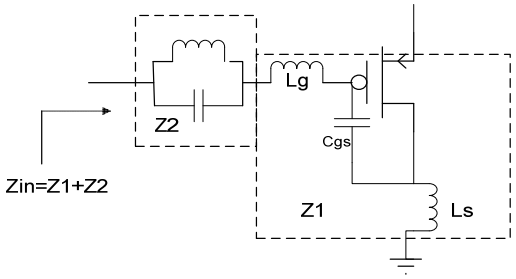

Fig. 4: Input matching circuit of the LNA.

Input matching is divided into two parts as shown in Fig. 4. Z_1 provides notch at its resonance frequency. To match input to 50 Ω, following equation should be satisfied.

$$\begin{matrix}\mathrm{Im}(Z_1(\omega_1)+Z_2(\omega_1)) \\ \mathrm{Im}(Z_1(\omega_2)+Z_2(\omega_2))\end{matrix} \quad (3)$$

$$\frac{g_m \cdot L}{C_{gs}} = 50\Omega \quad (4)$$

Output resonator circuit is designed in the same way except parallel resonance circuits are used to match (see Fig. 3).

C. Mixer Design

The mixers used in the WLAN receiver are double balanced active mixer with differential RF and differential LO inputs. Since both LO and RF are balanced, the mixer provides both LO and RF rejection at the IF outputs [6].

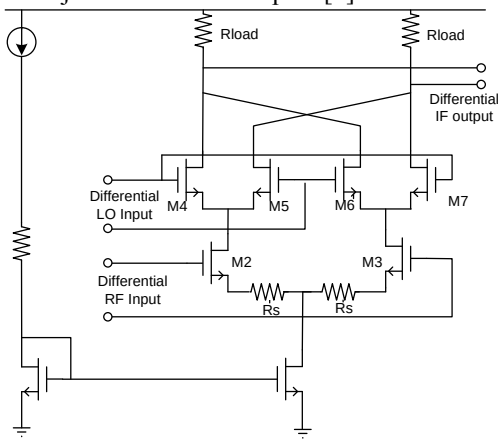

Fig. 5. Mixer Architecture

The symmetry removes the unwanted RF and LO output signals from the IF by cancellation. Linearity is also increased compared to single balanced mixer. Other advantages of the double balanced Gilbert mixer include good ports isolation from each other, improved suppression of spurious products and higher IIP3 as well as decreased susceptibility to supply voltage.

The design challenges of double Gilbert mixer are requirement of higher LO drive level and sensitivity of ports to reactive terminations. The voltage overdrive level (Vgs-Vth) should be set at around 0.2 to 0.4V. Also, double mixer generally does not achieve high gain, so it's challenging to get both high gain and good linearity performance.

The important performance parameters of typical down conversion mixers include the noise figure, the conversion gain, the 3rd order intercept point and the port-to-port isolation. The noise figure is important in mixers as it is a measure of the performance of the mixer. The 3rd order intercept point is critical as it is a measure for the linearity of the mixer.

A high conversion gain reduces the requirements an extra buffer at the mixer output. The conversion gain of a double balanced mixer is given by

$$G_C = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_{m2} R_{load}$$

In which, the g_m given by

$$g_{m2} = \sqrt{\frac{2\mu_n C_{ox} W}{L} I_D}$$

The LO-RF feedthrough results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feedthrough allows strong interferers in the RF path to interact with the local oscillator driving the mixer. In the differential Gilbert mixer, LO-IF feedthrough will be cancelled completely in the ideal case. However, if mismatch is considered, the LO-IF still exists but is minimized.

Performance can be improved by adding degeneration resistors, on the source terminals of M2 & M3. A modified mixer architecture with source degeneration (Rs) is added for improving the linearity . And the conversion gain of the modified mixer is

$$G_C^{'} = \frac{2}{\pi} \frac{R_{load}}{R_S + 1/g_{m2}}$$

This equation highlights the importance g_{m2} of M_2 plays in the conversion gain of the mixer. The RF signal is applied to the transistors M2 & M3 which perform a voltage to current conversion. For correct operation these devices are generally not driven into saturation. The first version of schematics gets low gain since it's hard to get enough overdrive under 1.2 voltage supply. By increasing the size of M2 and M3, good performance with higher conversion gain is achieved. In consideration of power consumption, the biased current need to carefully be designed to provide an optimum balance of conversion gain. Different architectures of biased circuits to LO and RF are tested to get both a stable reference with less variation and less power consumption. The bias reference circuits are needed to offer common mode voltage to LO&RF input transistor and also a bias current source in the mixer.

The current to voltage transformation giving differential output IF signals is performed by the load resistors on the top. Transistors M4 to M7 form a multiplication function, multiplying the linear RF signal current from M2 and M3 with the LO signal applied across M4 to M7 which provide the switching function. Also, to increase the conversion gain, the input impedance in heterodyne architectures should be well matched.

D. QVCO Design

A QVCO using super-harmonic coupling is designed to oscillate at 3.143 GHz. The schematic of the design is from [5] and is shown in Fig. 6.

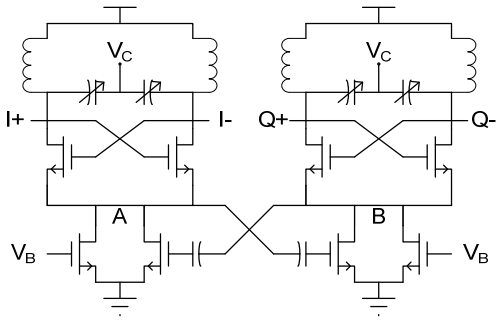

Fig. 6: QVCO schematic.

A super-harmonic coupled QVCO is designed to oscillate at the LO frequency of 3.143 GHz. The schematic of the design is shown in Fig. 6. The circuit works by coupling the energy of the oscillators such that the relative phase at which they oscillate is locked. First, a resonator which operates at the desire frequency is designed. This frequency is determined by the parallel inductor-varactor tank. Then, two instances of the oscillator are coupled together as shown in Fig. 6. When the QVCO begins to oscillate, each of the oscillators behaves independently of one another. However, as the amplitude of the output grows, the current begins to completely steer towards just one of the two cross-coupled transistors. This see-saw action causes the cross-coupled transistors to pull up the voltage at nodes A and B as indicated in Fig. 6. While the current of oscillator is switching sides, the bias current transistor is able to pull down on the node voltage. However, if the cross-coupled transistors are sized much larger than the current source transistor, the signal at the node appears to be oscillating at twice the fundamental frequency of the single oscillator. This oscillation gets fed into the gate of the bias current transistor of the other oscillator. If the oscillators are oscillating either in phase of 180º out of phase, contention develops at both nodes. In order to avoid this condition, the oscillators must oscillate 90º out-of-phase with respect to one another.

In the design of the QVCO, there are many parameters to consider. For example, consider the spiral inductor. Since the inductor has the most lost out of all the components, the quality factor needs to be maximized. In addition, the inductance of the inductor should also be maximized to increase the output voltage swing [6]. Other considerations that must be taken into account when designing each component are the tunability of the oscillator, power, output voltage amplitude, phase noise, and phase stability [7]. The characteristics of the designed oscillator for the dual-band receiver are listed in Table V. The output waveform is shown in Fig. 12.

III. Circuit Simulations

A. LNA simulation results

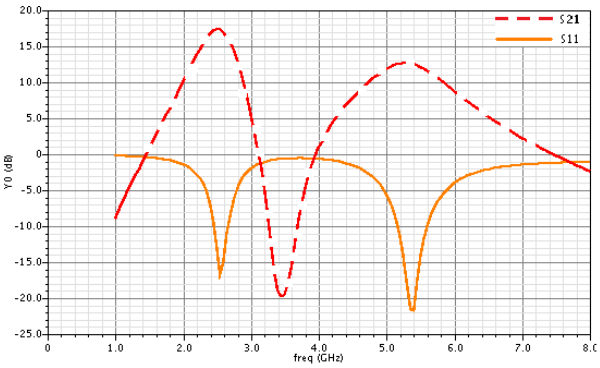

Fig. 7: Gain and input return loss of the LNA vs frequency.

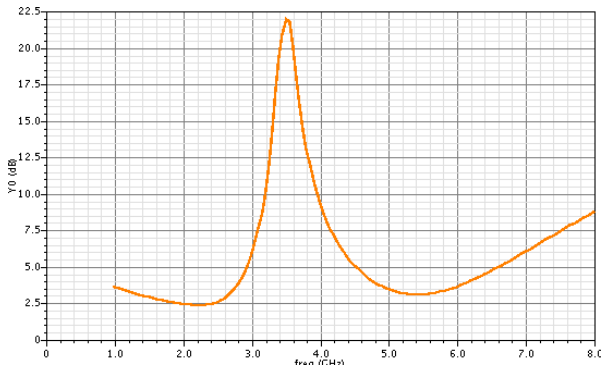

Fig. 8: Noise figure of the LNA vs frequency.

B. Mixer simulation results

Mixer simulations were performed following a SpectreRF application note. Conversion Gain Total harmonic distortion is from PSS simulations. Results in Fig. 9 are from a PNOISE simulation performed with the RF port set to DC 0 harmonics in the PSS simulation. IIP3 and the 1dB compression point were simulated using QPSS and QPAC simulations with a large signal LO and medium signal RF.

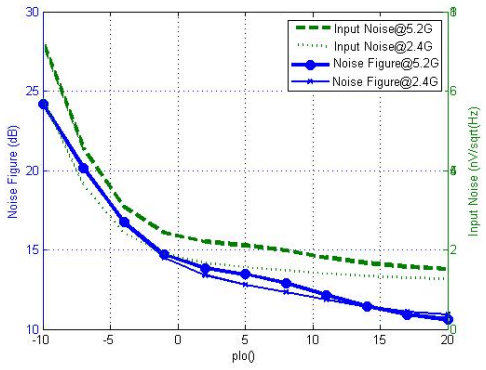

Fig. 9: Noise figure (dB) and input referred noise of the mixer vs plo, indicating very good noise performance.

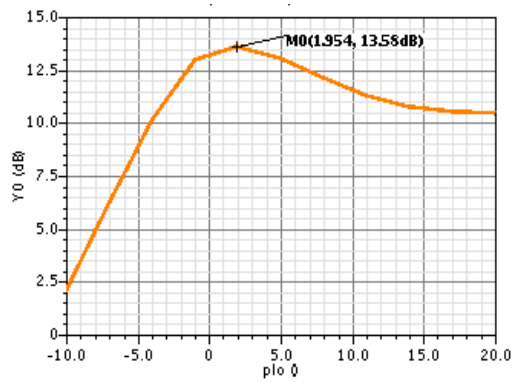

Fig. 10: Conversion Gain vs plo.

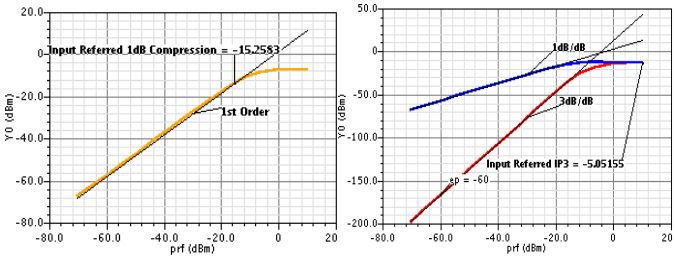

Fig. 11: 1dB Compression point and IIP3 vs prf, demonstrating good linear operation in the mixer.

C. QVCO simulation results

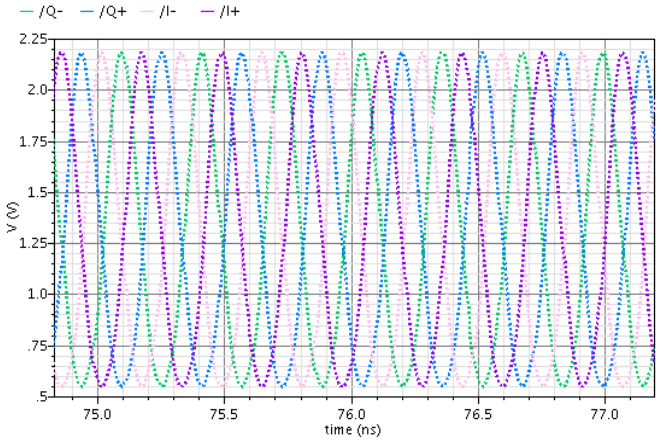

Fig. 12. Output waveform of the QVCO.

IV. Summary of Results

TABLE II
Overall Performance

Parameters	2.4 GHz	5.2 GHz
Frequency Band	2.4 - 2.4835 GHz	5.15 – 5.35 GHz
Gain (dB)	26.1	31.91
Quiescent Power (mW)	17.44	17.44

TABLE III
LNA PERFORMANCE

LNA Parameters	2.4 GHz	5.2 GHz
Gain (dB)	17.3	13
NF (dB)	2.5	3
S_{11} (dB)	<-9	<-11
IIP3(dBm)	-6	-3
IP1dB (dBm)	-13.5	-12.9
Quiescent Power (mW)	10.1	10.1

TABLE IV
MIXER PERFORMANCE

Mixer Parameters	
Gain (dB)	13.59
Quiescent Power (mW)	2.40
THD (dB)	-62.17
SSB NF (dB)	10.70
Input Ref Noise(nV/√Hz)	2.43
Isolation RF to IF (dB)	91.80
Isolation RF to LO (dB)	100.0
Isolation LO to RF (dB)	87.70
Isolation LO to IF (dB)	91.90
IIP3(dBm)	-5.89
P1dB (dBm)	-15.95

TABLE V
QVCO PERFORMANCE

QVCO Parameter	
Supply Voltage (V)	1.2
Frequency (GHz)	3.143
Output Amplitude (V)	1.409
Power Dissipation (mW)	4.94
Phase Noise (dBc/Hz @ 1 MHz)	105.37
Tuning Ratio (%)	> 16

V. CONCLUSION

In this paper, the front-end of a concurrent dual-band WLAN receiver is presented. Concurrent dual-band transceivers have advantages over traditional dual-band transceivers in characteristics such as area and power consumption. The designed front-end has a power consumption of 17.44 mW and an area of 2200x1300 μm^2.

APPENDIX

The path of the design and simulation files is: /afs/umich.edu/class/eecs522/w09/students/xiaozhu/CAD/receiver_Apr10/receiver_10.

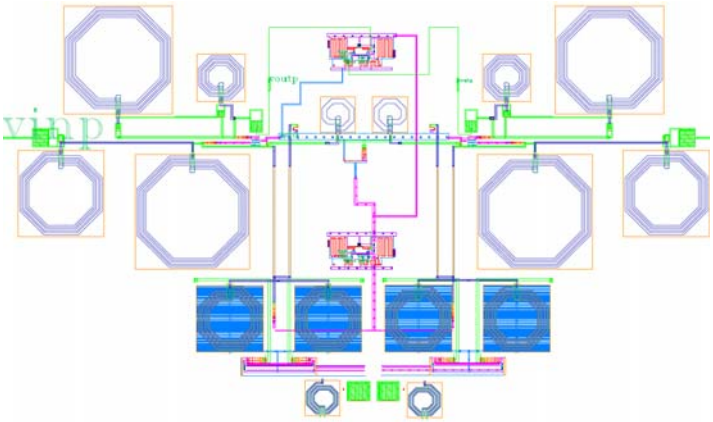

Fig. 12: The layout of the concurrent dual-band receiver with an area of 2200x1300 μm^2.

ACKNOWLEDGMENT

Our group would like to thank Professor Wentzloff for his assistance with this project.

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