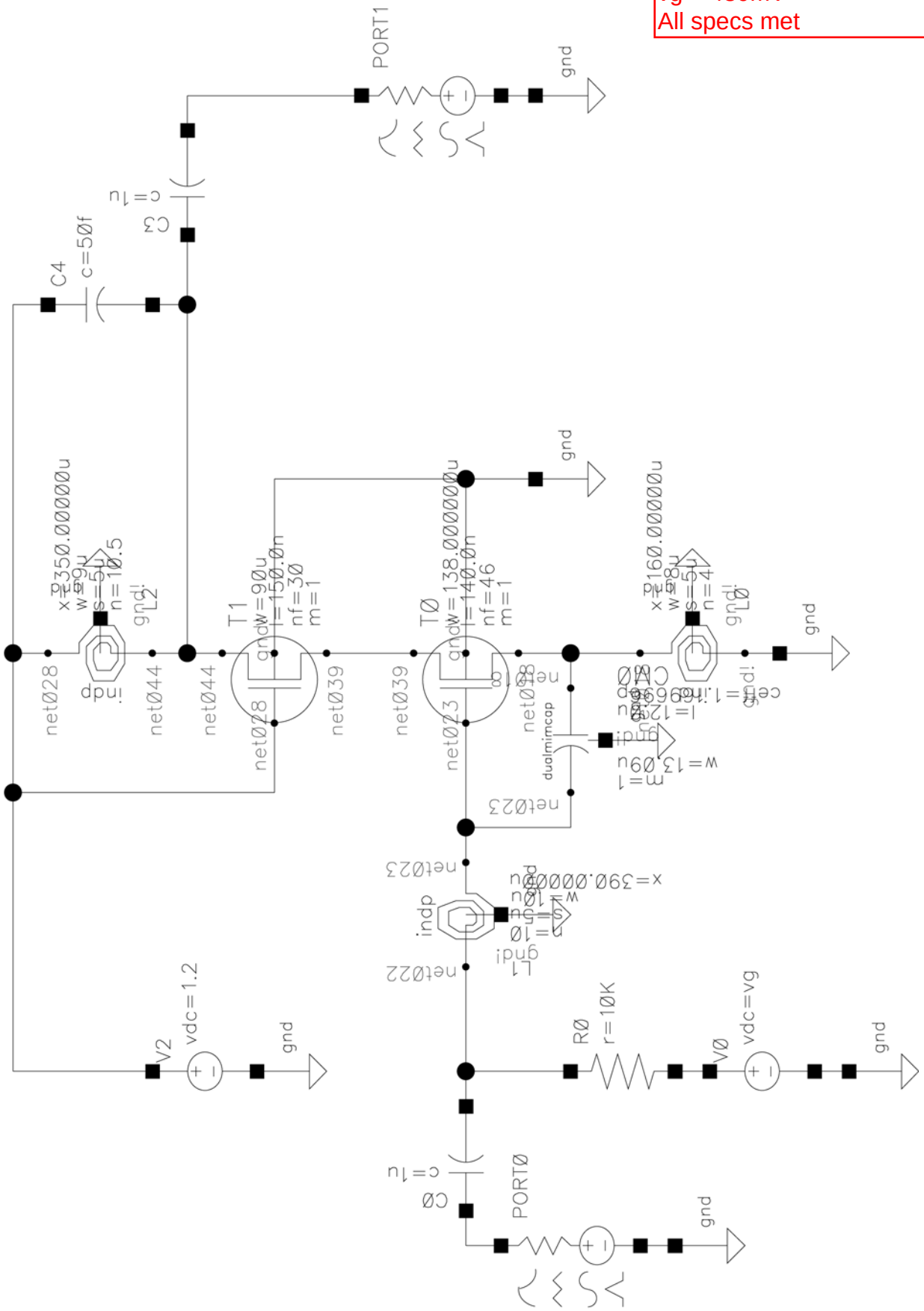
Solution from David Wentzloff
vg = 480mV
All specs met



A GSM Band Low-Power LNA

1. LNA Schematic

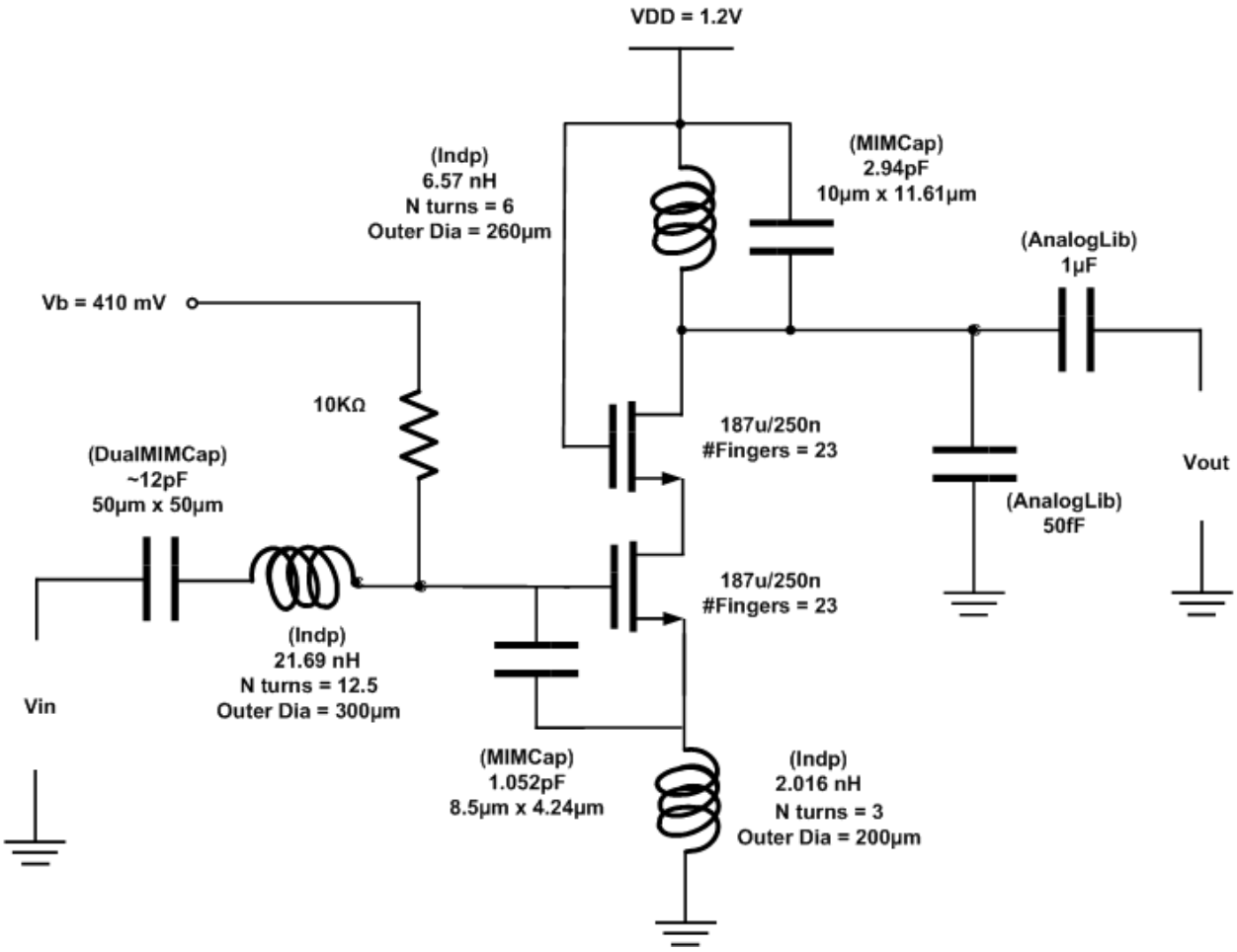


Fig1.1 Schematic of the Designed LNA

2. Design Summary

Specification	Required	Simulation Results
Peak S21 (Gain)	> 10dB	>11 dB
3dB Bandwidth	> 200MHz (<300MHz)	574 M
Center Frequency	900MHz	893.5 MHz
Noise Figure	< 1.7dB (800-1000MHz)	1.275dB (800MHz) 1.566dB (1000MHz)
S11	< -10dB (800-1000MHz)	-10.45dB (800MHz) -25.56dB (917.6MHz) -14.26dB (1000MHz)
P1dB	>-30dBm (input referred)	-3.68dBm
IIP3	>-15dBm (input referred)	7.586dBm
Power Consumption	<4mW (total)	3.846mW

3. Simulation Results

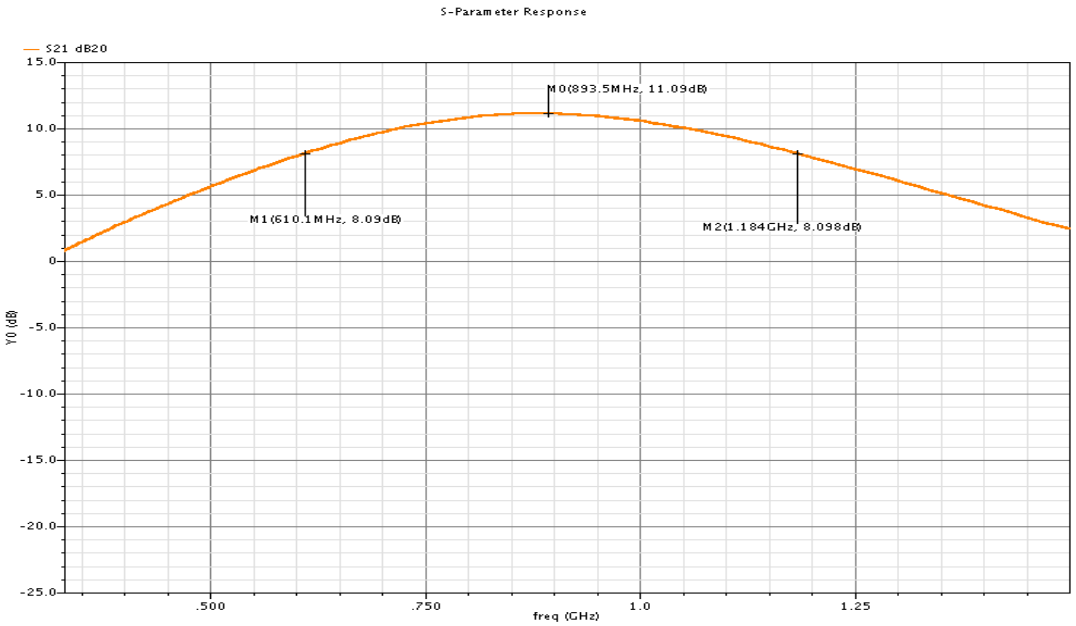


Fig1.2 Simulation Result for S21

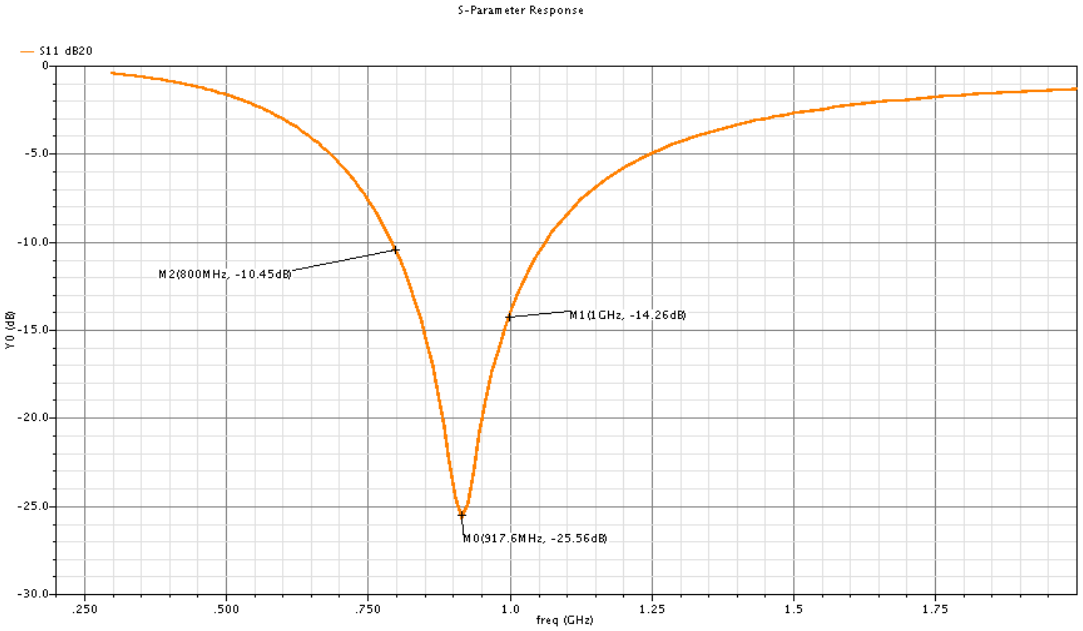


Fig1.3 Simulation Result for S11

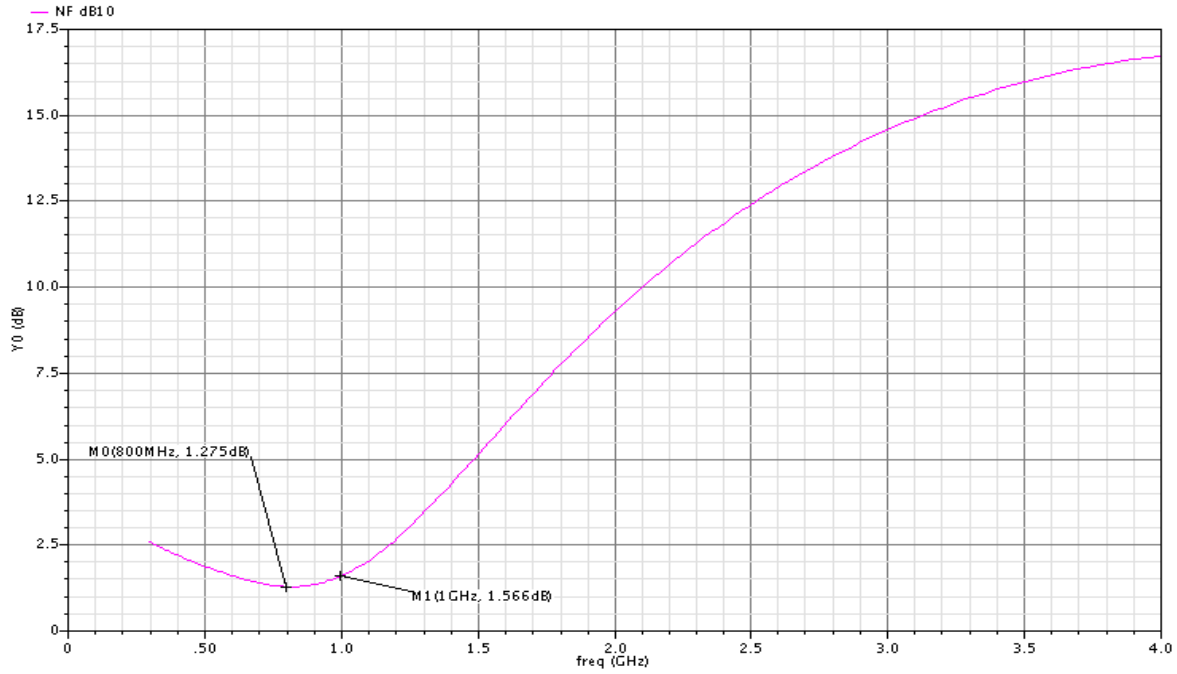


Fig1.4 Simulation Result for Noise Figure

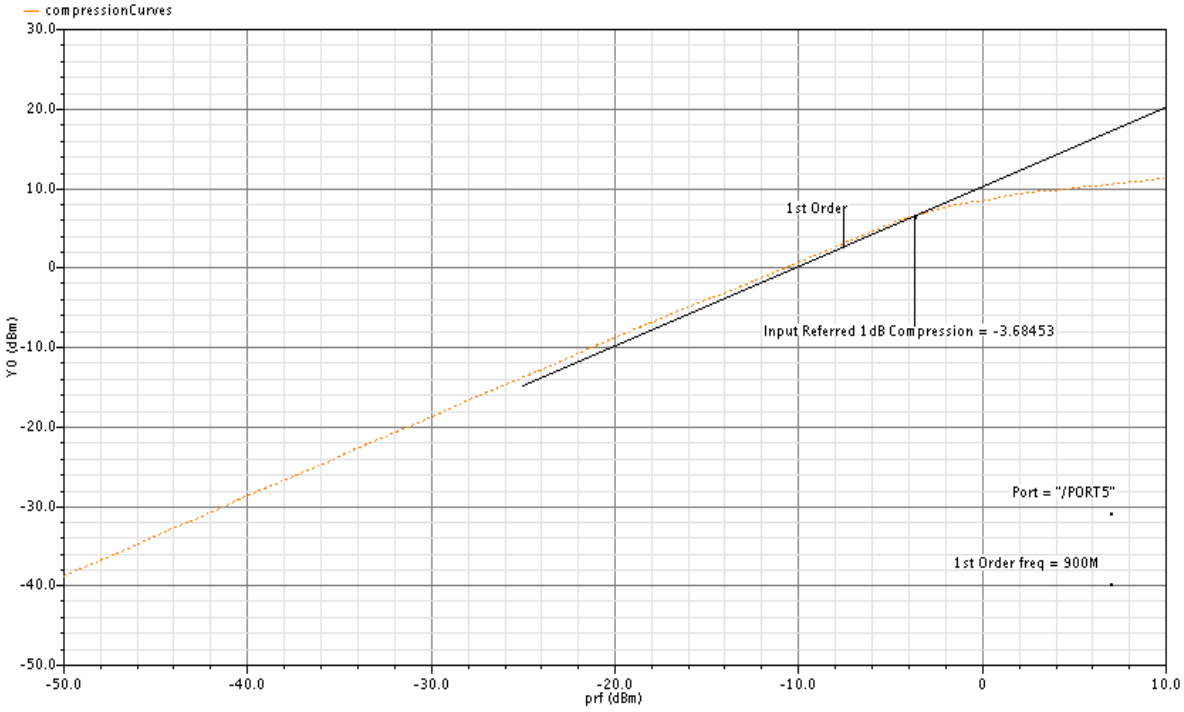


Fig1.5 Simulation Result for P1dB

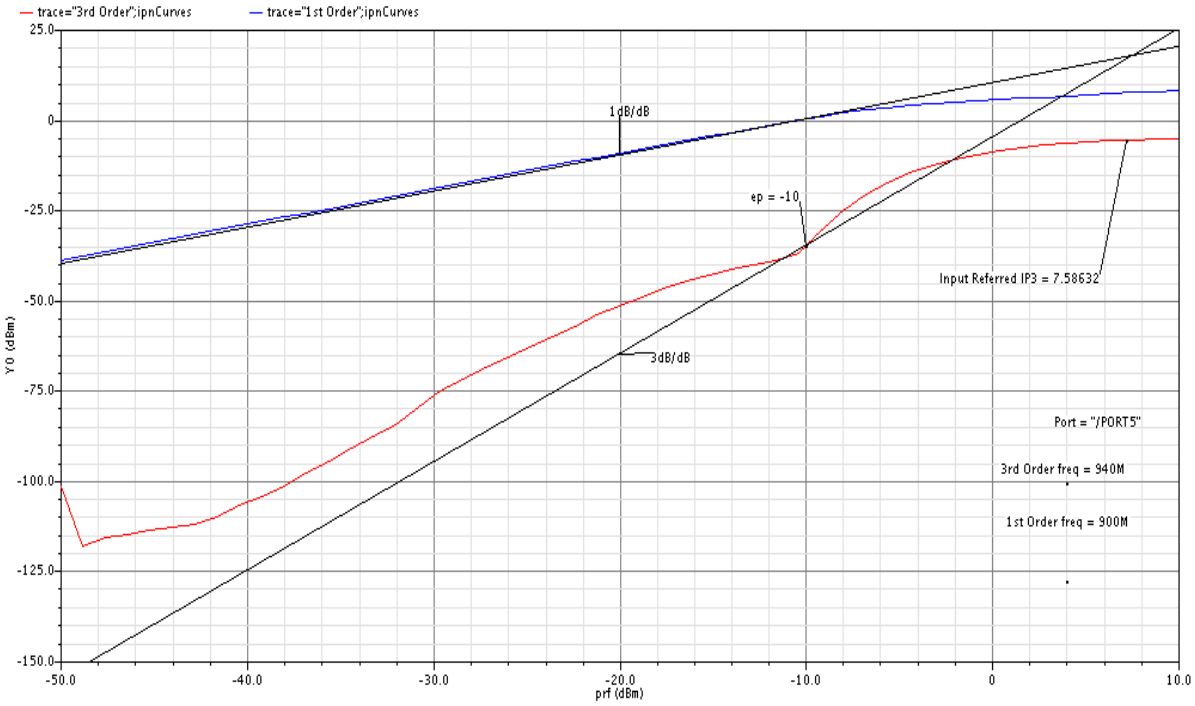


Fig1.6 Simulation Result for IIP3 (Start point = -10dBm)

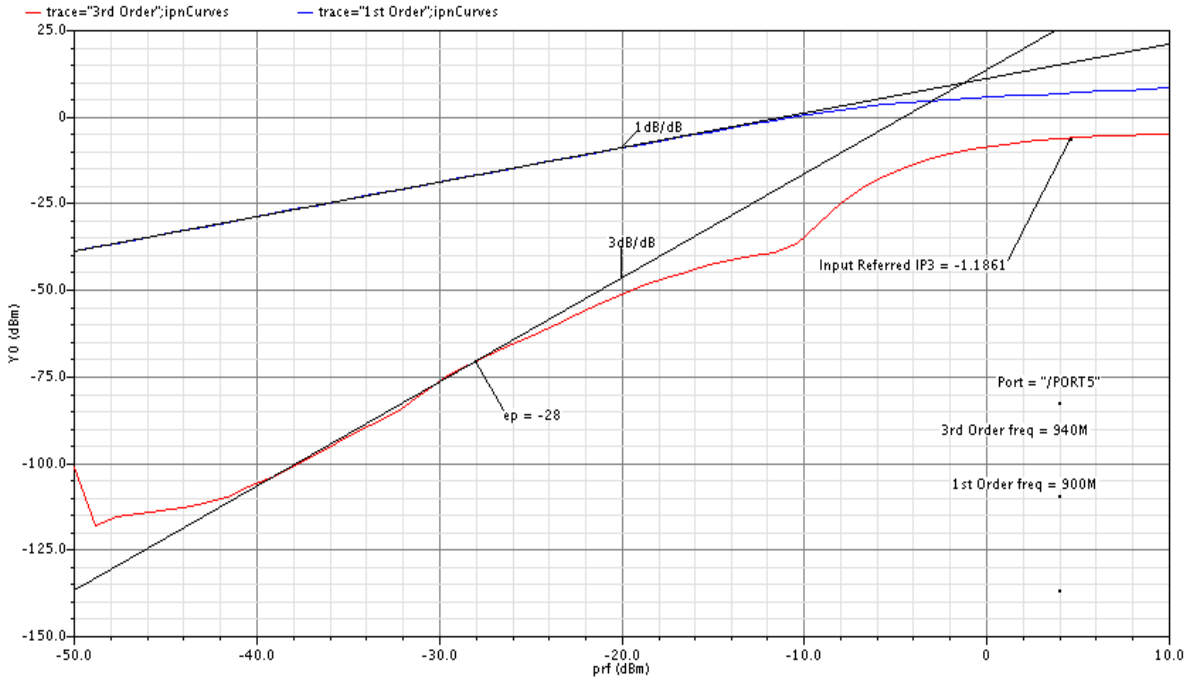


Fig1.6 Simulation Result for IIP3 (Start point = -28dBm)

CAD II: Low-Noise Amplifier Design

I. Device parameter summary

Inductors

Locations	Value	Outer diameter	# of Turns
gate inductance	16.407 nH	1.64 mm	2
source degen.	2.498 nH	410 um	2
load inductance	171.22 nH	10 mm	2

Capacitor (for C_{GS} compensation)

Location	Value	X dimension	Y dimension
Cgs compensation	16.407 nH	1.64 mm	2

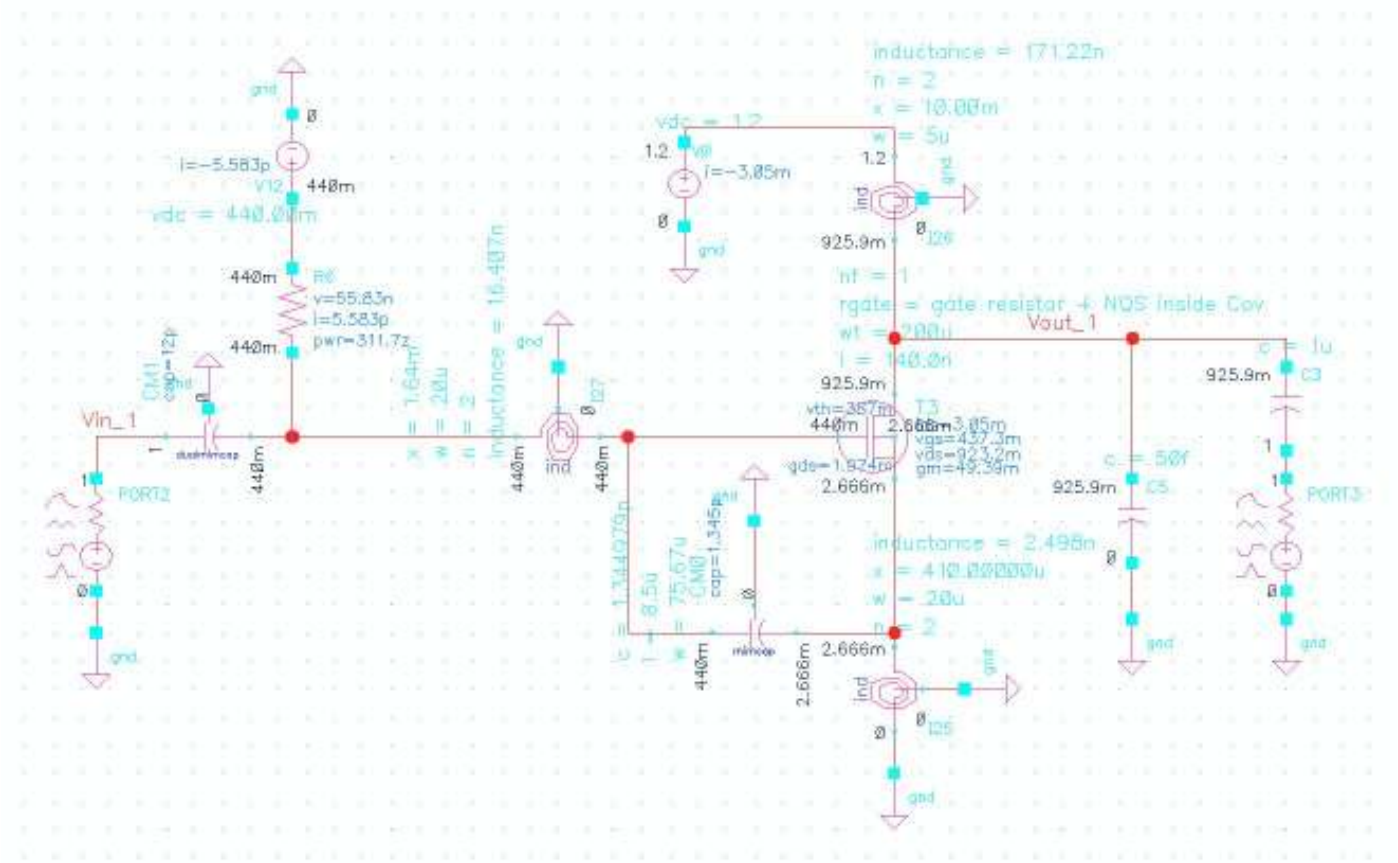
MOSFET

Location	Width	Length	#r of fingers
Input	200 um	0.14 um	1

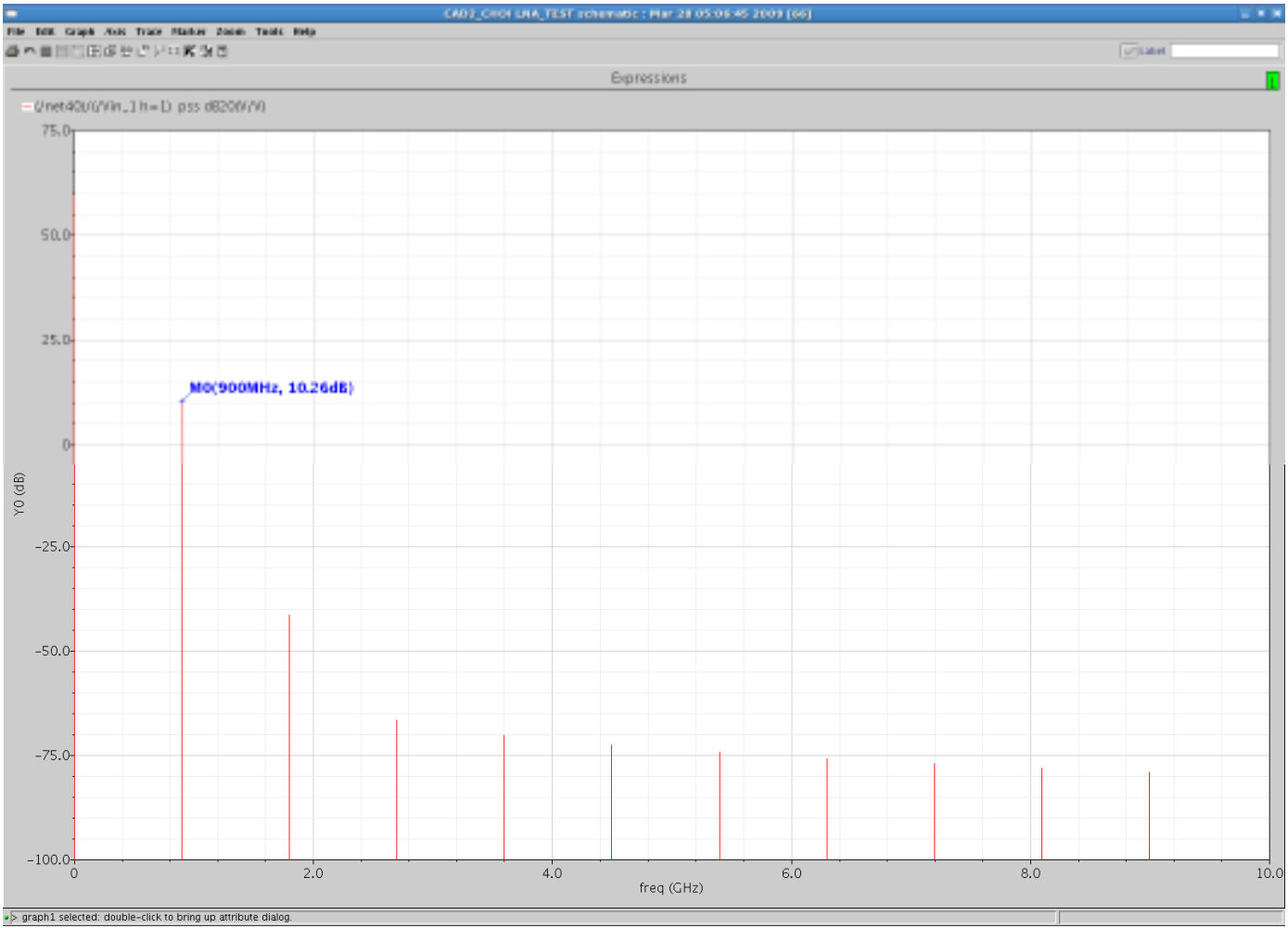
II. Simulation Results

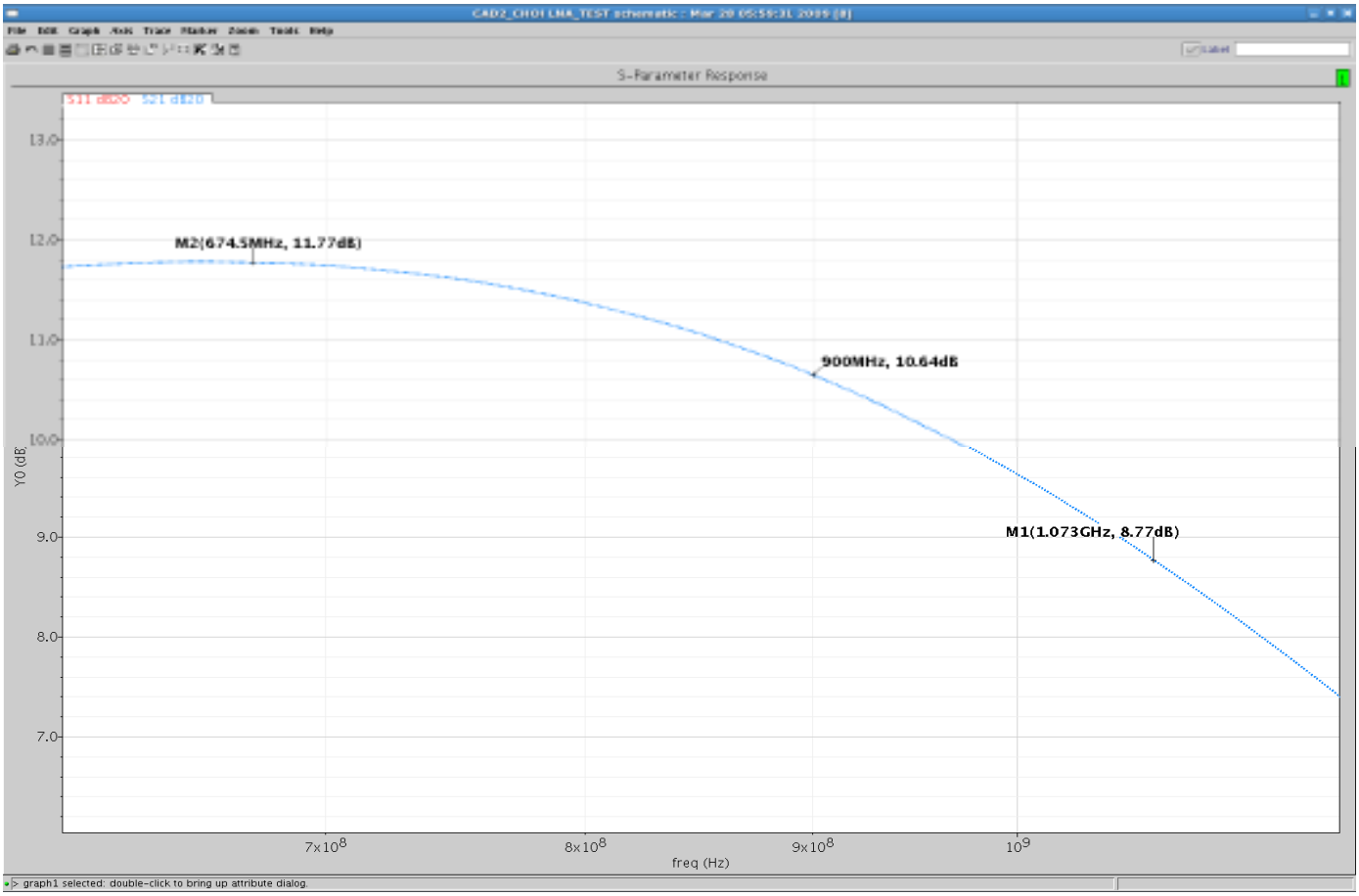
Parameters	Result
Peak S21 (Gain)	10. 26 dB
3 dB BW	797 MHz
Center Freq.	674.5 MHz
S11	-10.01 dB
Noise Figure	< 1.576 dB
P1 dB	- 12.79 dBm
IIP3	- 7.52 dB
Power Consumption	3.66 mW

Schematic

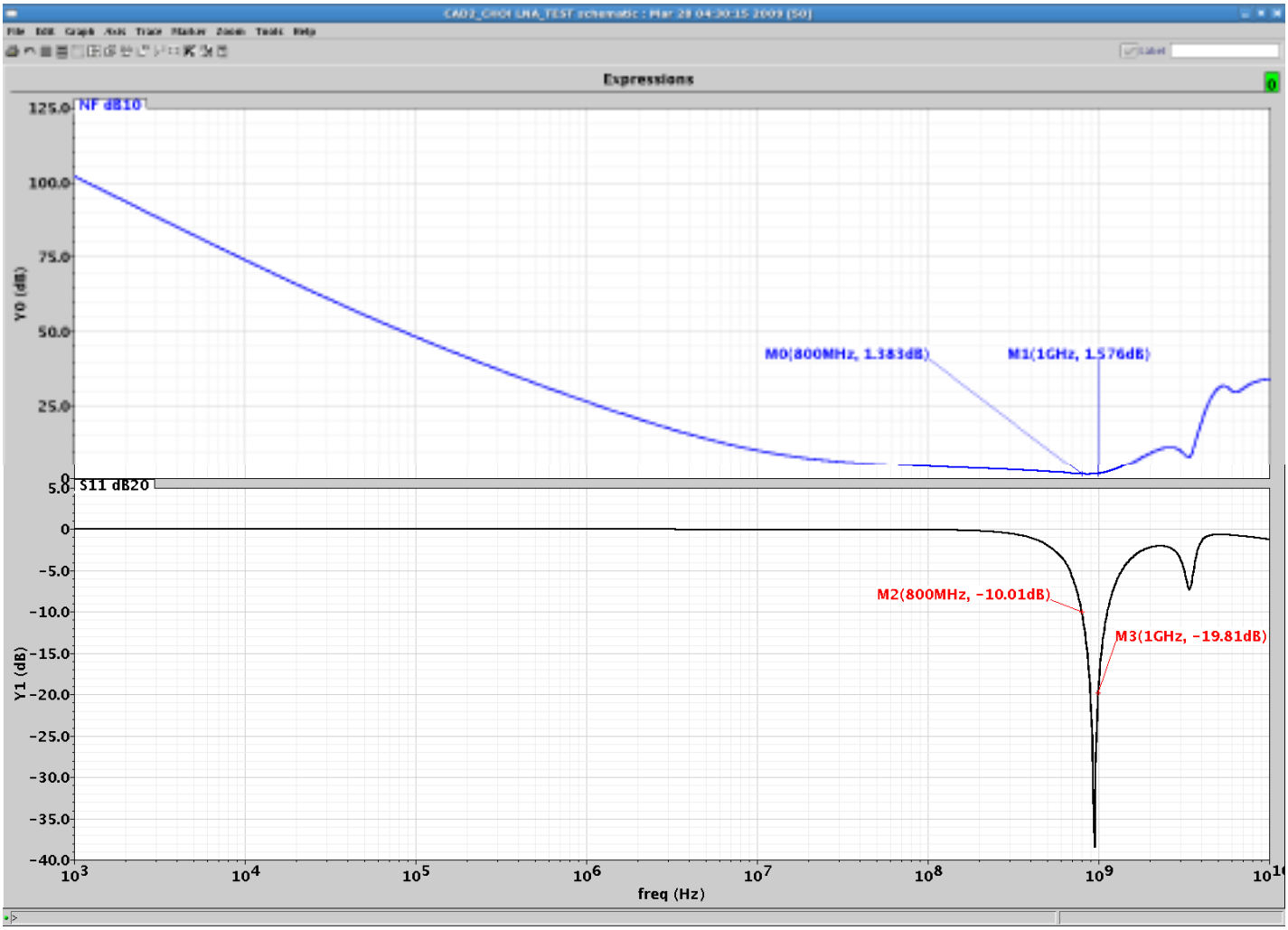

inductance = 171.22n
n = 2
x = 10.00m
w = 5u
vdc = 1.2
1.2
i=-3.85m
925.9m
nf = 1
rgate = gate resistor + NOS inside Cov
wt = 200u
l = 140.0n
Vout_1
925.9m
C = 1u
C3
925.9m
vth=357m
440m
2.666m
vgs=437.3m
vds=923.2m
gm=49.59m
gds=1.924m
T3
C = 50f
C5
925.9m
inductance = 2.498n
x = 410.00000u
w = 20u
n = 2
2.666m
2.666m
440m
Vin_1
PORT2
PORT3
440m
440m
440m
440m
440m
i=-5.583p
V12
vdc = 440.00m
440m
R6
v=55.83n
i=5.583p
pwr=311.7z
440m
CM1
cap=12f
1.64m
x
20u
w
2
n
inductance = 16.487n
ind
I27
1.344079n
8.5u
75.67u
CM0
cap=1.345fF
ind
I26
ind
I25
gnd

S21 (PSS)

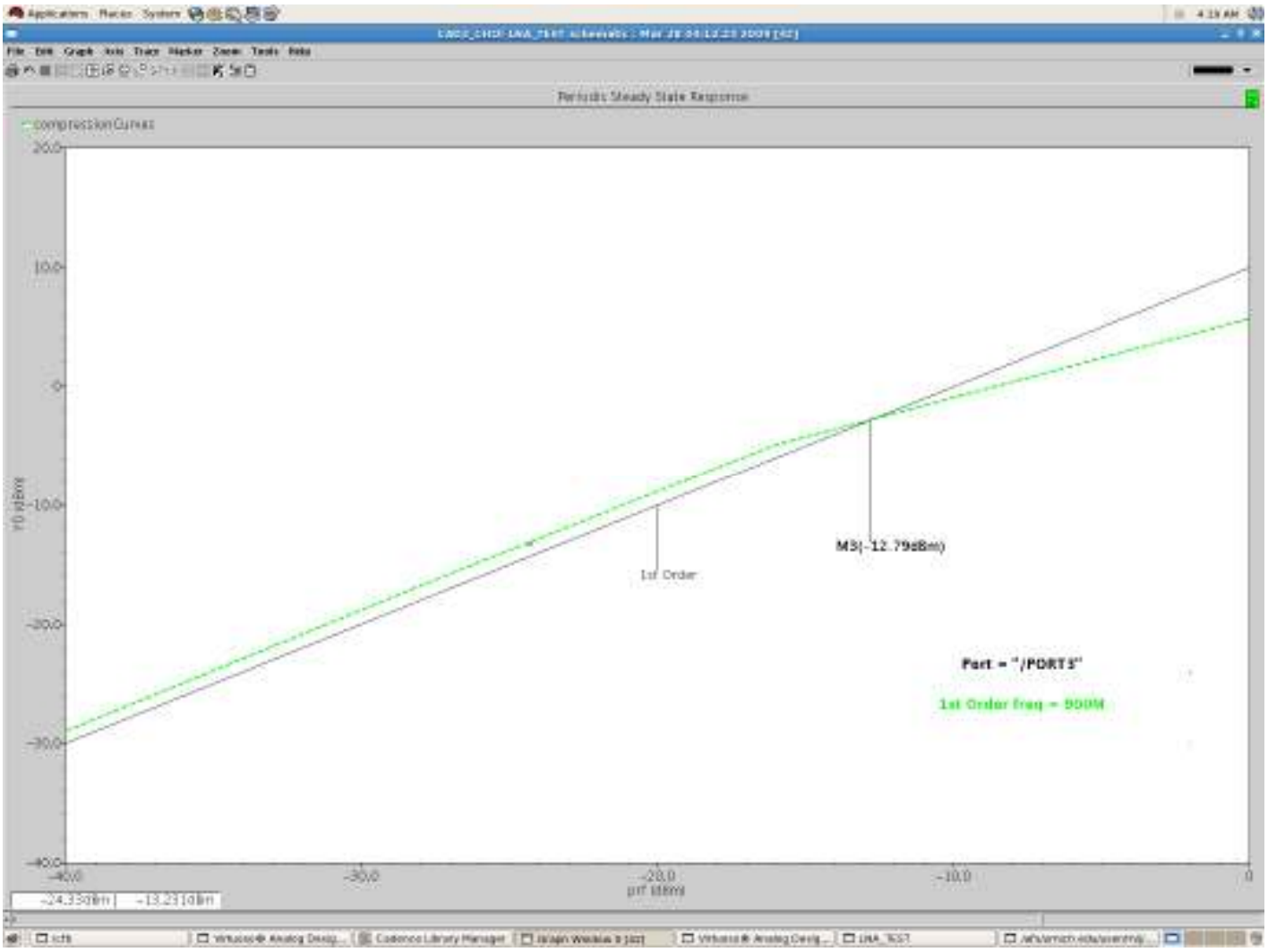

Expressions
M0(900MHz, 10.26dB)
Y0 (dB)
freq (GHz)
graph1 selected: double-click to bring up attribute dialog.


S-Parameter Response
M2(674.5MHz, 11.77dB)
900MHz, 10.64dB
M1(1.073GHz, 8.77dB)
Y0 (dB)
freq (Hz)
graph1 selected: double-click to bring up attribute dialog.

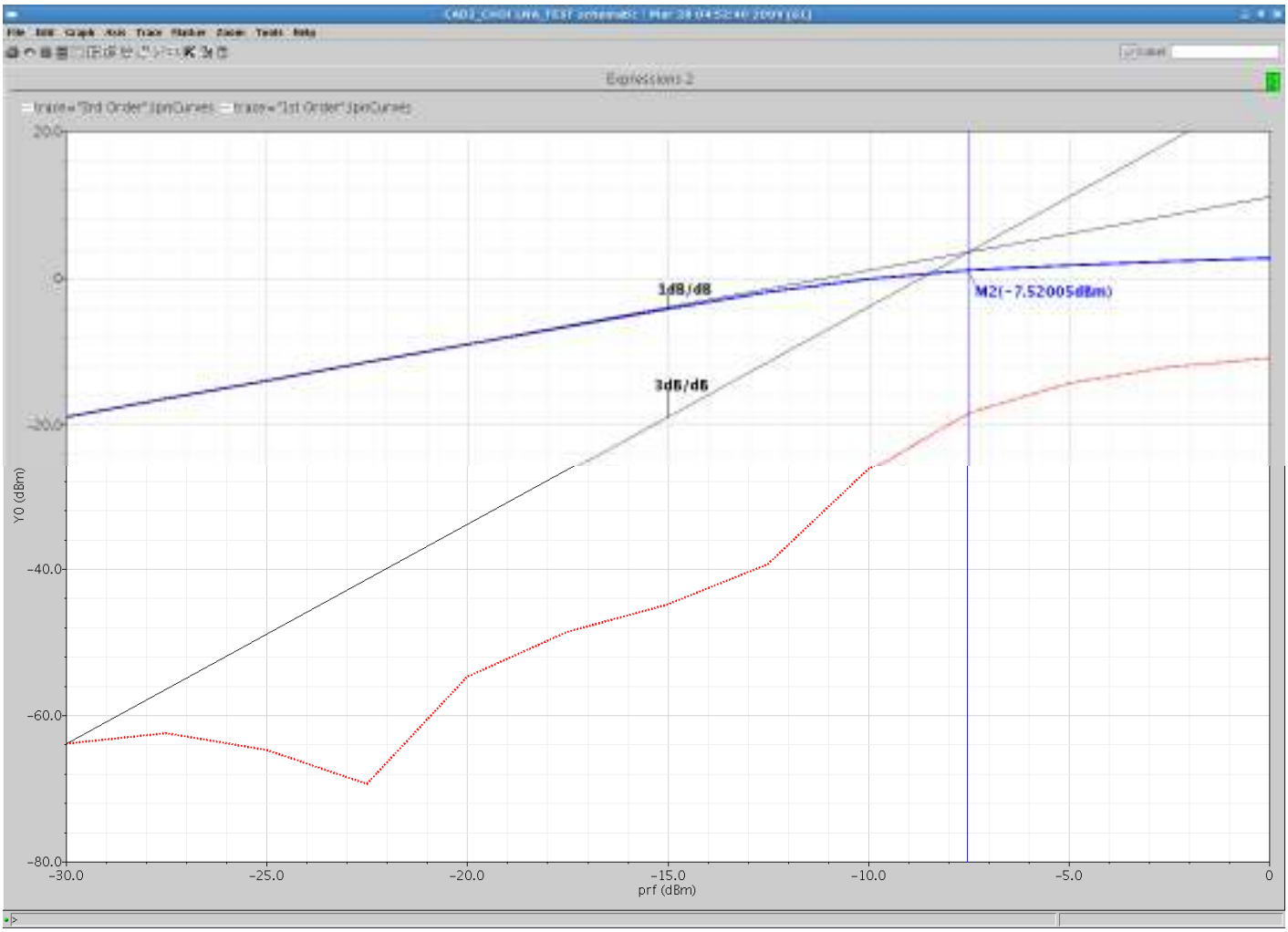
NF & S11


Expressions
NF dB10
M0(800MHz, 1.383dB)
M1(1GHz, 1.576dB)
Y0 (dB)
S11 dB20
M2(800MHz, -10.01dB)
M3(1GHz, -19.81dB)
Y1 (dB)
freq (Hz)

P1dB


Periodic Steady State Response
compressionCurve1
20.0
10.0
0
-10.0
-20.0
-30.0
-40.0
y0 (dBm)
M5(-12.79dBm)
1st Order
Part = "/PORT5"
1st Order freq = 900M
-40.0
-30.0
-20.0
-10.0
0
pin (dBm)
-24.35dBm
-13.21dBm

IIP3


Expressions 2
trace="3rd Order" ipxCurves
trace="1st Order" ipxCurves
20.0
0
-20.0
-40.0
-60.0
-80.0
Y0 (dBm)
1dB/dB
3dB/dB
M2(-7.52005dBm)
-30.0
-25.0
-20.0
-15.0
-10.0
-5.0
0
prf (dBm)

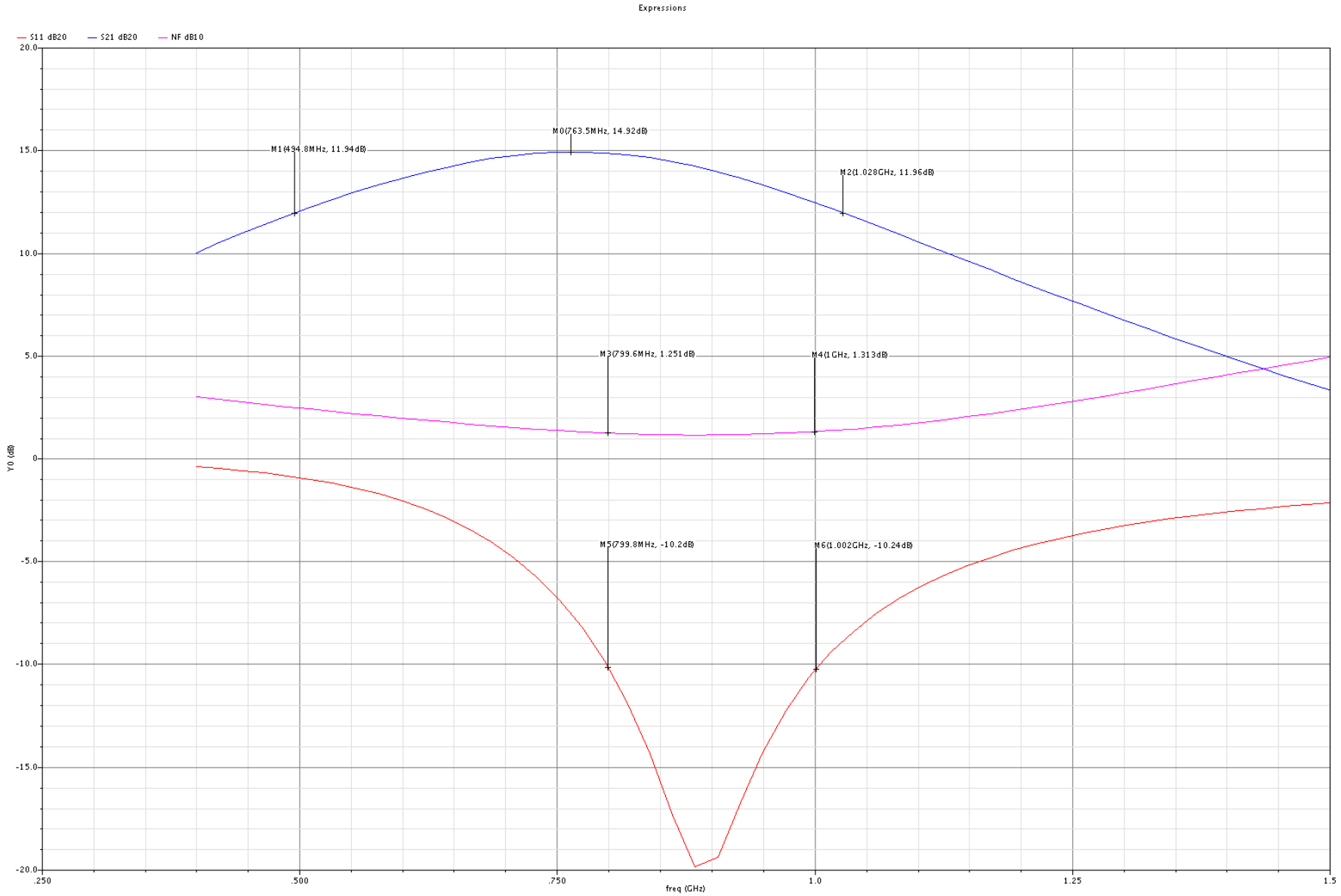


Figure 1. NF, S11, S21

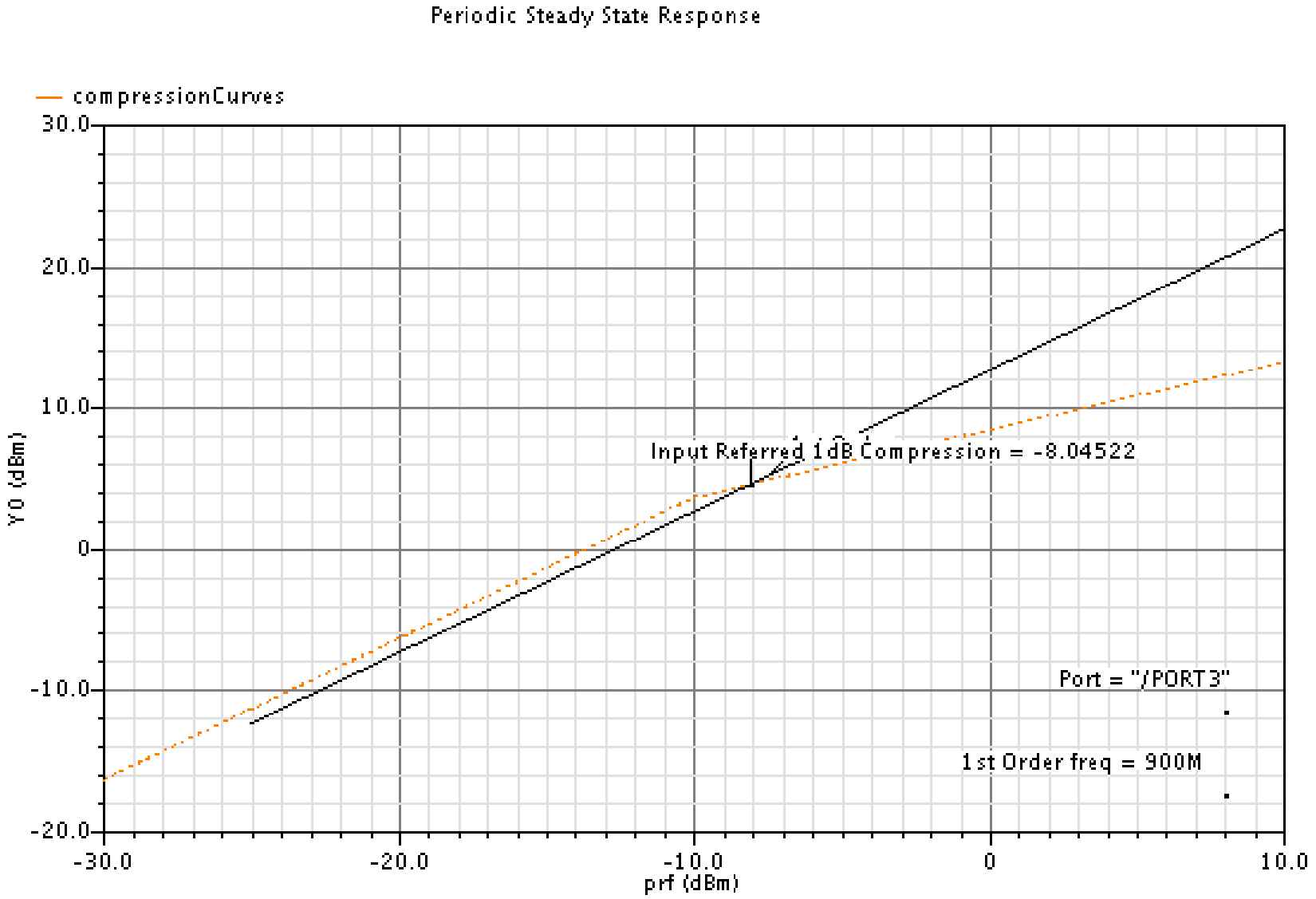


Figure2. 1dB Compression point.

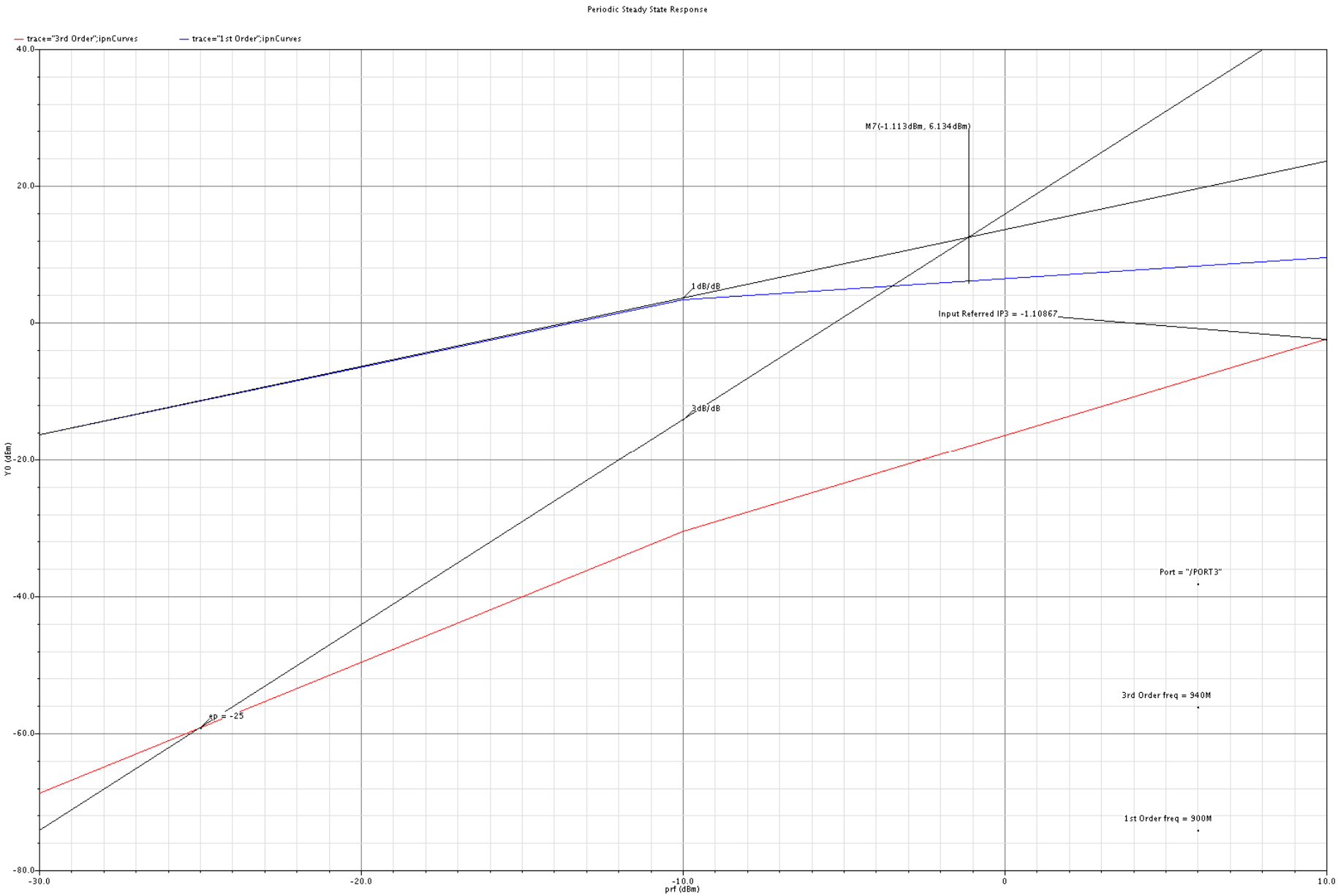
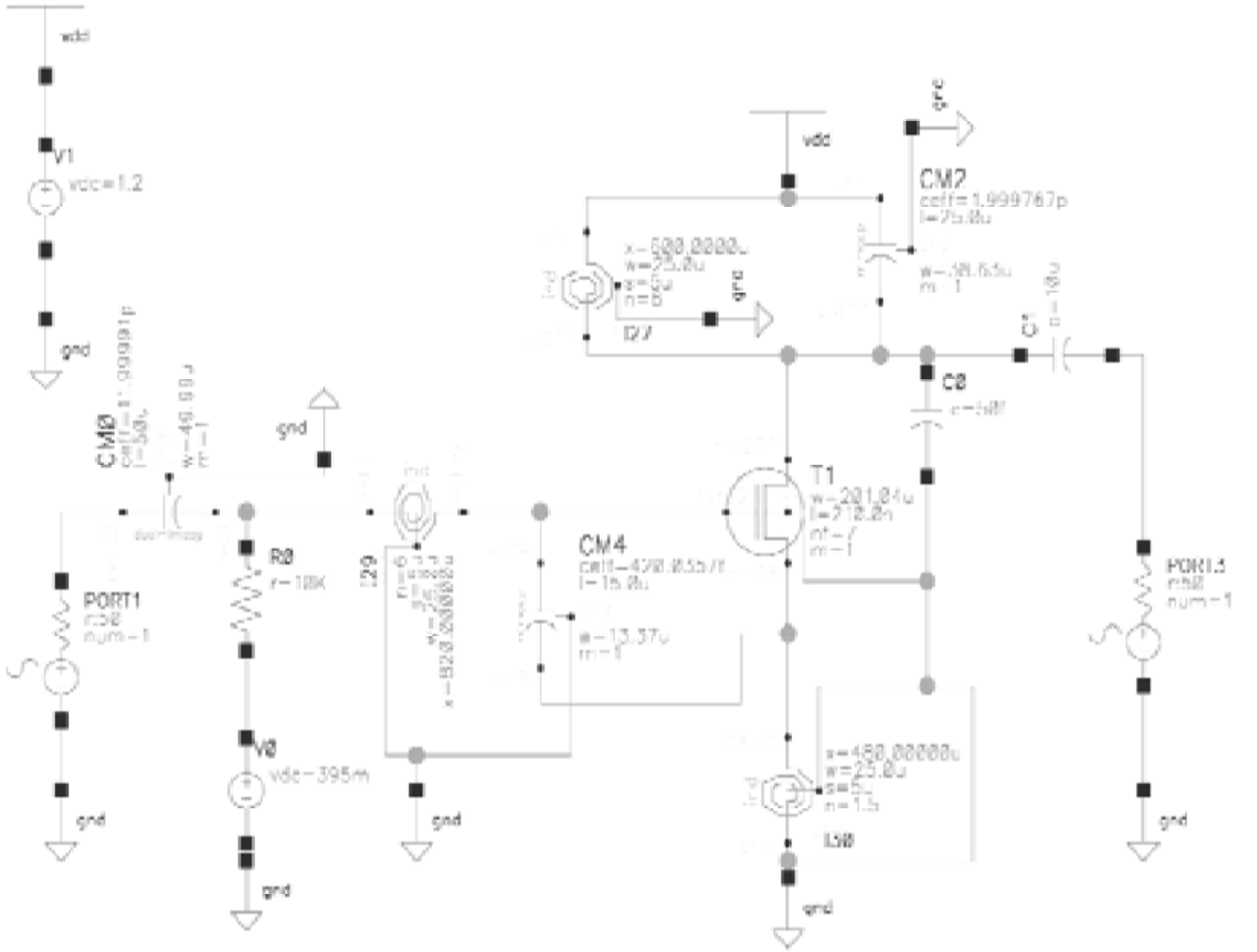


Figure 3. 3dB Compression point.

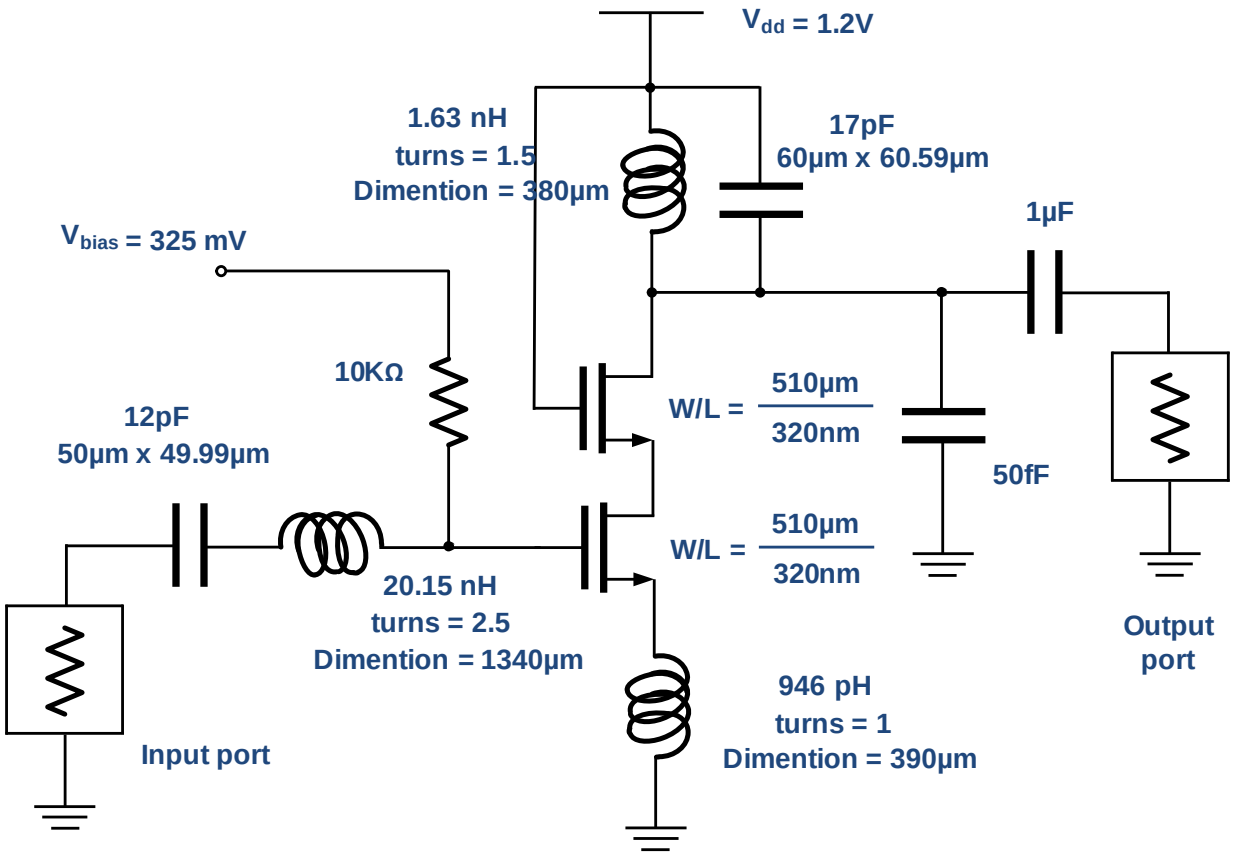
Specification	Desired	Achieved
Peak S21 Gain	>10dB	15dB
3dB Bandwidth	200MHz - 300MHz	500MHz to 1.028GHz
Center Frequency	900MHz	763MHz (for peak Gain) ~900MHz (for NF)
Noise Figure	<1.7dB	1.25dB - 1.31dB
S11	<-10dB	-10.2dB
P1dB	>-30dB	-8.04dB
IIP3	>-15dB	-1.113dB
Power Consumption	< 4mW	3.8mW

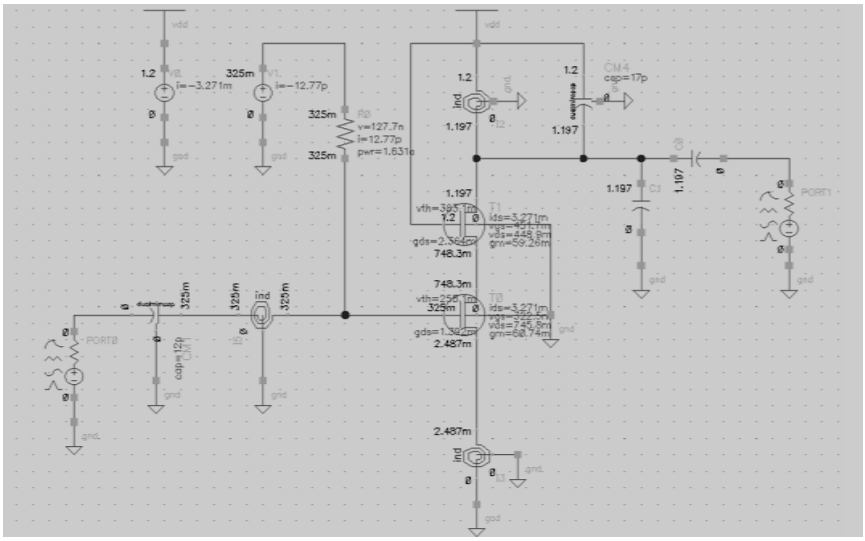
Table 1. Desired vs. Achieved values


vdc
V1
vdc=1.2
gnd
CM0
w=46.88u
m=1
gnd
PORT1
num=1
gnd
R0
r=10K
V0
vdc=395m
gnd
I29
gnd
CM4
w=13.37u
m=1
gnd
vdc
grc
CM7
coff=1.999767p
l=75.8u
w=38.65u
m=1
grc
I27
C1
c=10p
C0
c=1pF
T1
w=201.84u
l=718.8n
nf=7
m=1
x=460.00000u
w=25.8u
m=1.5
I30
gnd
PORT2
num=1
gnd

EECS 522 CAD2

1. Schematic of the LNA

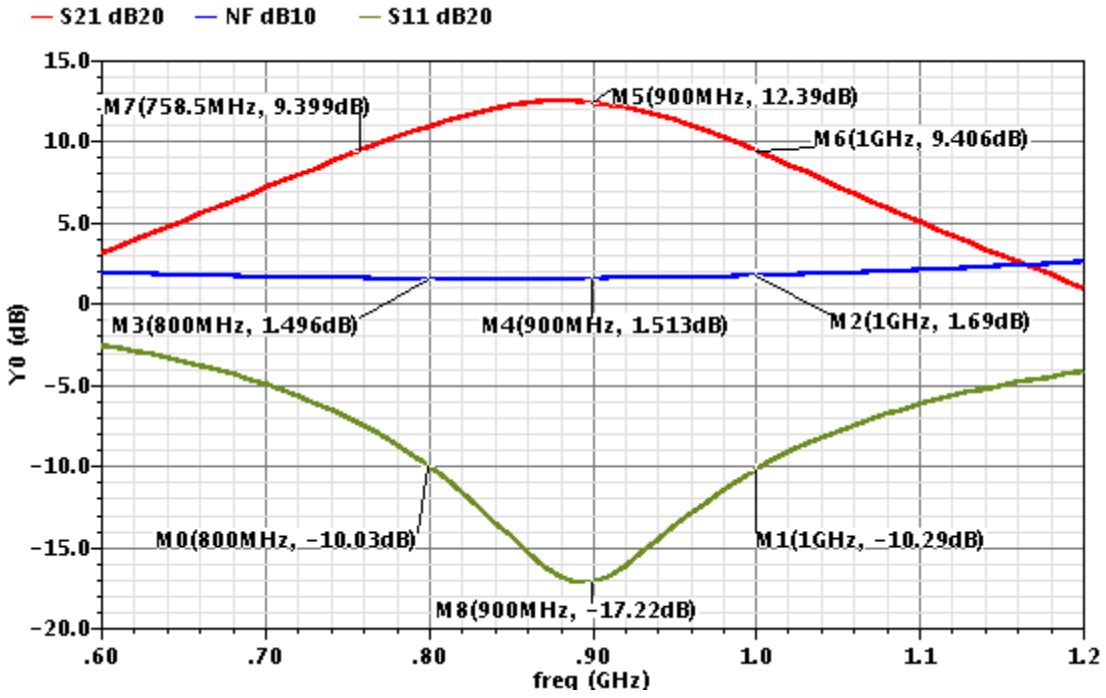


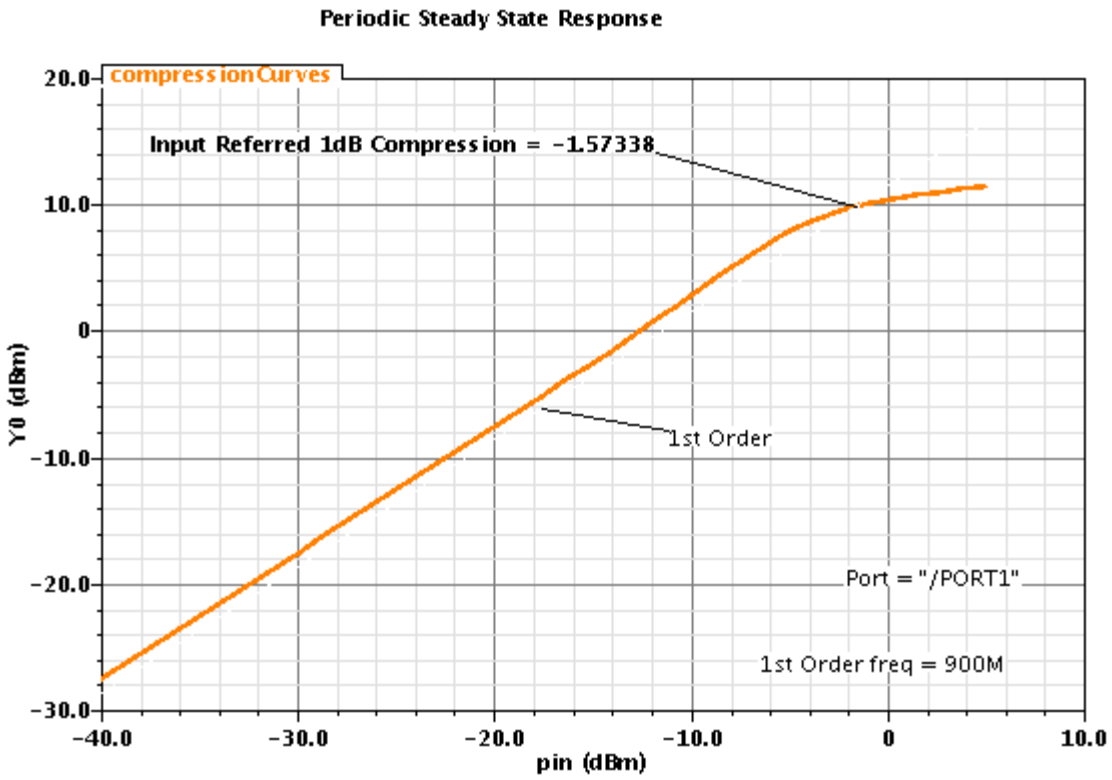


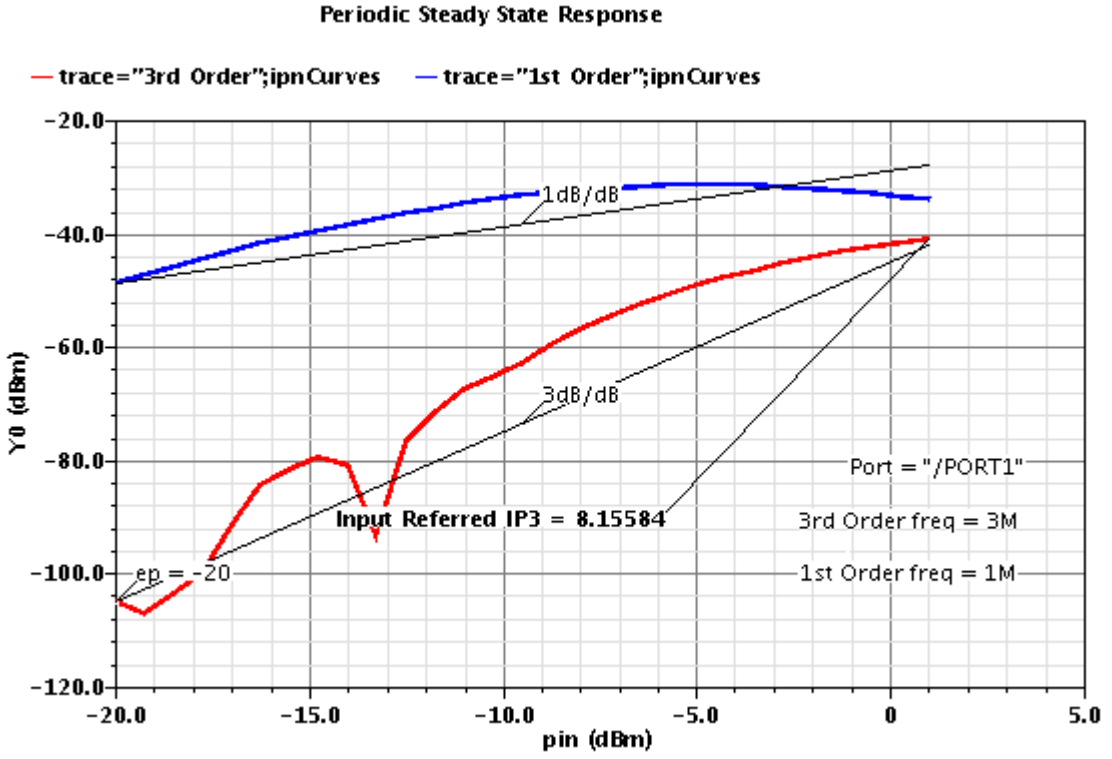
2. Summary Table

	Specification	LNA Design
Peak S21	> 10 dB	12.4 dB
3dB Bandwidth	200 MHz ~ 300 MHz	242 MHz
Center Frequency	900 MHz	880 MHz
Noise Figure	< 1.7 dB from 800 MHz to 1 GHz	< 1.69 dB (in band)
S11	< -10 dB from 800 MHz to 1 GHz	< -10.03 dB (in band)
P1dB	> -30 dBm	-1.57 dBm
IIP3	> -15 dBm	8.15 dBm
Power	< 4 mW	3.924 mW
Path: /afs/umich.edu/user/k/k/kkhuang/eecs522/CAD/CAD_LNA		

3. Plots of S_{11} S_{21} P_{1dB} IIP_3 and Noise Figure




Periodic Steady State Response
compressionCurves
Input Referred 1dB Compression = -1.57338
1st Order
Port = "/PORT1"
1st Order freq = 900M
Y0 (dBm)
pin (dBm)
20.0
10.0
0
-10.0
-20.0
-30.0
-40.0
-30.0
-20.0
-10.0
0
10.0


Periodic Steady State Response
trace="3rd Order";ipnCurves
trace="1st Order";ipnCurves
1dB/dB
3dB/dB
Input Referred IP3 = 8.15584
ep = -20
Port = "/PORT1"
3rd Order freq = 3M
1st Order freq = 1M
Y0 (dBm)
pin (dBm)
-20.0
-40.0
-60.0
-80.0
-100.0
-120.0
-20.0
-15.0
-10.0
-5.0
0
5.0

EECS522 CAD 2
Submitted March 28, 2009

TABLE OF MEASURED VALUES AND SPECIFICATIONS

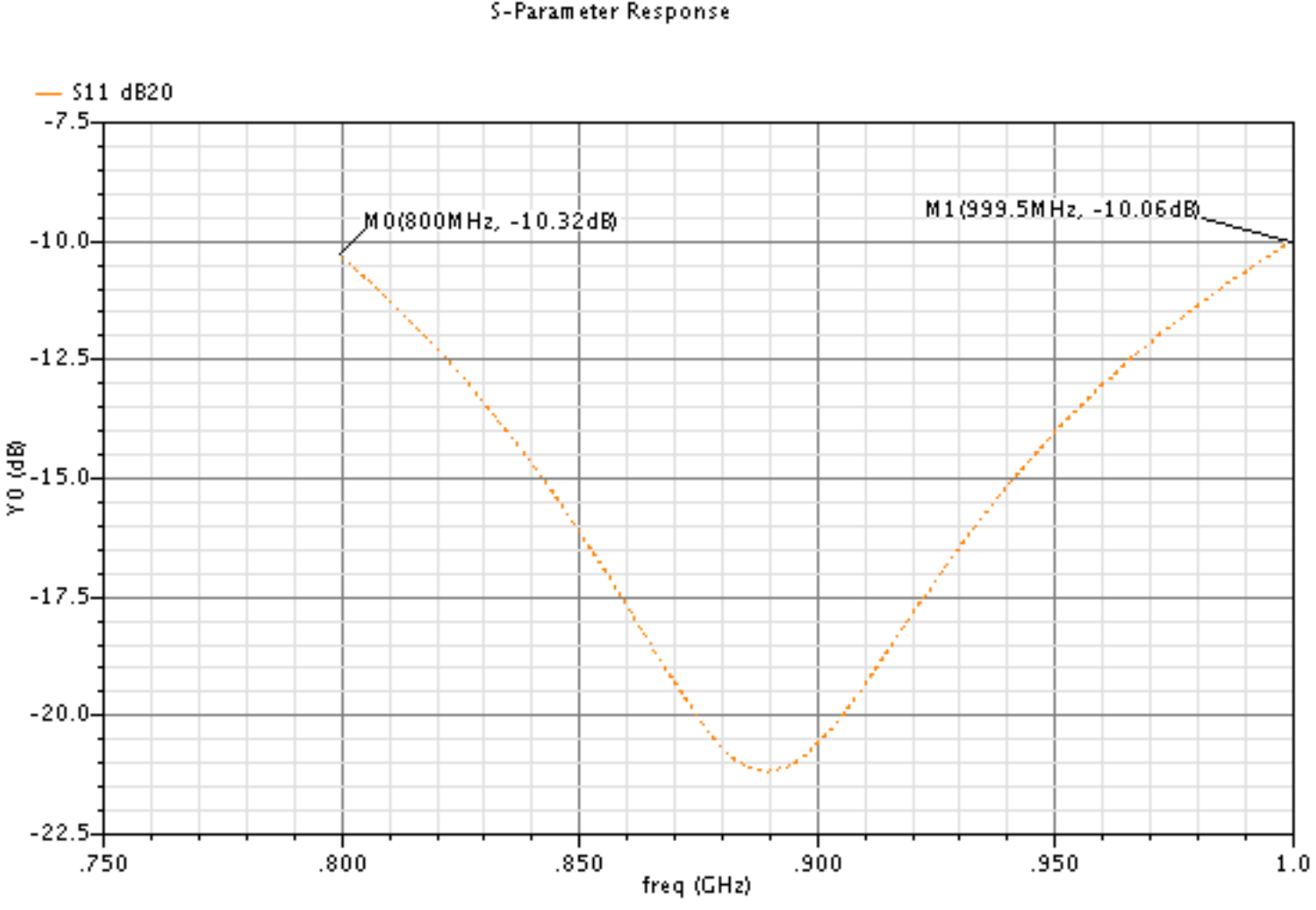
Specification	Required	This LNA
Peak S21 (Gain)	> 10 dB	13.99 dB
3dB Bandwidth	200 MHz < BW <300 MHz	299.5 MHz
Center Frequency	900 MHz	895.7 MHz
Noise Figure	< 1.7 dB between 800 MHz and 1 GHz	1.682 dB max
S11	< -10 dB between 800 MHz and 1 GHz	-10.32 dB max
P1dB	> -30 dBm (input feferred)	-7.15861 dB
IIP3	> -15 dBm (input referred)	14 dBm
Power Consumption	< 4mW (including bias circuits)	3.972 mW*

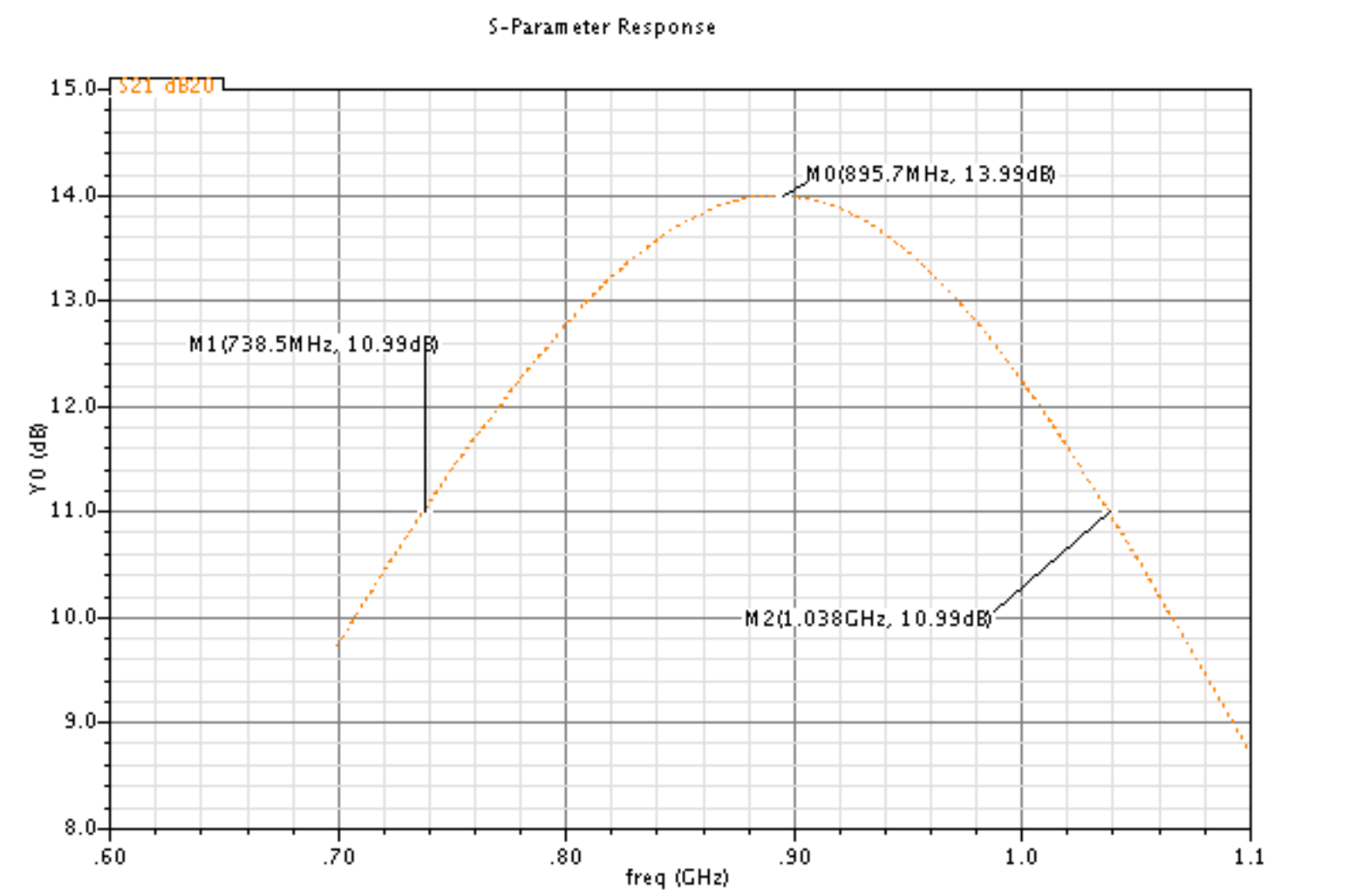
* 3.31 mA is drawn from the 1.2 V supply by the transistors, the bias resistor contribution is negligible (~5 pW)

Attached (in order):

- Illustration of the schematic
- Plots
  - S11
  - S21
  - P1dB
  - IIP3
  - Noise Figure

vdd
vdd!
x=680.00000u
w=5u
c=5u
n=1
gnd!
I14
net034
net034
vdd!
gnd!
top
w=750.00000u
l=100.0n
nf=30
m=1
net036
net034
CM1
ceff=12.0022p
l=50u
gnd!
w=50u
m=1
gnd!
C4
c=1
C0
c=50f
PORT0
r:50
num=2
gnd
gnd
gnd
net036
net1
gnd!
bottom
w=750.00000u
l=100.0n
nf=30
m=1
net9
CM0
ceff=12.0022p
l=50u
gnd!
w=5u
m=1
x=840.00000u
w=5u
c=5u
n=3.5
gnd!
I3
net5
dualmimcap
net13
net13
indp
net1
R2
r=10K
CM5
ceff=59.57881f
l=5.24u
gnd!
w=5.24u
m=1
CM7
ceff=59.57881f
l=5.24u
gnd!
w=5.24u
m=1
net1
mimcap
net034
net034
mimcap
net9
net9
x=350.00000u
w=5u
c=5u
n=1
indp
gnd!
I2
gnd!
gnd
vdd
V3
vdc=1.2
gnd
RF
r:50
num=1
gnd
V2
vdc=355.0m
gnd


S-Parameter Response
S11 dB20
-7.5
-10.0
-12.5
-15.0
-17.5
-20.0
-22.5
Y0 (dB)
M0(800MHz, -10.32dB)
M1(999.5MHz, -10.06dB)
.750
.800
.850
.900
.950
1.0
freq (GHz)


S-Parameter Response
S21 dB20
M0(895.7MHz, 13.99dB)
M1(738.5MHz, 10.99dB)
M2(1.038GHz, 10.99dB)
15.0
14.0
13.0
12.0
11.0
10.0
9.0
8.0
Y0 (dB)
.60
.70
.80
.90
1.0
1.1
freq (GHz)

compressionC...

Input Referred 1dB Compression = -7.15861

1st Order

Port = "/PORT0"

1st Order freq = 900M

Y0 (dBm)

15.0
10.0
5.0
0
-5.0
-10.0
-15.0
-20.0

-30.0
-25.0
-20.0
-15.0
-10.0
-5.0
0

prf (dBm)

Periodic Steady State Response

1

trace="3rd Order";ip... trace="1st Order";ip...

IIP3 (14 dBm)->

1dB/dB

3dB/dB

ep = -25

Port = "/PORT0"

3rd Order freq = 940M

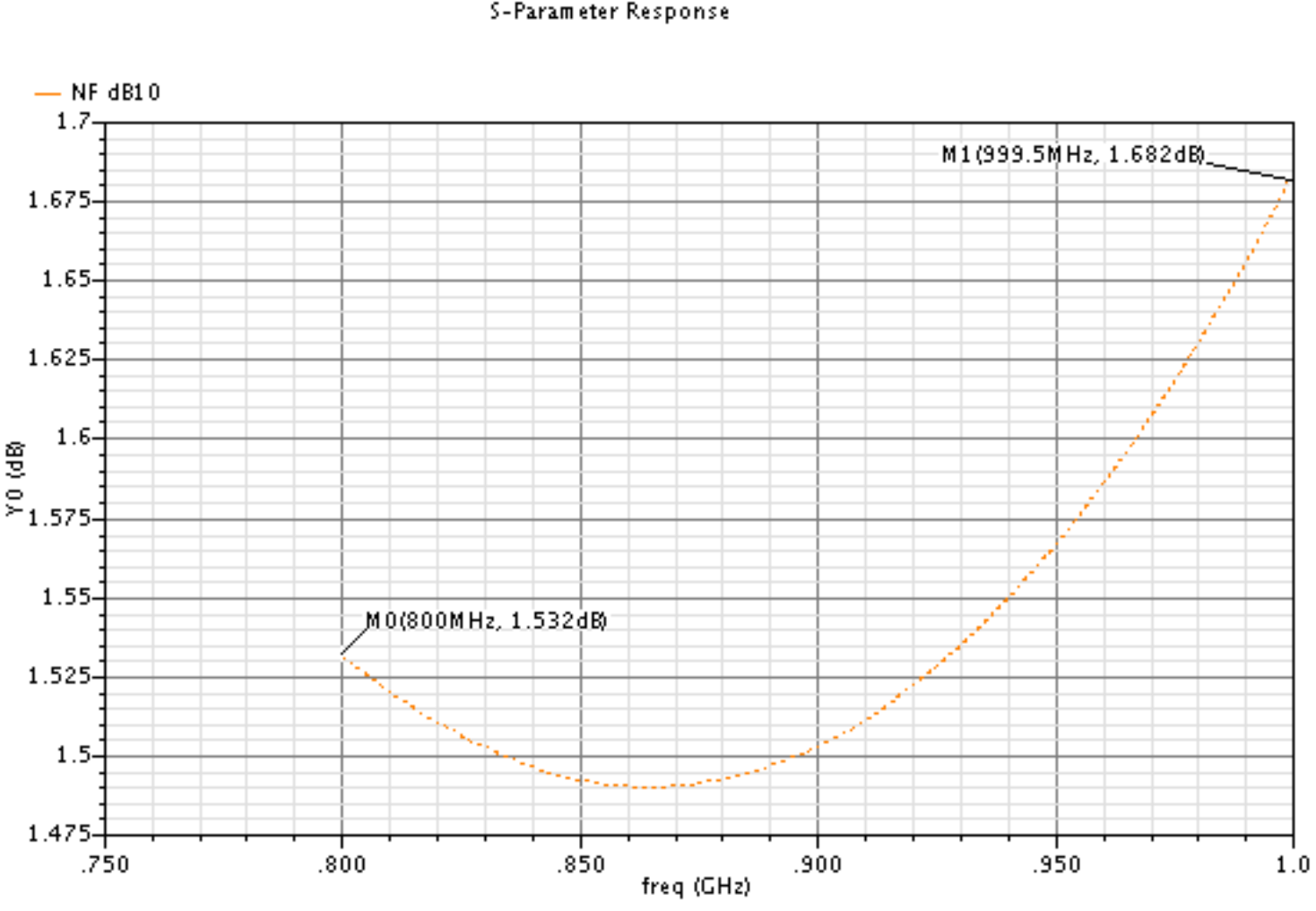
1st Order freq = 900M

Y0 (dBm)

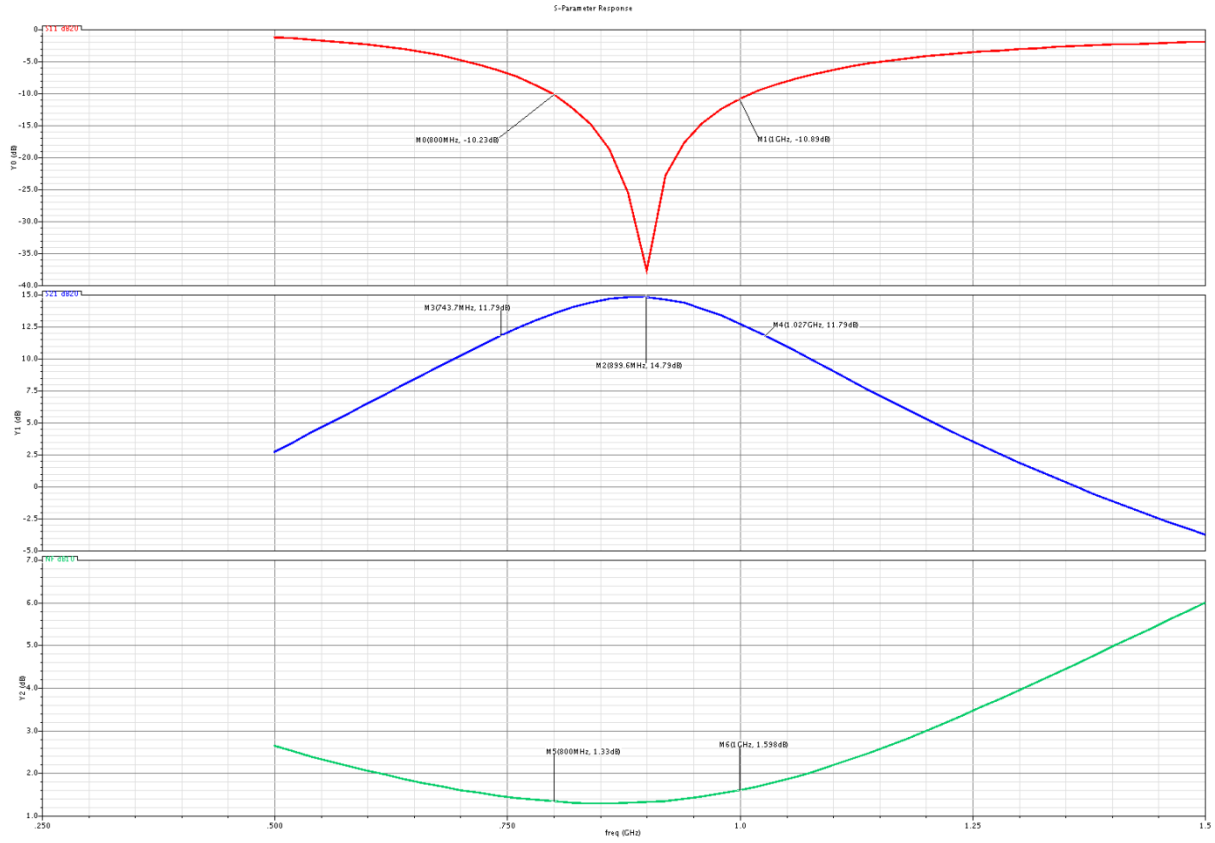
20.0
0
-20.0
-40.0
-60.0
-80.0

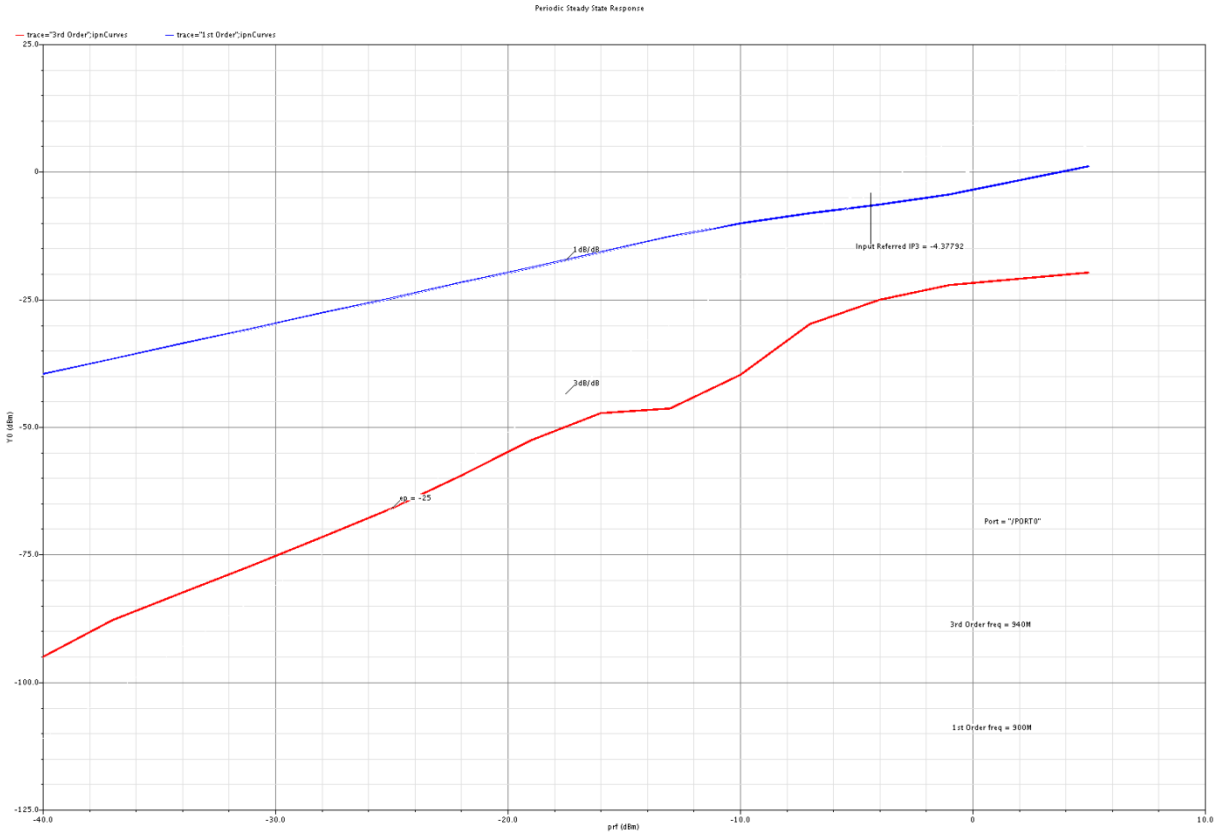
-30.0
-25.0
-20.0
-15.0
-10.0
-5.0
0

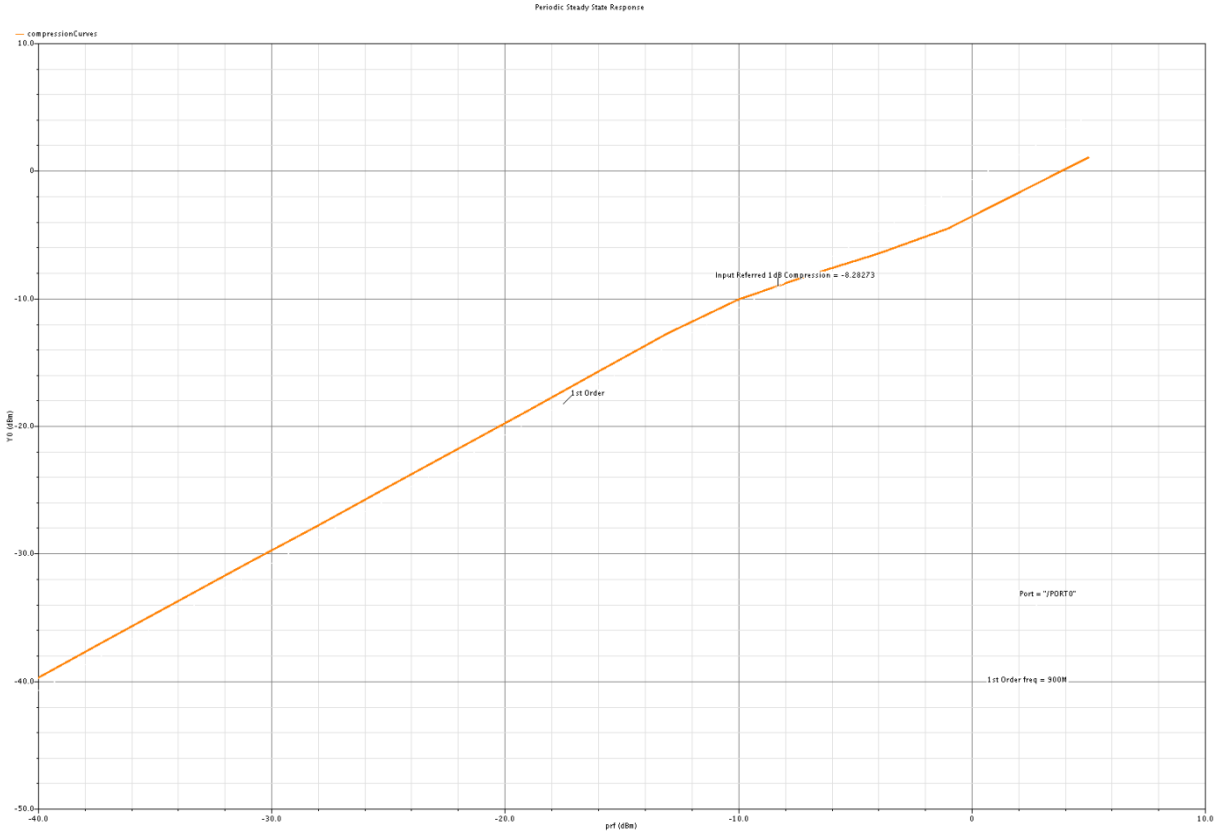
prf (dBm)

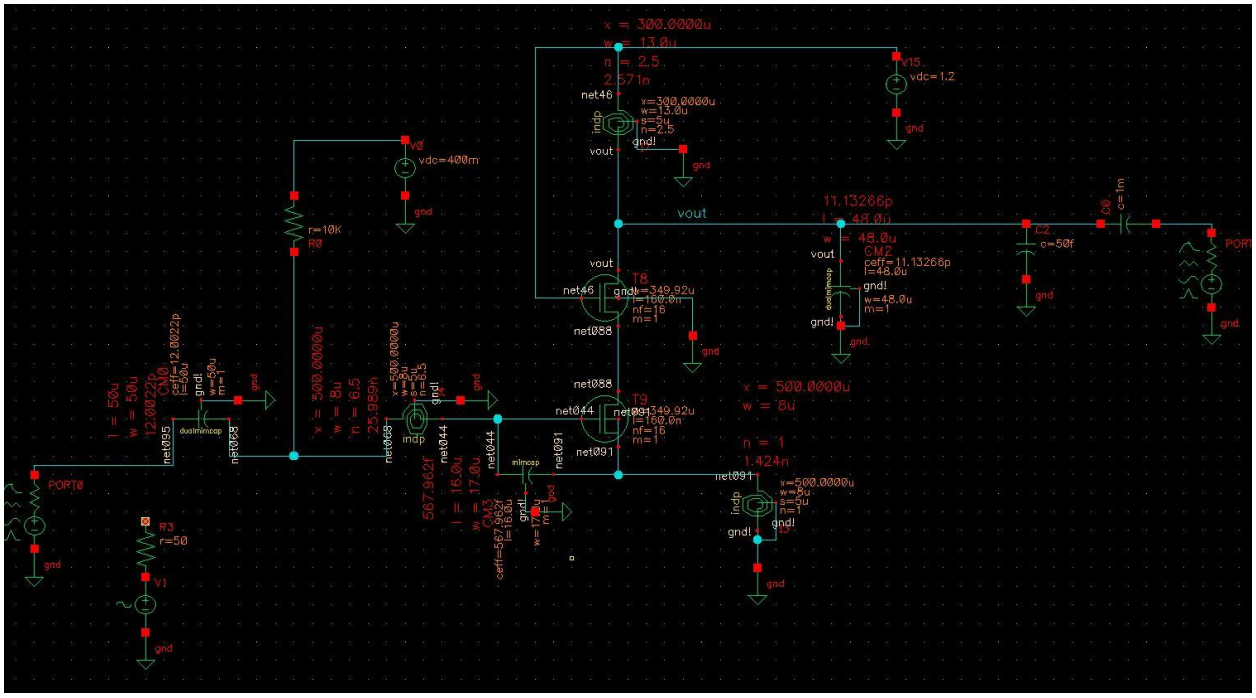

S-Parameter Response
NF dB10
1.7
1.675
1.65
1.625
1.6
1.575
1.55
1.525
1.5
1.475
Y0 (dB)
M1(999.5MHz, 1.682dB)
M0(800MHz, 1.532dB)
.750
.800
.850
.900
.950
1.0
freq (GHz)

Specification	Goal	Simulation Results
S21(Gain)	>10 dB	>13 dB
3db Bandwidth	200 MHz < BW <300 MHz	283 MHz
Center Frequency	900 MHz	900 MHz
Noise Figure	<1.7 dB between 800MHz & 1GHz	<1.6 dB between 800MHz & 1GHz
S11	<-10 dB between 800 MHz & 1 GHz	<-10 dB between 800 MHz & 1 GHz
P1dB	>-30 dBm input referred	-8.3 dBm
IIP3	>-15 dBm input referred	-4.4 dBm
Power Consumption	<4mW	3.87 mW

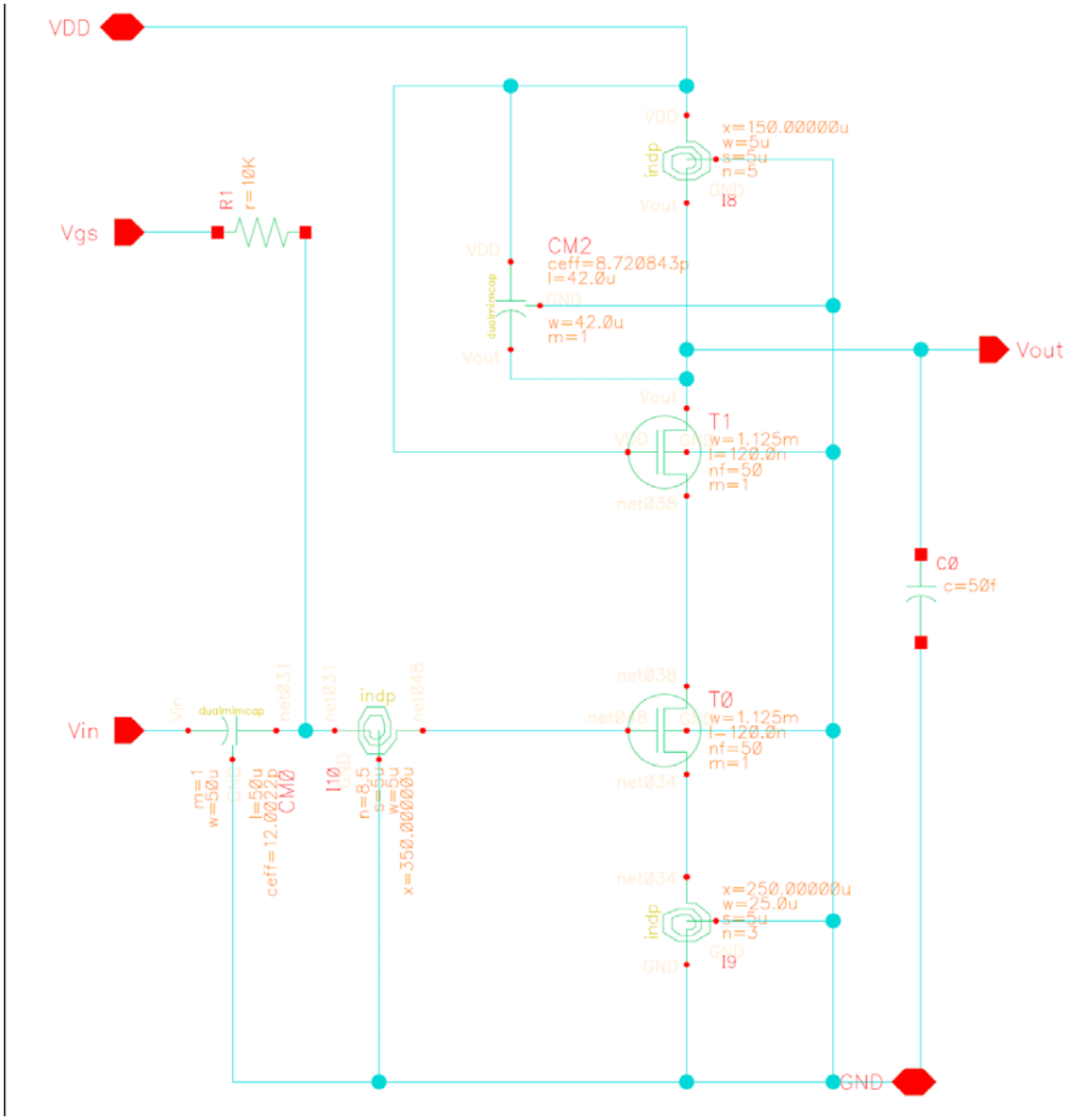



Periodic Steady State Response
trace="3rd Order":ipnCurves
trace="1st Order":ipnCurves
25.0
0
-25.0
-50.0
-75.0
-100.0
-125.0
Y0 (dBm)
-40.0
-30.0
-20.0
-10.0
0
10.0
prf (dBm)
1dB/dB
3dB/dB
Input Referred IP3 = -4.37732
49 = -25
Port = "/PORT0"
3rd Order freq = 940M
1st Order freq = 900M


Periodic Steady State Response
compressionCurves
10.0
0
-10.0
-20.0
-30.0
-40.0
-50.0
Y0 (dBm)
-40.0
-30.0
-20.0
-10.0
0
10.0
prf (dBm)
Input Referred 1dB Compression = -8.28273
1st Order
Port = "/PORT0"
1st Order freq = 900M


x = 300.0000u
w = 13.0u
n = 2.5
2.571n
net46
indp
vout
gnd!
x=300.0000u
w=13.0u
s=5u
n=2.5
V15
vdc=1.2
gnd
V0
vdc=400m
r=10K
R0
vout
11.13266p
l = 48.0u
w = 48.0u
CM2
ceff=11.13266p
l=48.0u
C2
c=50f
C0
c=1m
PORT1
T8
i=349.92u
l=160.0n
nf=16
m=1
net088
w=48.0u
m=1
x = 500.0000u
w = 8u
n = 1
1.424n
net058
net044
net091
T9
i=349.92u
l=160.0n
nf=16
m=1
x = 500.0000u
w = 8u
s = 5u
n = 1
l = 50u
w = 50u
12.0022p
CM0
ceff=12.0022p
l=50u
w=50u
m=1
dualmimcap
net095
net068
x = 500.0000u
w = 8u
n = 6.5
25.989n
567.962f
l = 16.0u
w = 17.0u
CM3
ceff=567.962f
l=16.0u
mimcap
PORT0
R3
r=50
V1

Schematic



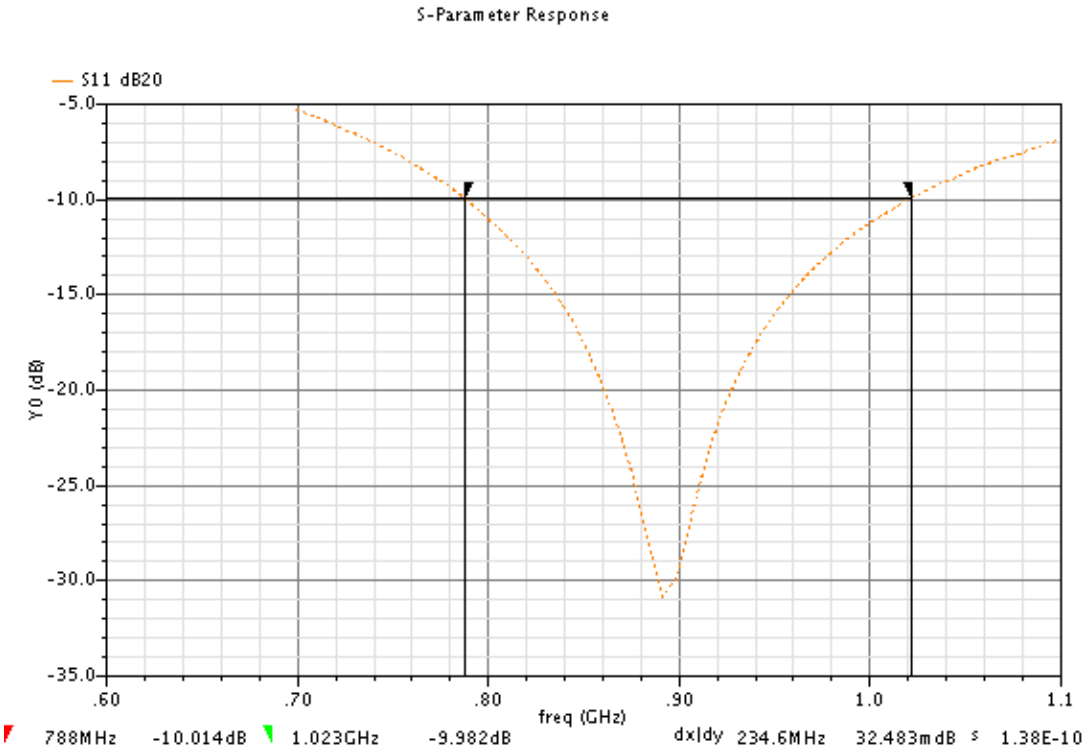
The bias voltage was set to 0.370 VDC.

Summary

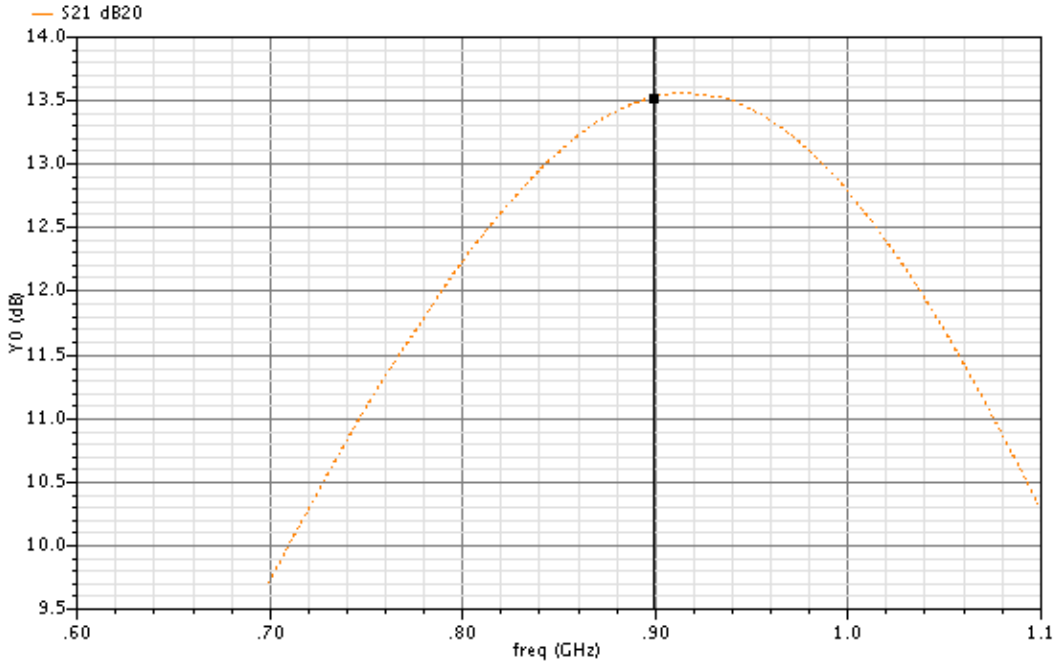
	Peak S21	3dB BW	IIP3	1 dB Compression	Power
Design	13.548 dB	225.4 MHz	-5.58	-5.75 dBm	3.953 mW
Goal	> 10 dB	200 MHz < BW < 300 MHz	> -15 dBm	>-30 dBm	< 4 mW

Frequency	S21	NF	S11
800 MHz	12.211 dB	1.3421 dB	-10.982 dB
900 MHz	13.518 dB	1.3518 dB	-29.761 dB
1 GHz	12.785 dB	1.5043 dB	-11.326 dB

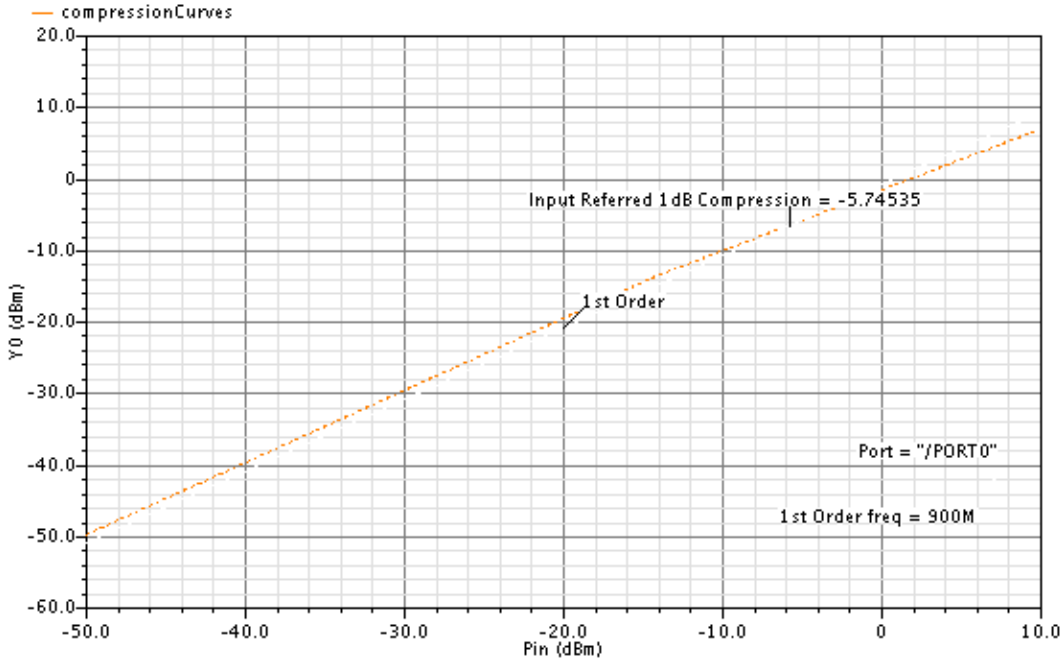
Plots



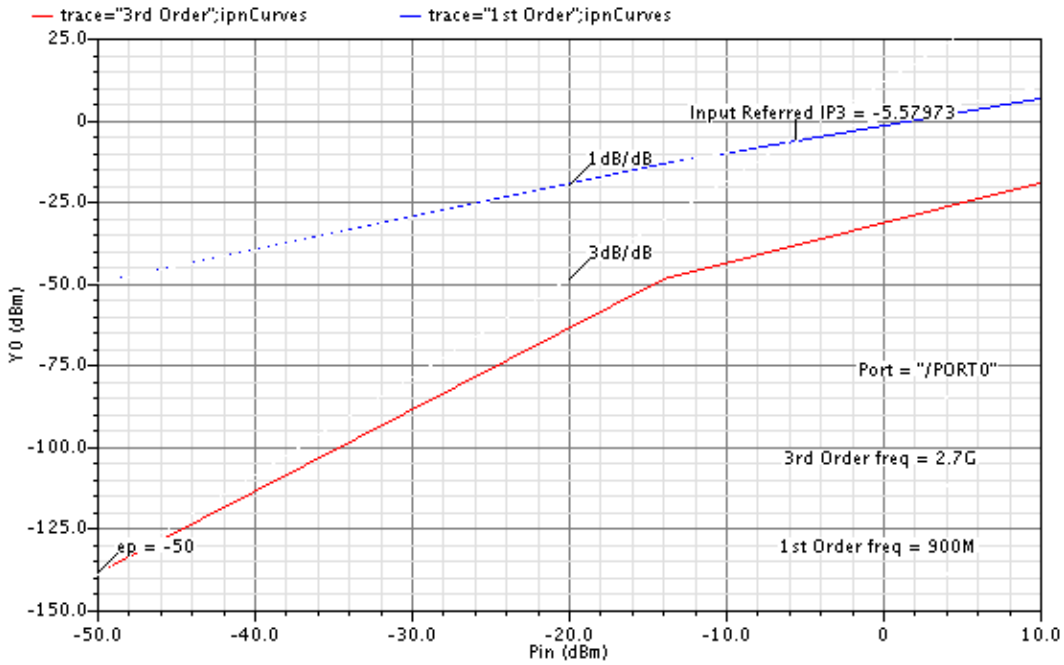
S-Parameter Response



Periodic Steady State Response



Periodic Steady State Response



S-Parameter Response

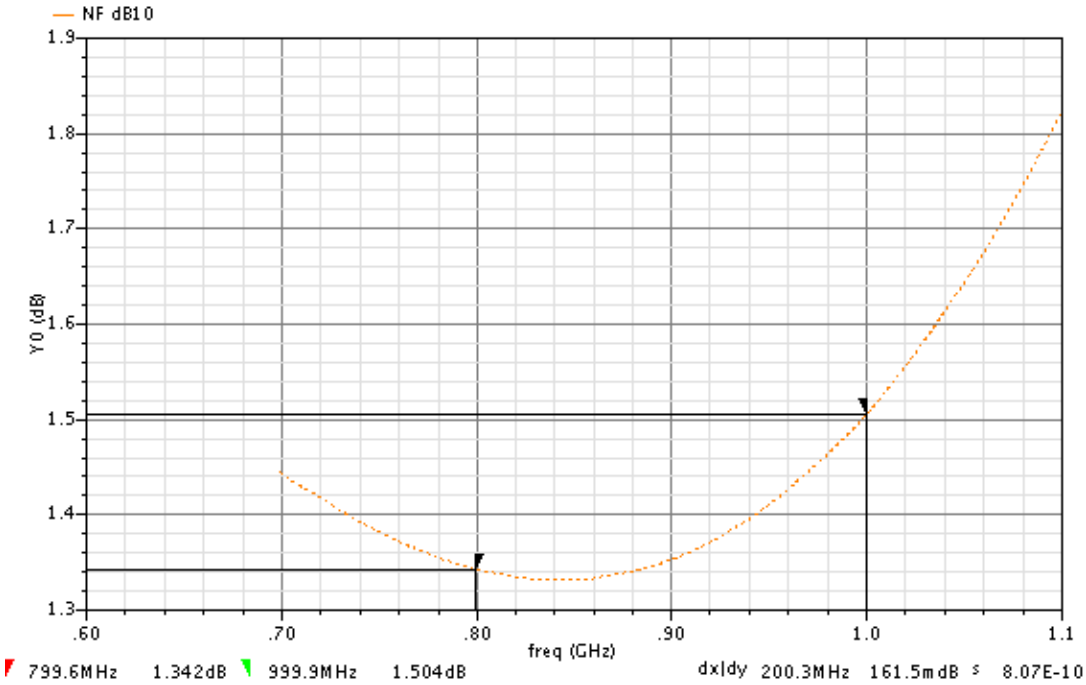
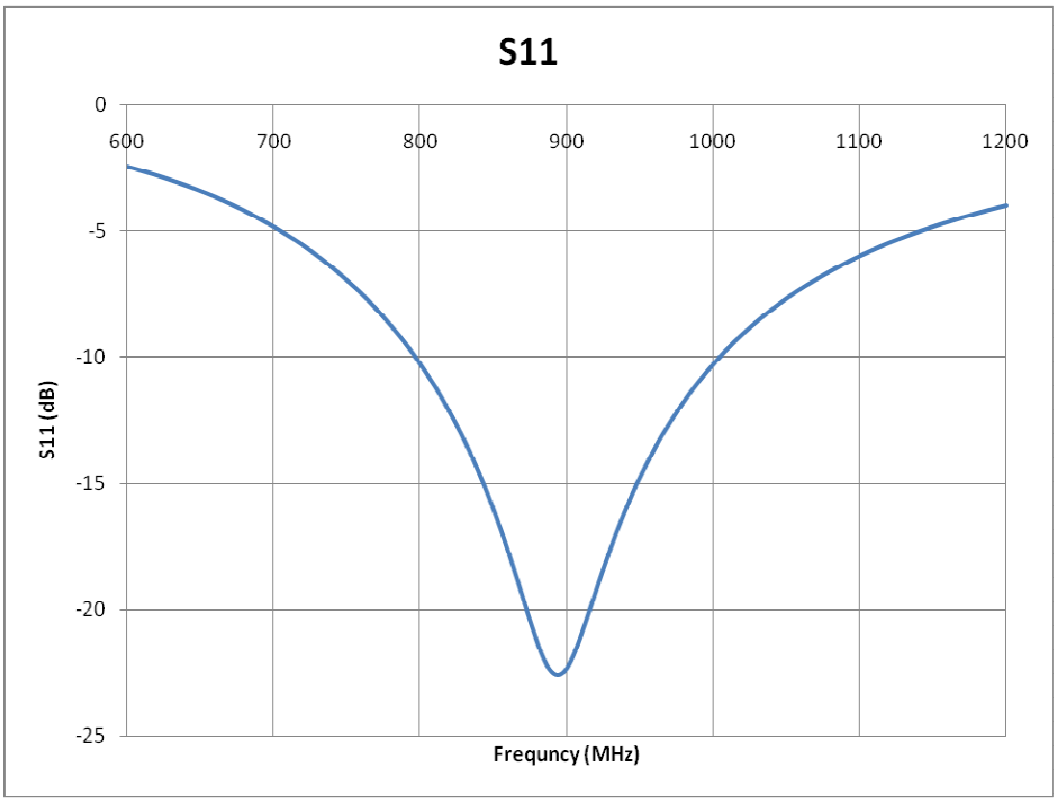


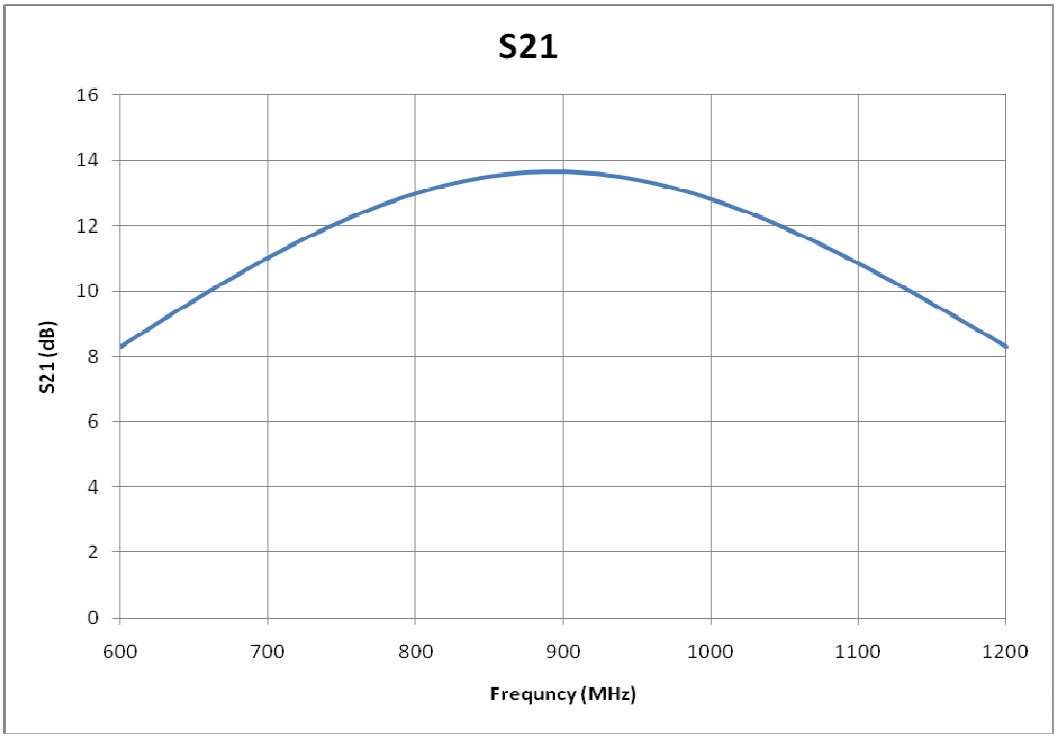
Table 1 - Specification List

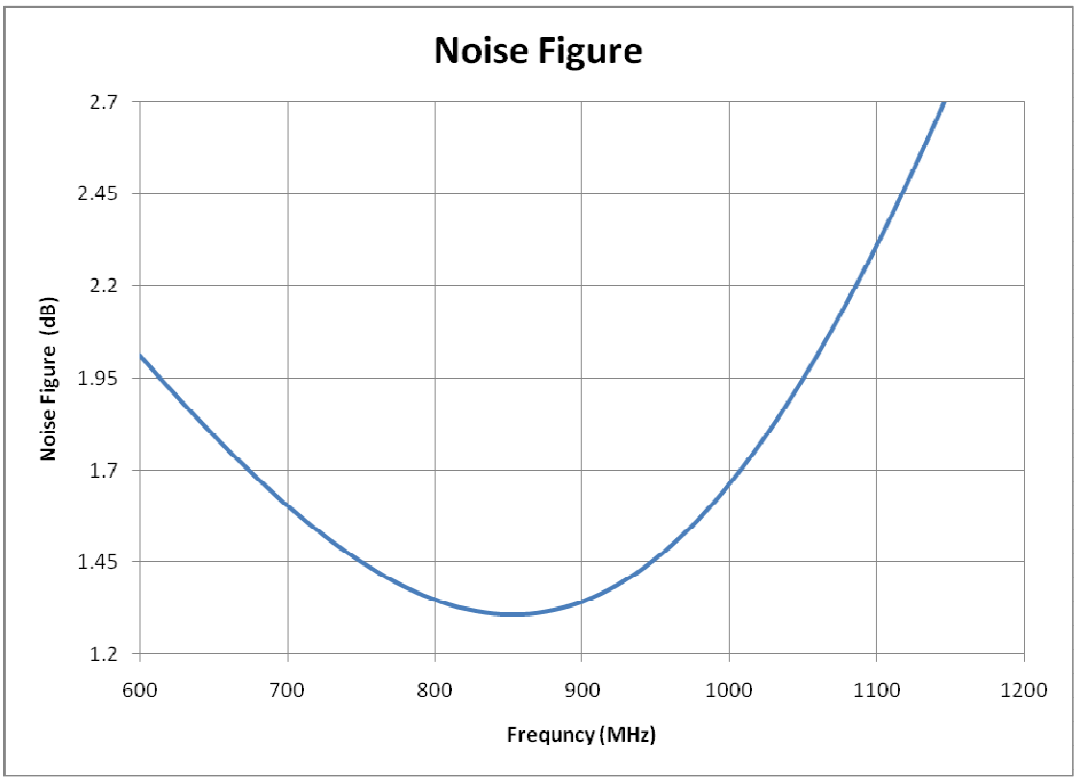
Specification	Target Value	Actual Value Lower Corner	Actual Value 900MHz	Actual Value Upper Corner
Peak S21	> 10dB	13.05 dB	13.66 dB	12.79 dB
3dB BW	200MHz < BW < 300MHz	N/A	450 MHz	N/A
Center Frequency	900MHz	N/A	900 MHz	N/A
Noise Figure	<1.7dB between 800MHz and 1GHz	1.343 dB	1.343 dB	1.675 dB
S11	<10dB between 800MHz and 1GHz	-10.62 dB	-22.32 dB	-10.14 dB
P1dB	> -30dBm	N/A	-4.63 dBm	N/A
IIP3	> -15dBm	N/A	-4.23 dBm	N/A
Power Consumption	< 4mW	N/A	3.994 mW	N/A

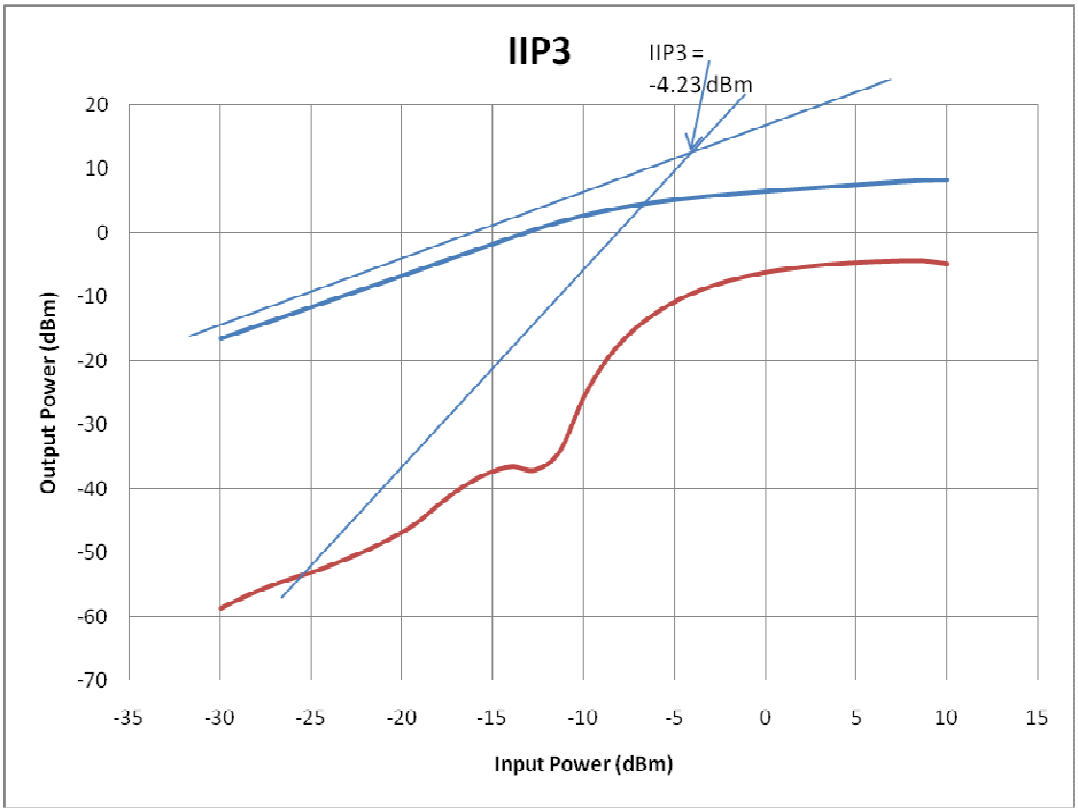
Table 2 - Component List

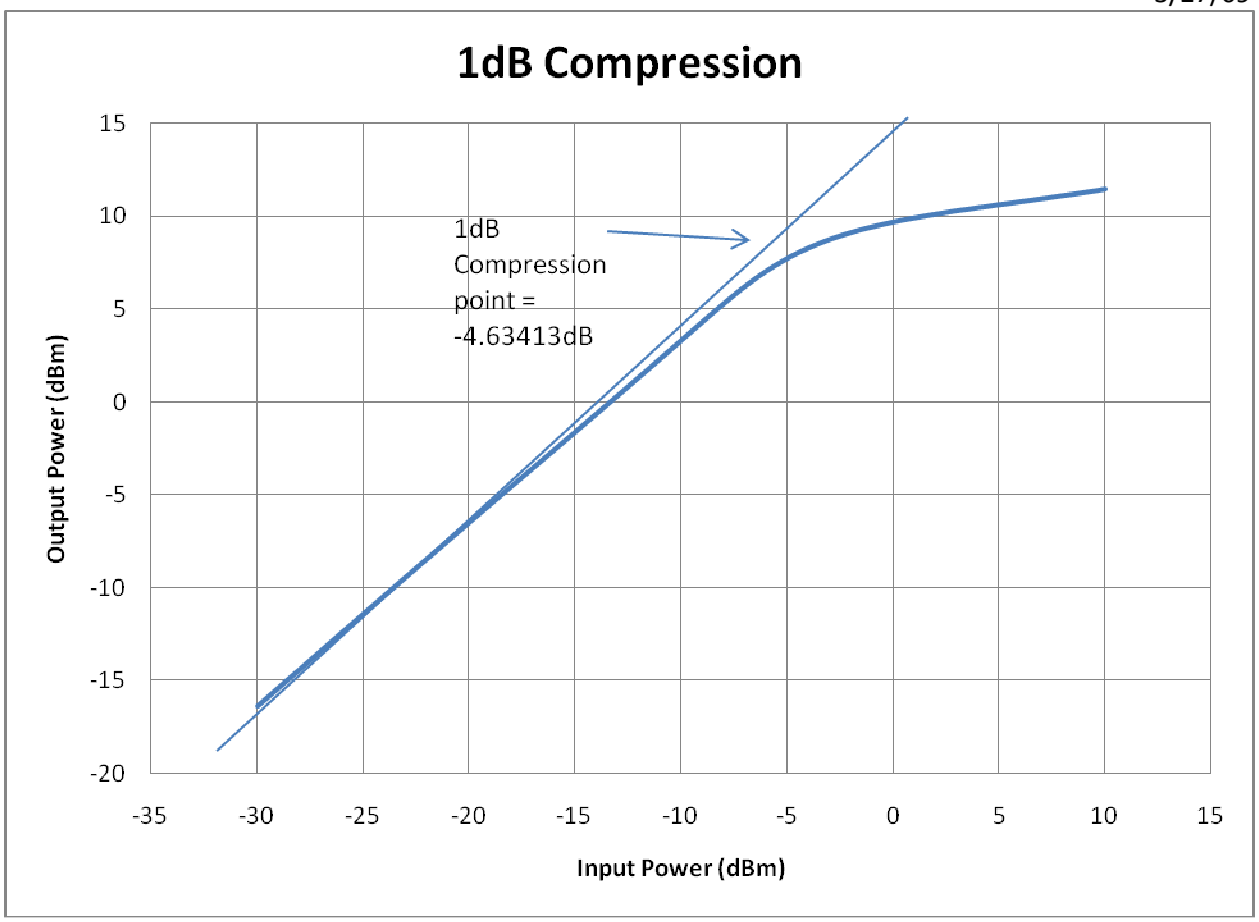
Component		**Parameters**		
		Capacitance	*Length*	*Width*
CM2	Capacitor	830.6277fF	8.5um	11.05um
CM1	Capacitor	4.999709fF	8.5um	81.71um
		Inductance	*Outer Dimension*	*n turns*
I3	Inductor	28.043nH	400um	8
I4	Inductor	1.609nH	150um	3
I5	Inductor	4.673nH	300um	3
		Width	*Length*	*# fingers*
T1	NFET	200um	150nm	8
T6	NFET	200um	150nm	8

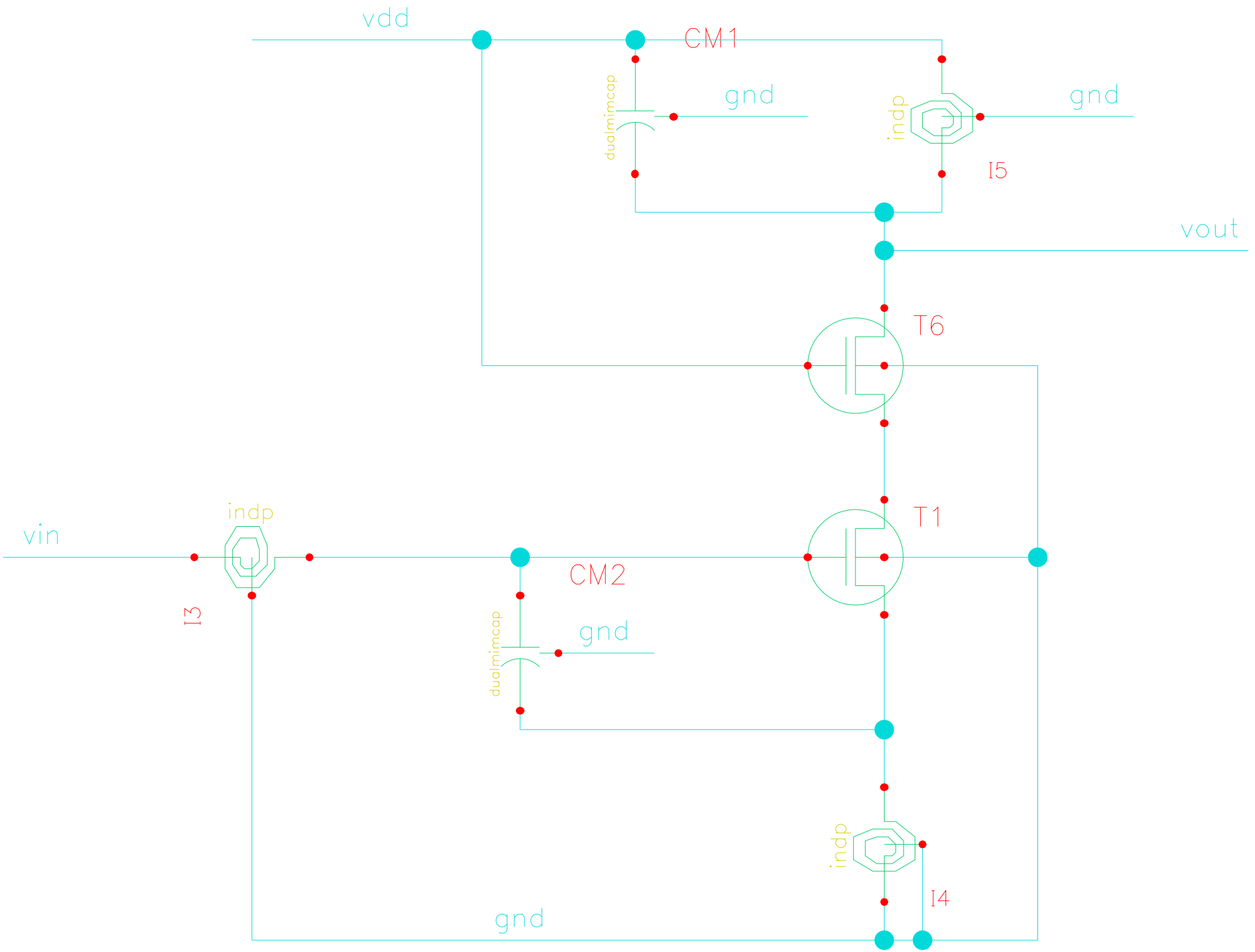

S11
0
-5
-10
-15
-20
-25
600
700
800
900
1000
1100
1200
S11 (dB)
Frequncy (MHz)


S21
16
14
12
10
8
6
4
2
0
600
700
800
900
1000
1100
1200
S21 (dB)
Frequncy (MHz)


Noise Figure
Noise Figure (dB)
2.7
2.45
2.2
1.95
1.7
1.45
1.2
600
700
800
900
1000
1100
1200
Frequncy (MHz)


IIP3
IIP3 =
-4.23 dBm
Output Power (dBm)
20
10
0
-10
-20
-30
-40
-50
-60
-70
-35
-30
-25
-20
-15
-10
-5
0
5
10
15
Input Power (dBm)


1dB Compression
1dB
Compression
point =
-4.63413dB
Output Power (dBm)
Input Power (dBm)
15
10
5
0
-5
-10
-15
-20
-35
-30
-25
-20
-15
-10
-5
0
5
10
15


vdd
CM1
gnd
dualmimcap
indp
gnd
I5
vout
T6
T1
vin
indp
I3
CM2
gnd
dualmimcap
indp
I4
gnd

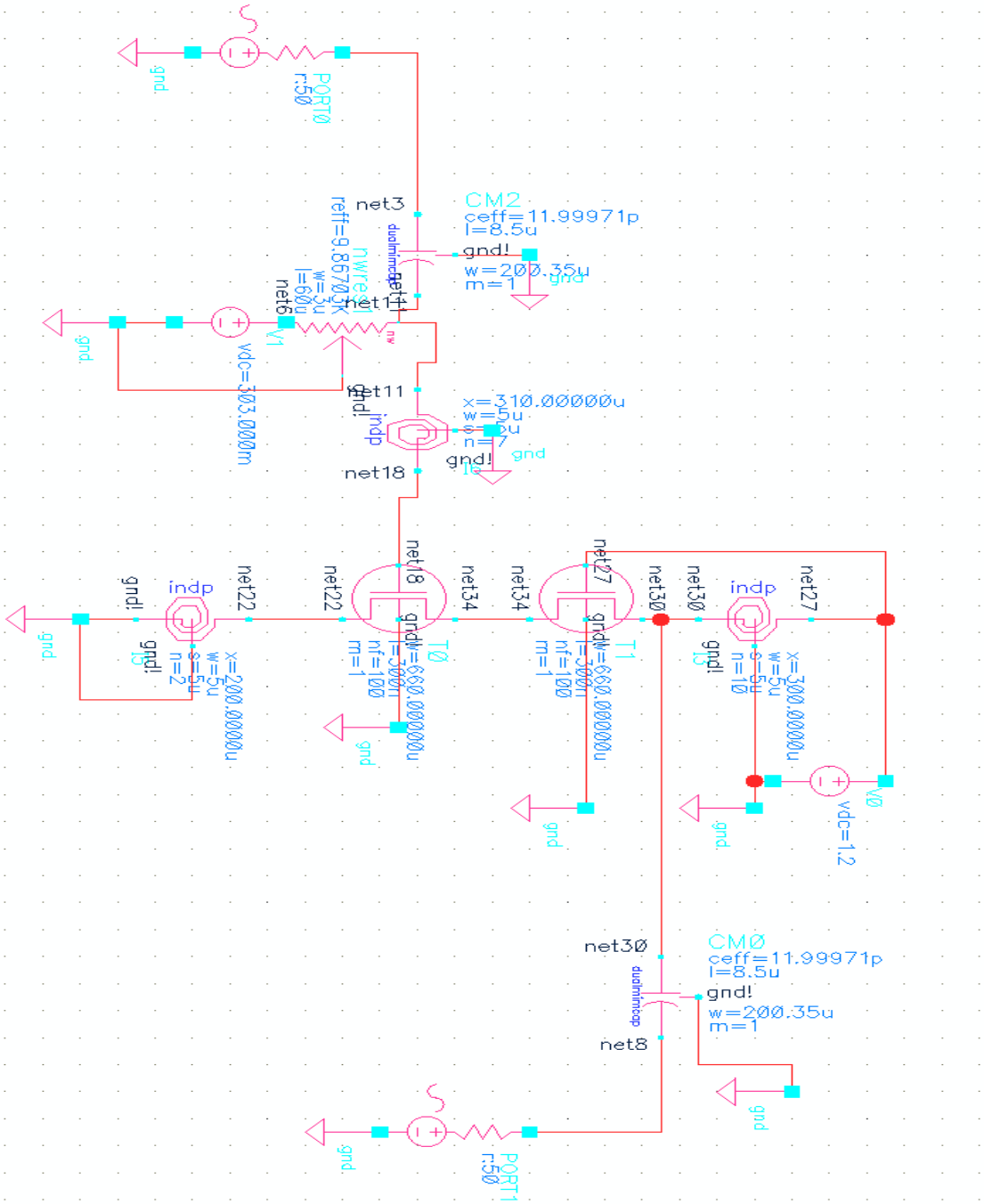


figure 4 designed circuit

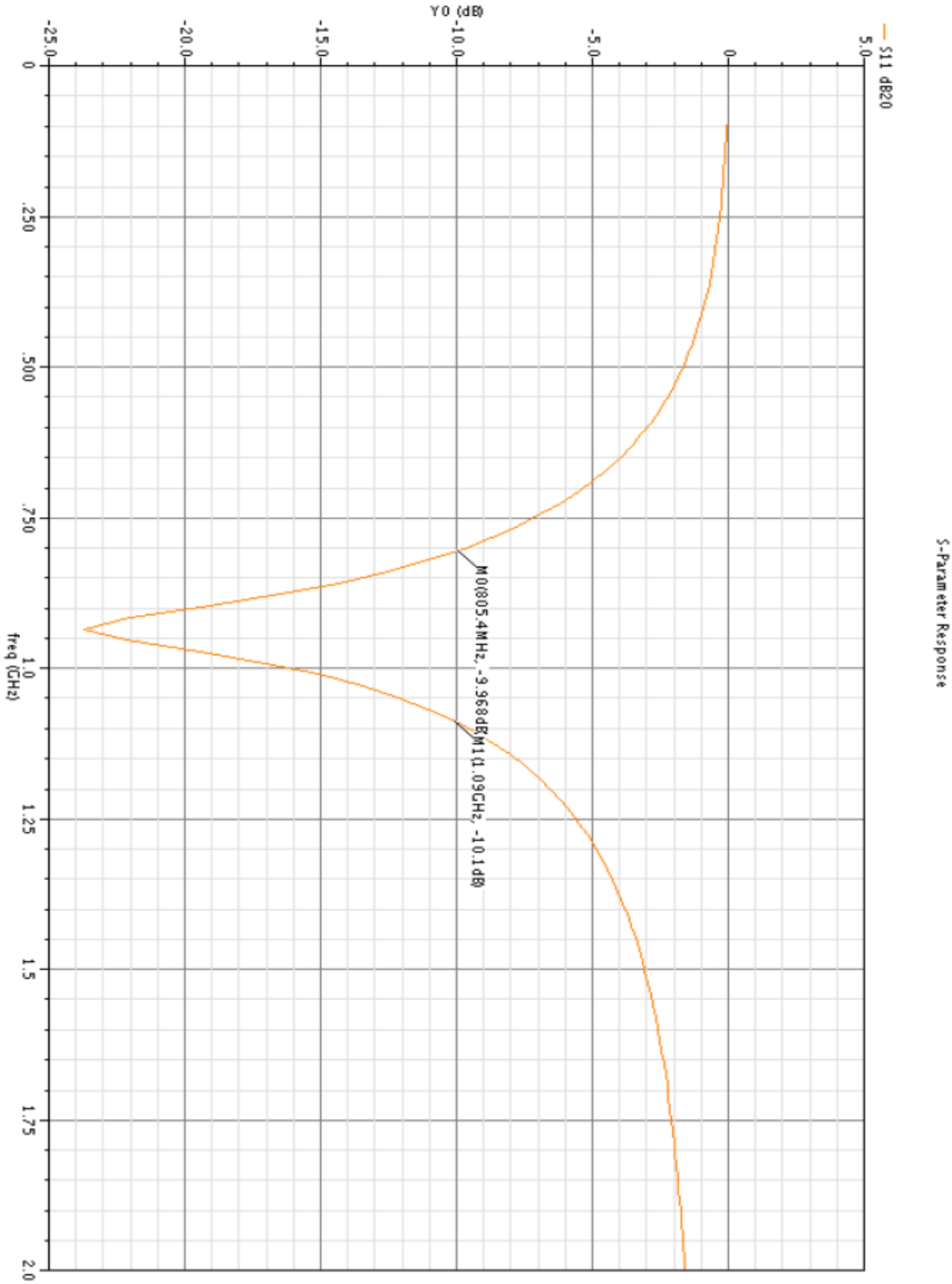


figure 5 s parameter analysis results (s11)

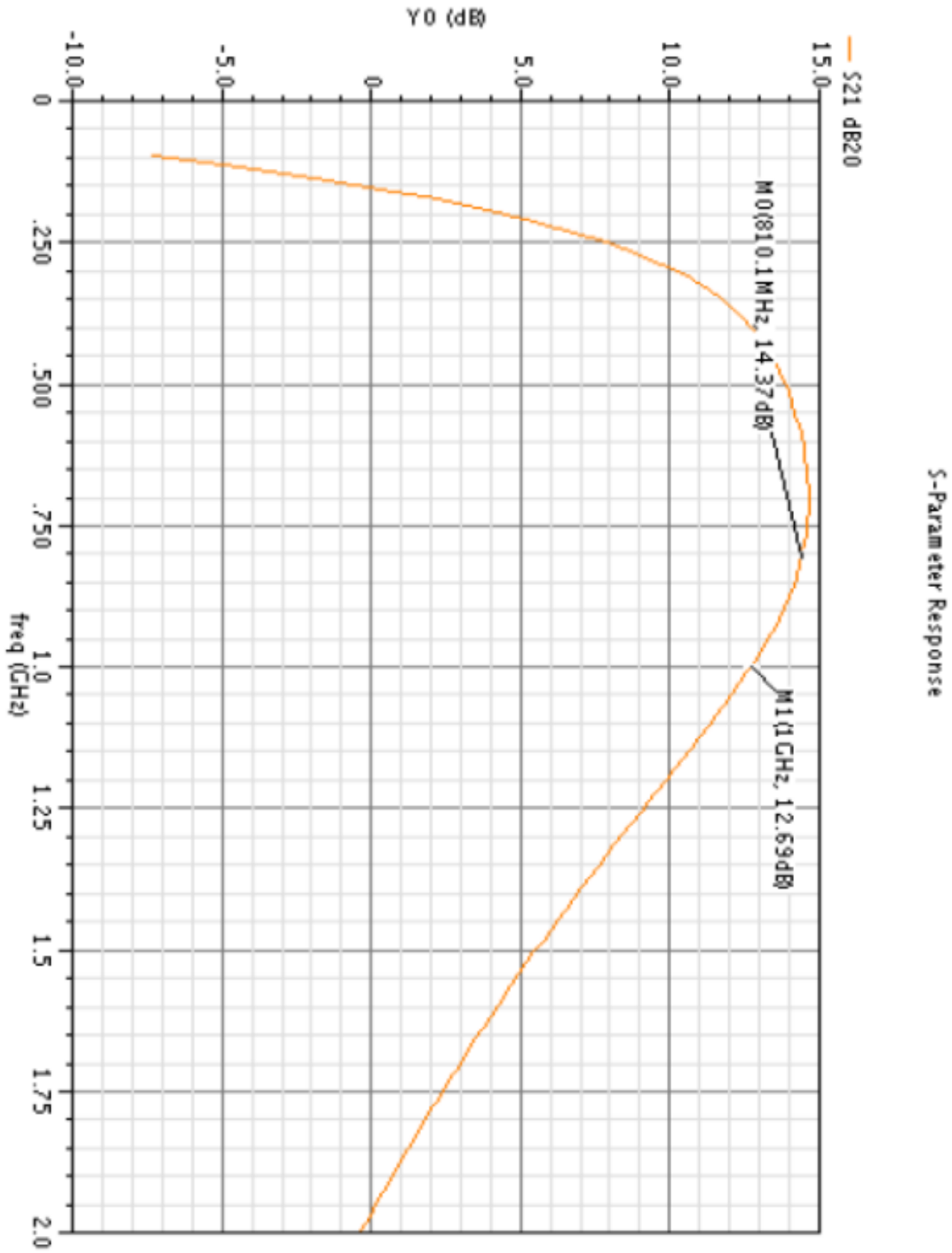


figure 6 s parameter analysis results (s21)

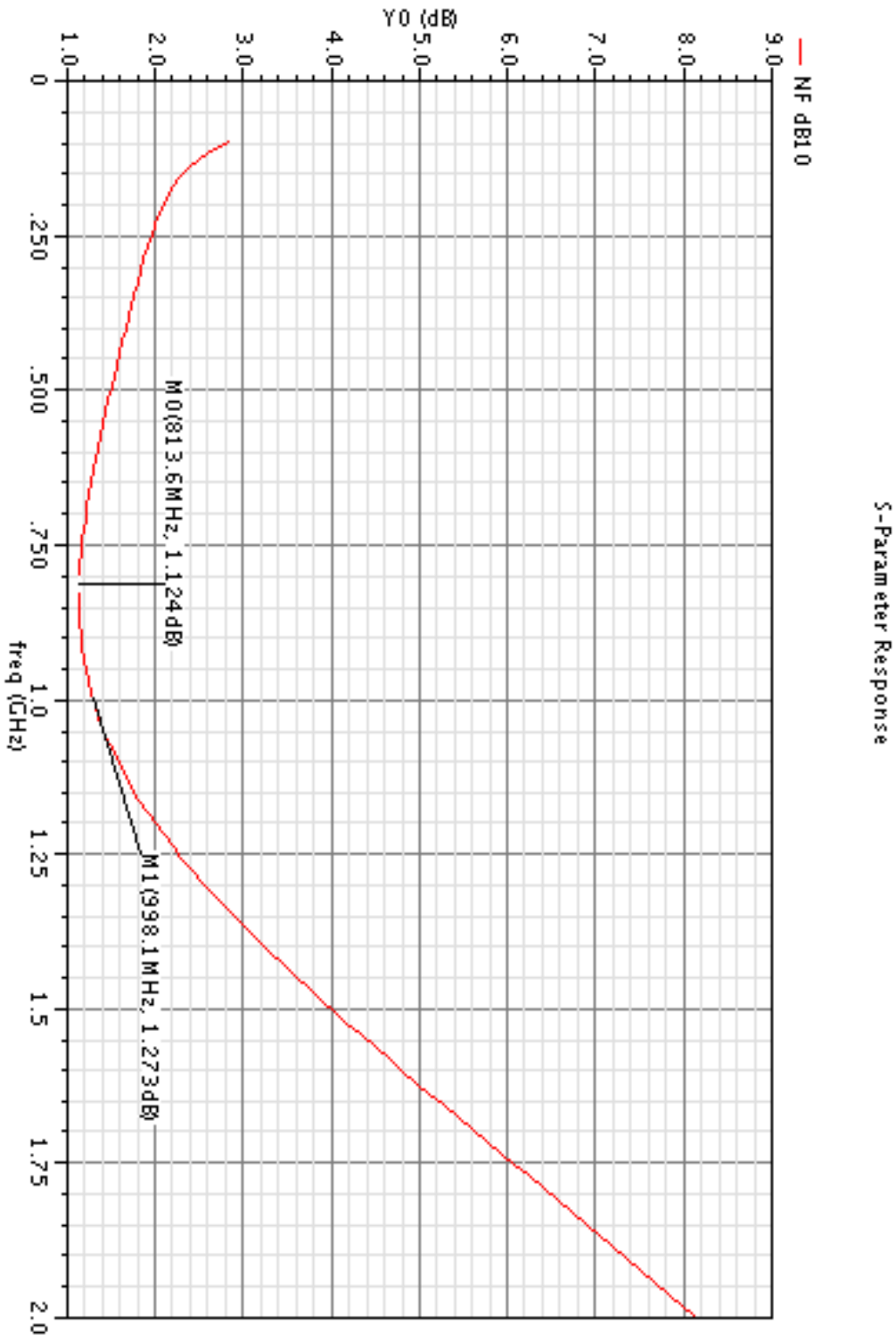


figure 7 s parameter analysis results (Noise Factor)

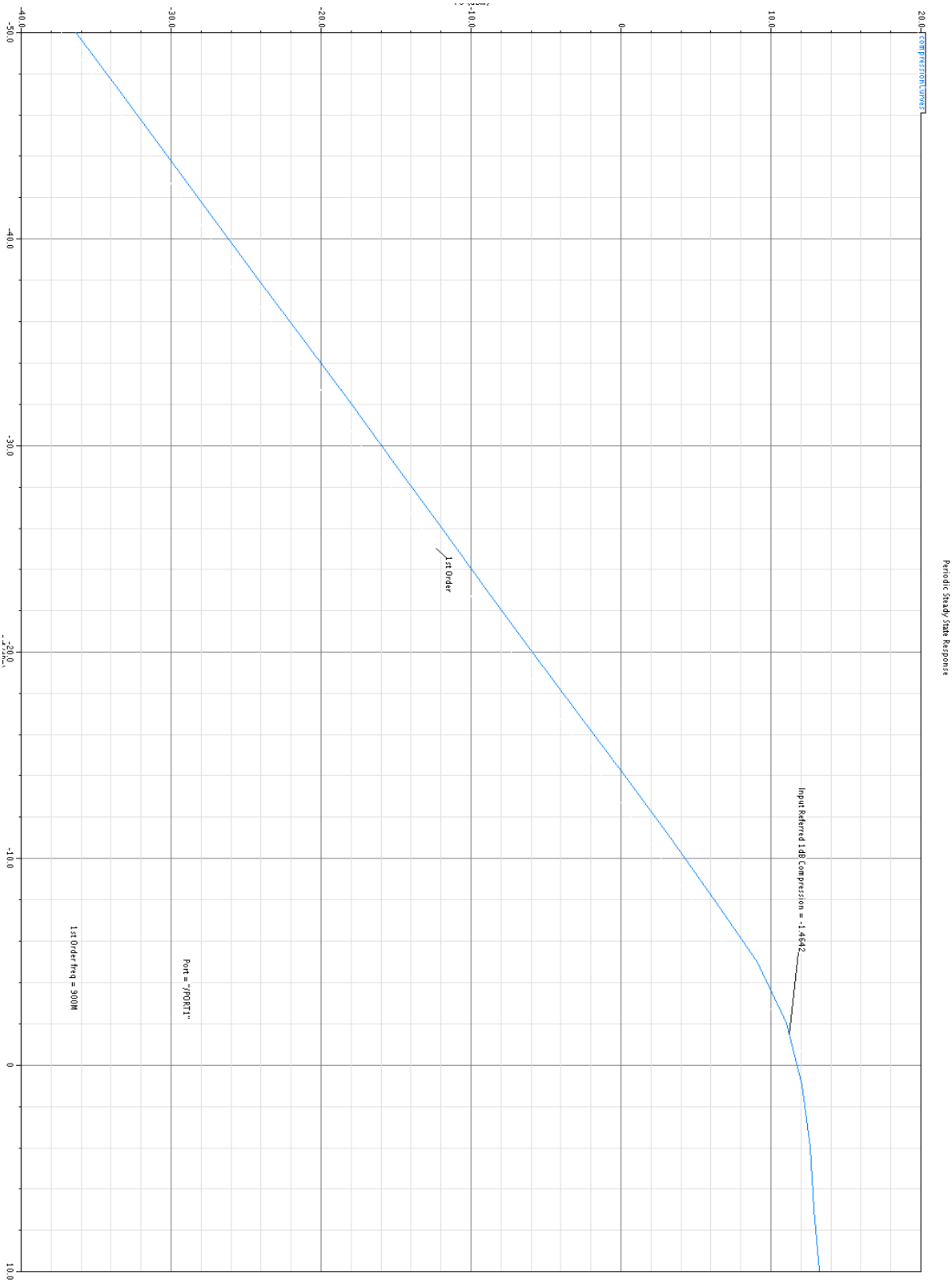


figure 6 1 dB compression point

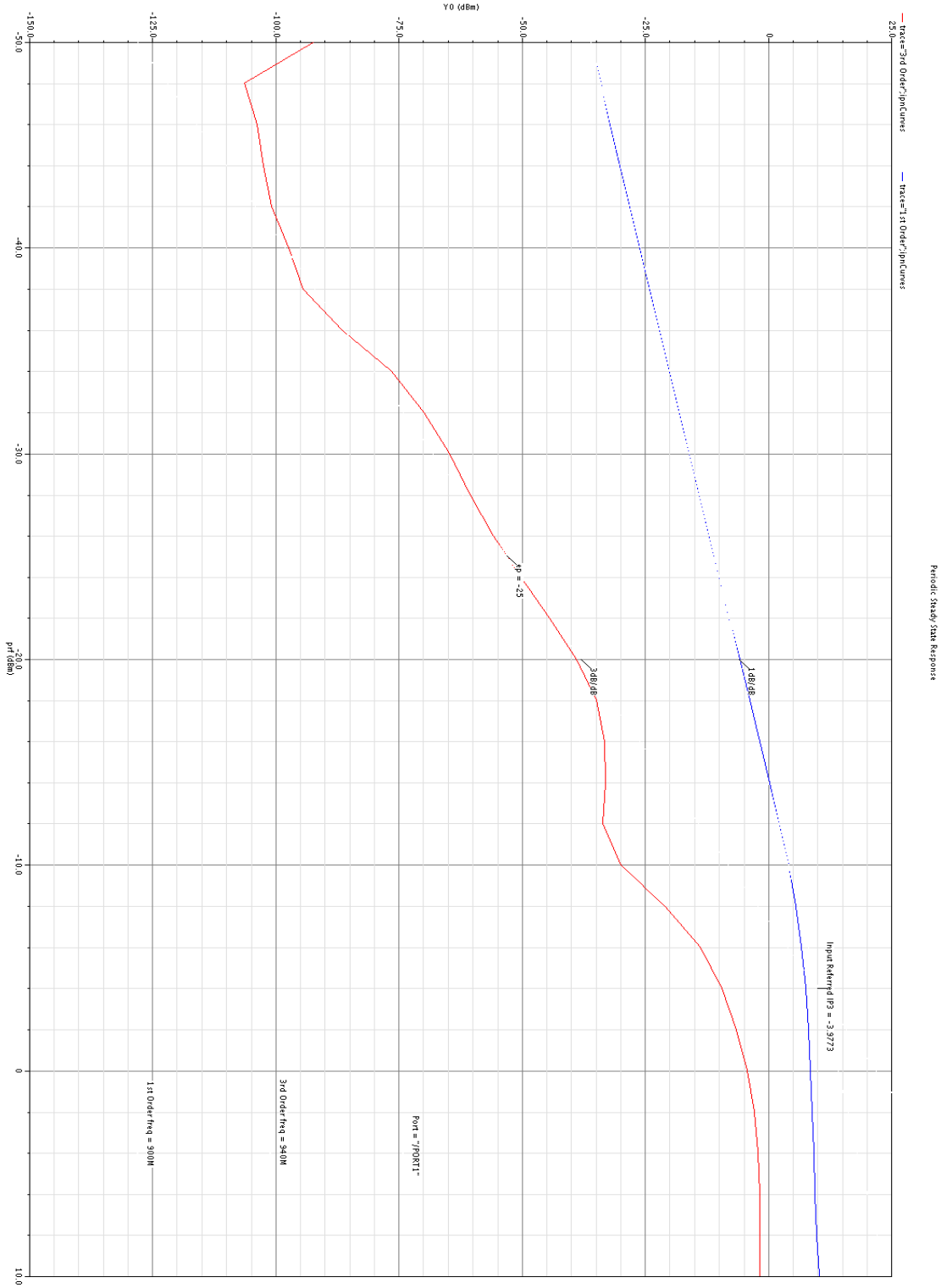


figure 7 IIP3 Point (it is -3.9 dBm, red line is 3th harmonic blue is fundamental)

3-27-09
EECS 522
CAD 2

EECS 522 CAD Assignment #2

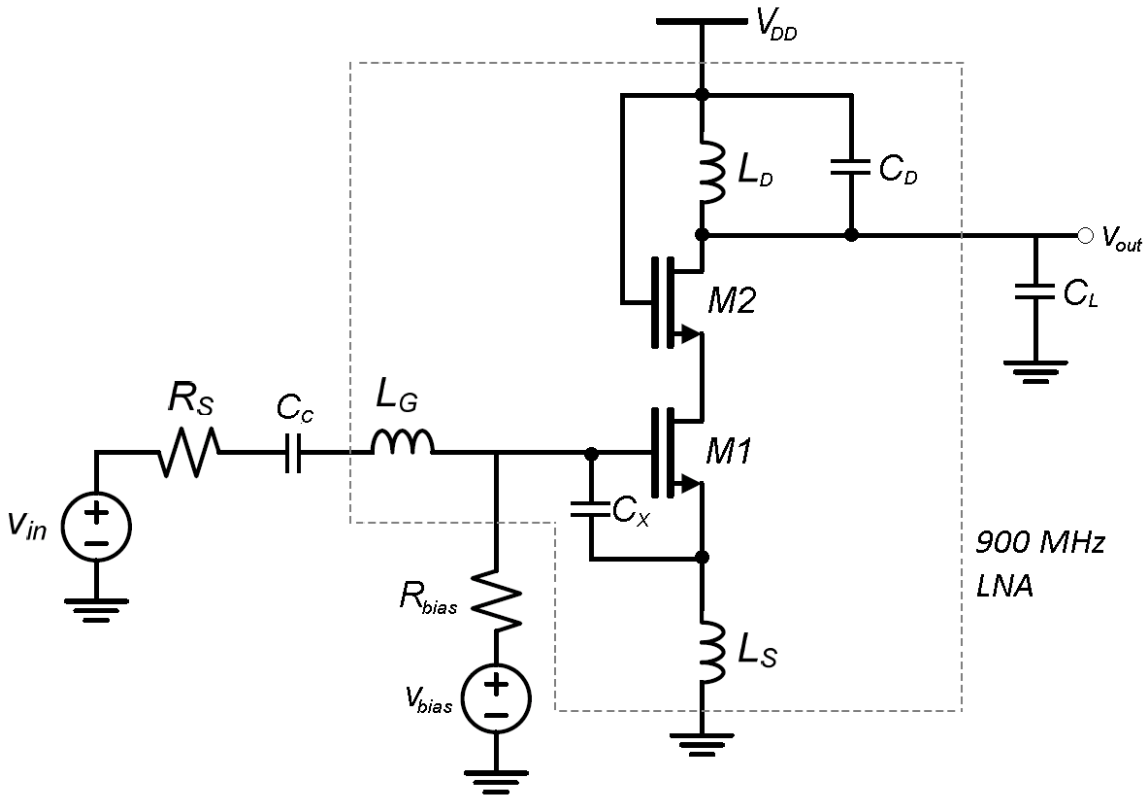


Figure 1. Schematic of 900 MHz LNA Including Given Components

Device Values and Sizes:

Given Devices:
R_S = 50 Ω
R_{bias} = 10 k Ω
C_C = 12 pF
C_L = 50 fF
V_{DD} = 1.2 V
V_{bias} = 397 mV

Inductors:

	Inductance	Outer Diameter	Metal Width	Number of Turns
L_G	23.075 nH	470 µm	11 µm	7.5
L_S	1.025 nH	400 µm	10 µm	1
L_D	2.266 nH	290 µm	15 µm	2.5

Capacitors:

	Capacitance	X-Dimension	Y-Dimension
C_X	709.6945 fF	50 µm	6.75 µm
C_D	11.60083 pF	200 µm	28.12 µm

Transistors:

	Width of Single Finger	Width of All Fingers	Length	Number of Fingers
M1	15.21 µm	380.25 µm	160 nm	25
M2	15.21 µm	380.25 µm	160 nm	25

Summary Table:

Specification	Desired Value	Measured Value
Peak S21 (Gain)	> 10 dB	13.378 dB
3dB Bandwidth	200 MHz < BW < 300 MHz	297.14 MHz
Center Frequency	900 MHz	900 MHz
Noise Figure	< 1.7 dB between 800 MHz and 1GHz	< 1.637 dB between 800 MHz and 1 GHz
S11	< -10 dB between 800 MHz and 1 GHz	< -10.17 dB between 800 MHz and 1 GHz
P1dB	> -30 dBm (input referred)	-2.525 dBm
IIP3	> -15 dBm (input referred)	-7.037 dBm
Power Consumption	< 4 mW	3.913 mW

Plots:

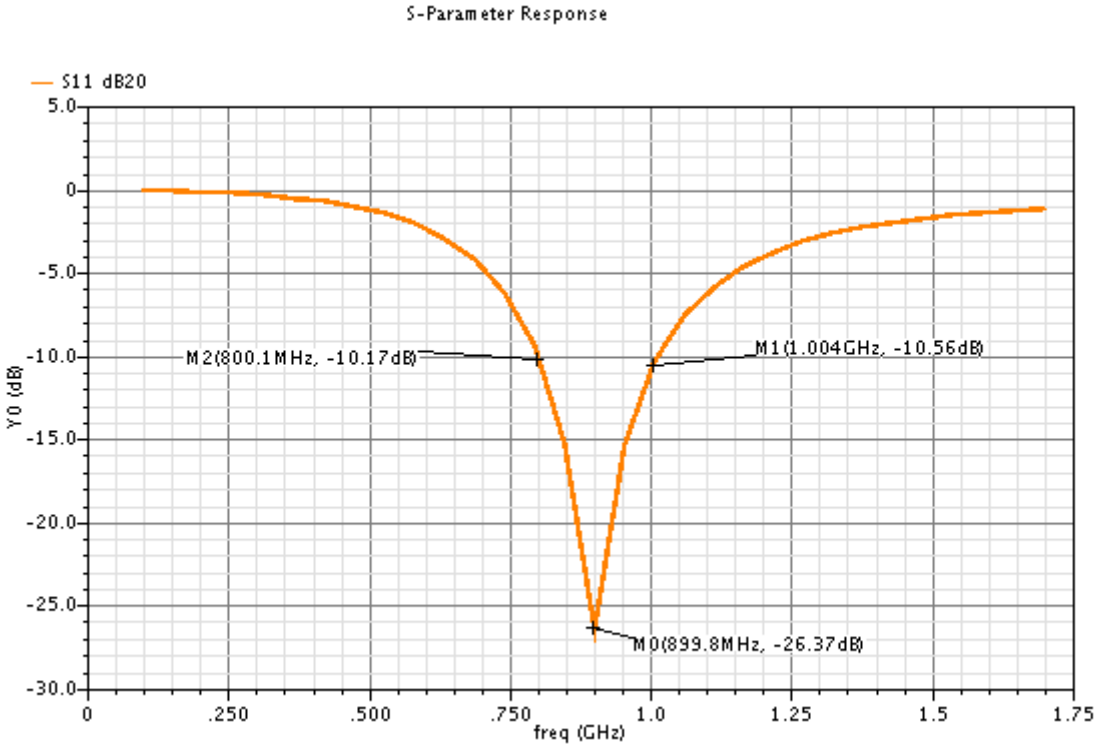


Figure 2. Plot of S11

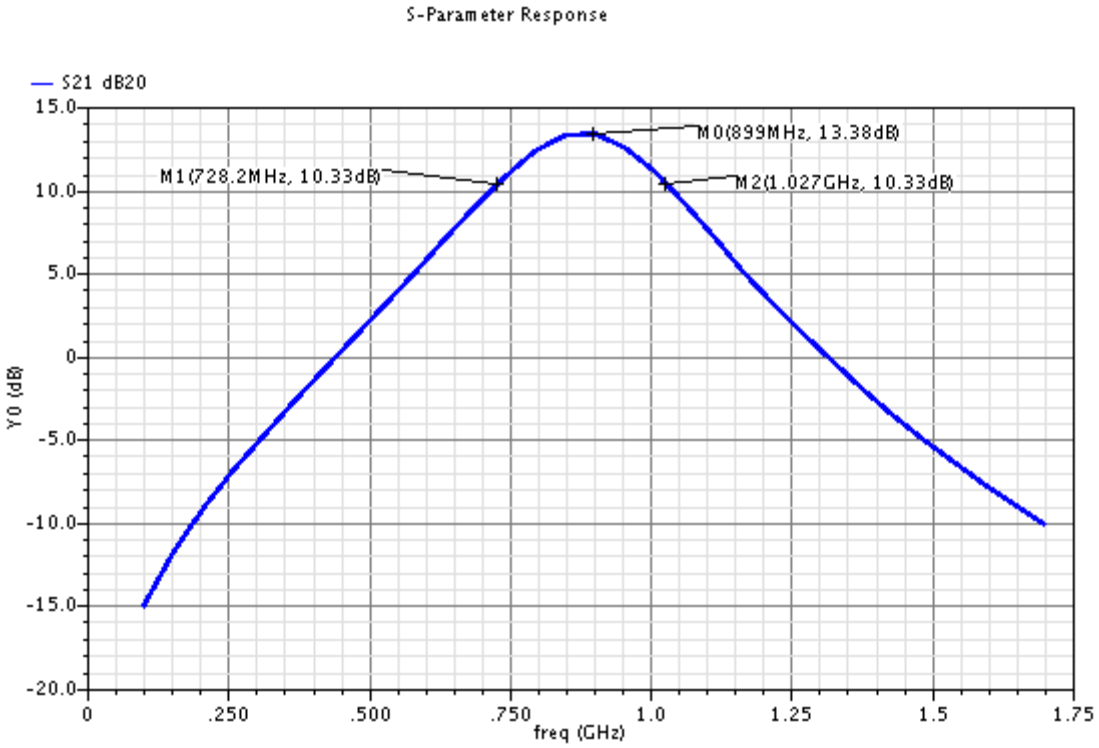


Figure 3. Plot of S21

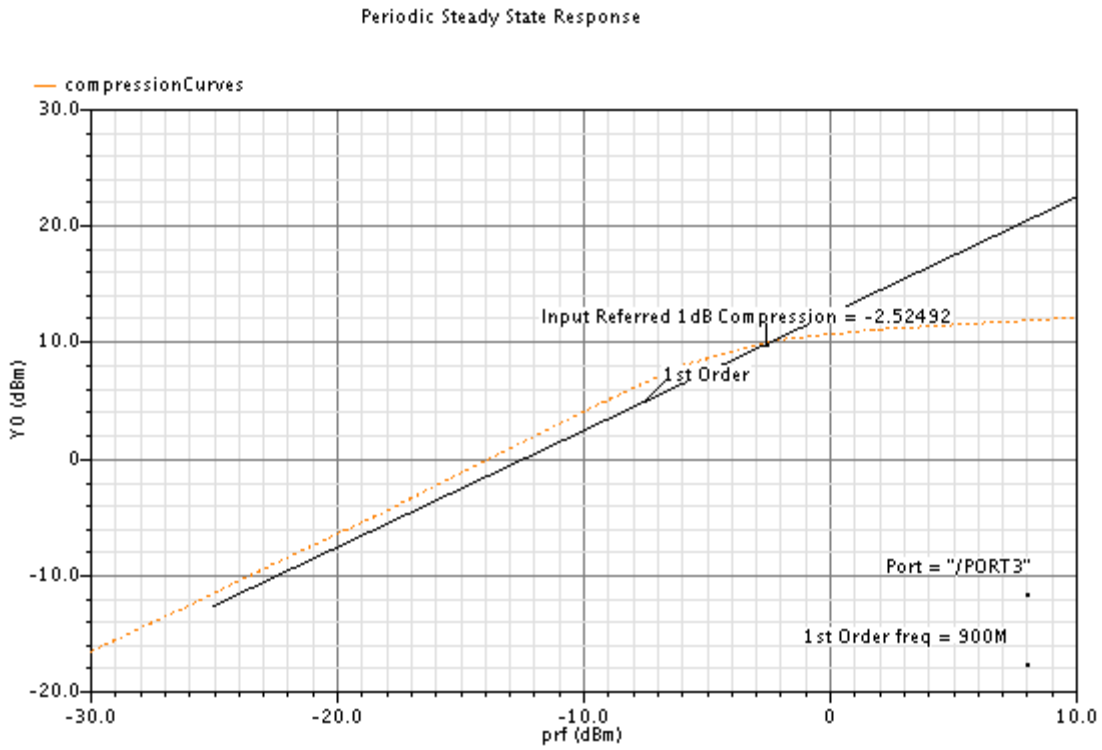


Figure 4. Plot of P1dB

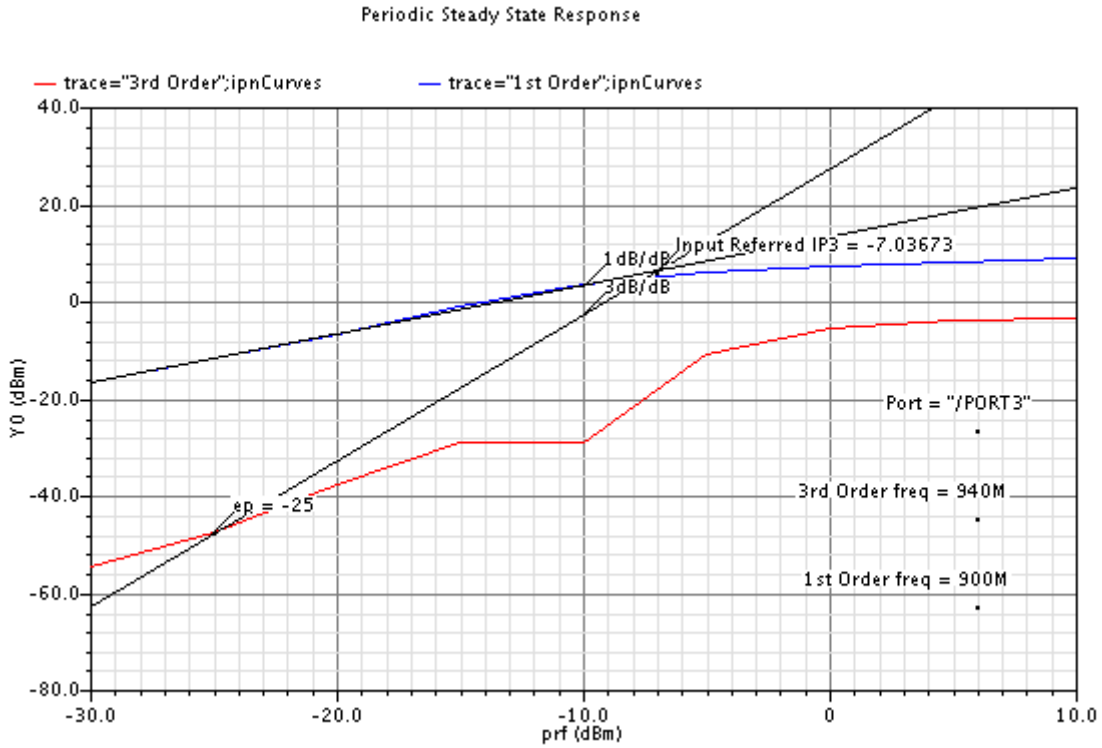


Figure 5. Plot of IIP3

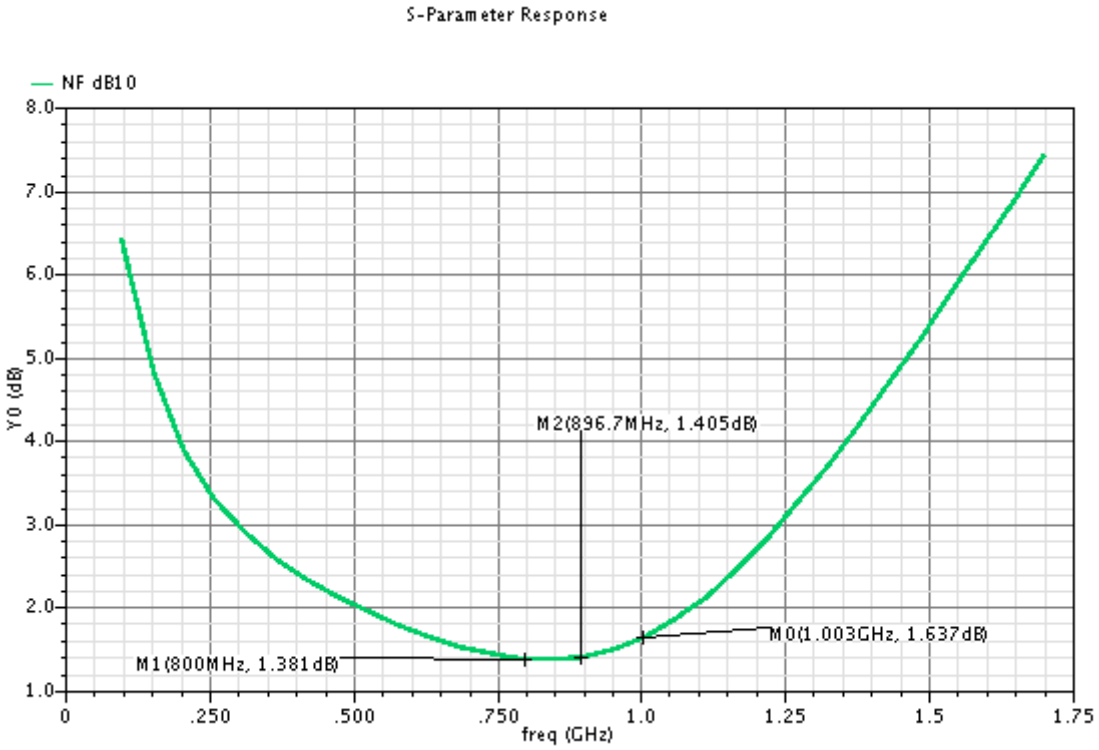


Figure 6. Plot of Noise Figure