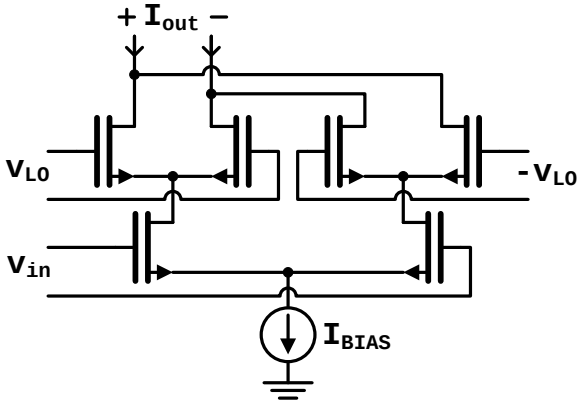
University of Michigan
EECS 522: Analog Integrated Circuits
Winter 2009

Problem Set 7

Issued 4/1/2008 – Due 4/8/2008

Problem 7.1: For this problem, assume the LO is a square wave at 900MHz, and the RF signal is a tone at 1GHz.



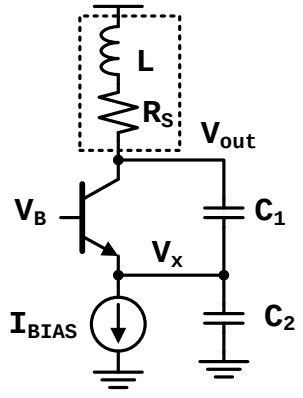
a) Considering only the first harmonic component of the LO signal, what frequencies appear at the output of the mixer? Assume the mixer is perfectly balanced.

b) Derive an expression for the conversion gain of the mixer from the RF signal to the desired component at IF.

c) Now introduce a phase offset between the LO applied to the left and right mixers of $\Delta\theta$. Assume $\Delta\theta$ is small. Derive an expression for the output amplitude of the LO leakage at 900MHz as a result of the offset.
Hint: $cos(A + \Delta) \approx cos(A) - \Delta sin(A)$ for small Δ.

d) Using your expression for conversion gain from part b), find an expression for the ratio of LO leakage amplitude to IF signal amplitude in dBc. Assuming $G_m v_{in} = 1\%$ of I_{BIAS} for good linearity and $\Delta\theta = 2\pi/100$ (1%), what is the required slope of the IF filter in dB/decade to attenuate the LO signal to -40dBc below the IF signal level?

Problem 7.2: You may neglect r_o and base current ($\beta = \infty$) for this problem.

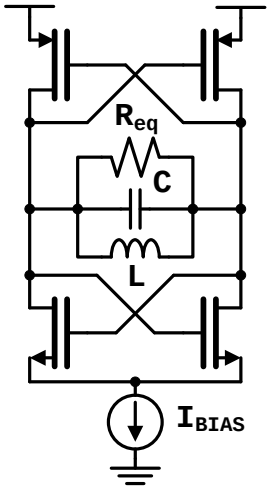


a) Simplify L, C_1, and C_2 into an equivalent parallel RLC tank. Use the series-to-parallel resistance transformations discussed in lecture to find an expression for the equivalent loss R_{eq} of the parallel tank. Assume a series loss in the inductor R_S, and an inductor $Q_L = 10$. Do not neglect the impedance on node V_x in your expression for R_{eq}.

b) Derive an expression for the oscillation frequency.

c) Now incorporating the small-signal model of the BJT, derive an expression for I_{BIAS} that biases the oscillator just at the edge of oscillation. To simplify your expression, use the definition $n = C_1/(C_1 + C_2)$.

Problem 7.3: For this problem, assume L and C are lossless, and all losses are modeled by R_{eq}.

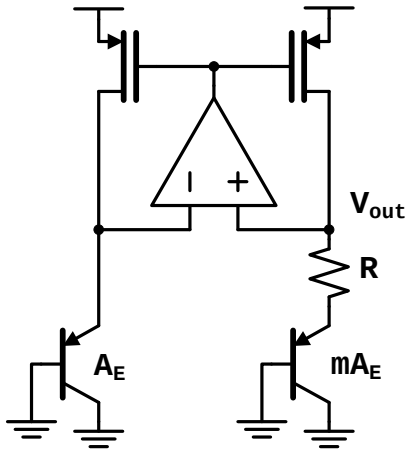


a) Derive and expression for the differential amplitude of the fundamental oscillation across the tank. Assume all higher-order harmonics are perfectly filtered by the tank.

b) Replace the NMOS devices with NPNs. Explain how the amplitude is limited by the parasitic diodes in the BJTs. How would you modify the circuit to eliminate this limitation?

Problem 7.4: This problem refers to the bandgap reference and corresponding expression for $\partial V_{BE}/\partial T$ shown in Lecture 22.

a) Assuming V_{G0} = 1.2V, V_{BE} = 750mV at 300K, and from simulation, the exponent of I_S temperature dependency r = 2. What is the value of n, the exponent of I_C temperature dependency, determined by the circuit on the right?



b) Using your answer from part, calculate $\partial V_{BE}/\partial T$ at 300K and determine the value of m (BJT area scaling ratio) to cancel this slope.

c) Now assume the resistor has a temperature dependency, typically proportional to $\sqrt{T}$. What is the new value of n, the exponent of I_C temperature dependency, and new value of $\partial V_{BE}/\partial T$?

d) Using your value of m from part b), and the value of $\partial V_{BE}/\partial T$ from part c) calculated at 300K, what is the error voltage at V_{out} at 0°C and 85°C, the extremes of the commercial temperature range?

Problem 7.5: Use Cadence to solve this problem.

a) Build a schematic in Cadence of an nfet_rf with W=1um, L=130nm. Include independent gate and drain bias voltage sources. Include a transient sinusoidal source at the input.

b) Simulate the 1dB compression point of the short-circuit output current to a sinusoidal input voltage at a frequency of 10MHz. Bias the transistor at three separate current densities: 25uA/um, 75uA/um, and 200uA/um. This corresponds to alpha of 1, 0.75, and 0.5. For each bias point, set the drain bias voltage to the gate voltage for the corresponding current density. Hand in a plot of the output current showing the 1dB compression point for the three bias points.

c) Simulate the OIP3 of the short-circuit output current to a sinusoidal input voltage at frequencies of 10MHz and 10.1MHz. Bias the transistor at the same current densities and drain voltages as part b): 25uA/um, 75uA/um, and 200uA/um. Hand in a plot of the output current showing the OIP3 point for the three bias points.