Cadence Tutorial 2: Layout, DRC/LVS and Circuit Simulation with Extracted Parasitics

Introduction

This tutorial describes how to generate a mask layout in the Cadence Virtuoso Layout Editor. Use of DIVA for layout verification will also be covered along with instructions on how to resimulate your design with extracted parasitics in Spectre. In the first section, you will generate a layout for a simple CMOS inverter. In the second, you will create an AND gate using the inverter and a standard cell NAND. You may use the standard cells in later assignments for the digital portions of your circuits. The inverter, although digital, will be treated like an analog block in this tutorial in order to demonstrate how to handle both digital and analog blocks in the design flow.

Setup

When doing layout, a techfile must be attached to the library. This defines layers, parameterized cells (pcells) and other layout-related technology information. To do this, start icfb in your CAD directory by typing the following:

cd ~/eecs522/CAD source .cshrc_ibm_13 icfb &

then, open the Library Manager from the CIW with:

Tools > Library Manager

Right click on the *tutorial* library that was created in the first tutorial and choose *Properties*. Enter *cmrf8sf* in the textbox for techLibname and click on OK. You have now attached the techfile. In the list of cells, click on *cmos_inverter*, then choose:

File > New > Cell View

Select *Virtuoso* as the Tool. The View Name should automatically change to *layout* if you click in a different field. Click Ok (click Ok once again if an ensuing pop-up "Add AMS..." appears). A Virtuoso Layout window will now open. Before entering any layout, set the grid with:

Options > Display

Change the X and Y Snap Spacings to .01 and click on Ok. Turn Gravity off by typing the "g" key. With gravity on, the cursor will snap to objects, making it difficult to perform portions of the layout entry.

Layout: Creating Devices

Begin by adding an instance of an nfet transistor. This is done by choosing:

Create > Instance

in the layout window. Browse the cmrf8sf library and select nfet cell, with the layout view. The Create Instance window will now show parameters specific to this cell. We want to set the dimensions of this nfet to match the cmos_inverter schematic created in the first tutorial. Change the width to 400 nm and the length to 1200 nm. Place an instance of this cell by moving the cursor over the layout window and clicking LMB. Now, browse for the pfet cell, again with layout view. Change the width to 1 um and the length to 120 nm.

Layout, DRC/LVS, and Extracted Parasitics

Also, click on the "Add nw contact?" checkbox. This will place a bulk connection automatically. Add an instance of this pfet to the layout. Other than width and length, you won't need to consider most of the other parameters in the Create Instance pop-up. You may find occasional use for the *number of fingers* parameter. This is useful in generating layout for wide transistors by instantiating multiple devices (for eventual parallel connection) whose widths add to the final intended width.

To see the complete layouts for the instantiated devices, press Shift-F. If you later wish to view only the top-level layout data, press Control-F.

Layers

At this point you can see a variety of shapes on different layers that form the nfet and pfet cells. You will use some of these layers when connecting terminals of the devices and adding pins. The complete set of layers available to you is shown in the LSW window which appears when opening a layout view. The primary layers you'll be using are described in Table 1:

Layer Abbrev.	Layer Name	Color	Primary Function	
M1	Metal 1	Blue	first level of metal used for device interconnection	
PC	Poly	Red	forms transistor gate when crossing diffusion; short interconnect	
RX	Diffusion	Green	defines active areas for transistor formation as well as substrate and well contacts	
CA	Contact	Yellow	defines oxide cut for M1 connections to RX or PC	
NW	N-Well	Yellow	pfet devices will reside in n-well	
BP	P+ implant	Brown	defines p+ regions for pfets and substrate contacts	
V1	Via	Yellow	defines oxide cut for M2 connections to M1	
M2	Metal 2	Magenta	second level of metal used for further connections	

Table	1:	Primary	Mask	Layers
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The IBM 0.13um technology supports up to six levels of metal for interconnect, each with a respective via to the layer below. Check with your instructor to see how many layers are available to you in your assignments.

Design Rules

There are various inter/intralayer rules to follow to ensure reliable fabrication of the circuit. A list of these design rules can be found in the following document:

/usr/caen/generic/IBM_13_KIT/IBM_PDK/cmrf8sf/relDM/doc/cmrf8sf.design_manual.pdf

There are many rules for this technology but not all will be relevant to your designs. Still, the first few cell layouts you complete will be painfully slow to do until you become more familiar with the most common rules. Each layer will have a minimum width and space associated with it. Vias and contacts will differ in that they will be of fixed size. There are also spacing rules between shapes on different layers (e.g. diffusion to n-well edge or metal overlap of contact).

Layout: Interconnect and Pins

There are many ways to go about placing the nfet and pfet and wiring the terminals together to form the inverter layout. One way to do this is shown in Figure 1. Vdd runs horizontally on top in M1. Gnd is on the bottom, running horizontally in M1. Vin comes in from the left and vout comes out from the right, both in M1. Use this example for your layout. Don't be concerned about matching the dimensions. You can move the devices instances (or any other object you create) by first selecting the device with the LMB, then clicking on the Move icon. You will be prompted for a reference point for the move. Click the LMB on the layout window then move the cursor. You will see a ghost image of the object being moved. Click LMB once again to complete the move. You can set the edit snap mode by typing the e key in the layout window. anyAngle and orthogonal are commonly used settings. Orthogonal is recommended for most editing.



Figure 1. Example Inverter Layout

Other selected-object edit operations of interest include copy, delete, property modification and rotate. Copy, delete and property modification all have associated icons. A common use of

property modification would be to change the width or length parameter of a device that has already been instantiated. For rotate, select

Edit > Other > Rotate (or type the O key).

There are three ways to enter layout shapes: rectangle, polygon or path. Each has an associated icon. Experiment with each by first selecting the active layer in the LSW window. Do this by clicking with the LMB on the layer you wish to enter. For most layers, you'll see multiple layer subtypes in the LSW. The dg (drawing) subtype will be used for most of your layout entry. The pn (pin) subtype will be used when designating pins.

Using the LSW, you can turn viewing and/or selection on or off for any layer. To toggle viewing for a specific layer (other than the active layer), click with the MMB on the layer. To toggle selection, click with the RMB. You can also toggle viewing and selection for all layers with the AV/NV/AS/NS buttons near the top of the LSW. Type Control-r in the layout window to redraw the window with the new settings.

The ruler can be used to measure distances in the layout window. This is especially useful when considering design rules. You can activate the ruler by clicking on its icon. Then LMB click on the start and end points. Clear rulers with Window > Clear All Rulers or just type the K key.

Using the above techniques, move the nfet and pfet to approximate the placement in Figure 1. Draw a PC rectangle to connect the gates and draw M1 rectangles or paths for vdd, gnd and out connections for the devices sources and drains. The nwell contact should be connected to vdd as well. The input in Figure 1 is in M1. You can create a contact from M1 to PC by choosing:

Create > Contact

Set the contact type to be PC_M1 (poly to metal1) and place the contact such that it touches the PC shape. Next, draw the horizontal M1 for vin. Unlike nwell contacts, substrate contacts are created separate from the device instantiation. You can create a substrate contact with:

Create > Contact

select contact type RX_M1, set rows and columns to 2, and place it under the metal1 gnd line. The RX_M1 contact contains only RX, M1 and CA layers. You will also need BP to make the diffusion P+. Draw this shape over the contact as shown to complete the substrate contact.

The final step is to add pins to the layout. Pins will be used as initial correspondence points in the layout vs. schematic check. You can see the pins in Figure 1. They are the small M1 squares you see on vdd, gnd, vin and vout. Create these with:

Create > Pin

The pin type in this case will be M1_T. I/O Type should match that of the schematic and you may choose to display the pin names if you'd like. Note that you will have to turn on pin names in Display Options ("e" key) in order to see displayable pin names.

Design Rule Check (DRC)

To check if your layout violates any of the various design rules, run DIVA DRC by selecting: Verify > DRC Click Ok to run the check. View the results in the CIW window. Violations will be highlighted in the layout. Once you've corrected any violations, move on to the next section to create an extracted view of the layout for LVS.

Extraction

In this step, a netlist will be generated from the layout. This can be used for comparison to a netlist generated from the schematic and later for Spectre re-simulation including the effects of parasitics. To create the extracted view, do:

Verify > Extract

Change the "Rules File" to "divaEXT41.rul". Then, click on "Set Switches" and choose "resimulate_extracted" in the pop-up. You can select multiple switches by pressing the control key while clicking on additional switches.

Now, launch the extraction by clicking Ok.

LVS

Your layout can be DRC clean but if it doesn't match the schematic, it will not perform as expected. For ex-ample, if you forgot to connect the pfet gate to the nfet gate, your inverter will not work, though it may pass DRC. Before you can pass the LVS check, the schematic you created for the inverter in the first tutorial will need a small modification. The DIVA deck extracts substrate contact instances from the layout. These same substrate contacts, which eventually resolve to resistors, must be present in the schematic as well. Modify your schematic as shown in Figure 2, adding the subc cell from the cmrf8sf library.



Figure 2. Schematic with subc Instance

For schematics you create in the future, be sure to add the subc instance for the nfet substrate connection prior to simulating. While its effect is minor, making schematic changes without resimulating should not be done since it introduces a gap in your verification strategy.

Once you have saved your schematic, run LVS by selecting:

Verify > LVS

Browse or enter the correct library, cell and view for both schematic and extracted. The library should be *tutorial* for both, cell should be *cmos_inverter* for both, view in the left-hand box should be *schematic* and view in the right-hand box should be *extracted* (not layout!). You may also have to enter the rules file name, *divaLVS.rul*. Click on Run. A pop-up will appear indicating whether or not the run completed. Success here does not mean the layout matches the schematic but only that the run completed. To view the results of a successful run, click on Output. LVS will check that all devices are connected in the same manner and that they have the same width and length parameters. Top-level pins or terminals are checked as well. LVS problems can be difficult to debug. You may find it helpful to view the netlists that are being compared. They can be found in the LVS run directory (specified in the Verify > LVS pop-up > Output) within the schematic and layout subdirectories.

After you get LVS clean, click on Build Analog in the LVS pop-up. Click Ok in the next pop-up. This will create an analog_extracted view for the cmos_inverter cell which can be simulated in Spectre. The netlist will include capacitive parasitics for the nodes in the circuit along with extracted diodes for the source/drain regions.