An Inductorless 0.3 – 2.6 GHz CMOS Receiver Front-End
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Abstract—This paper presents a wideband inductorless CMOS receiver front-end for a frequency range of 0.3 to 2.6 GHz. This front-end features a low noise amplifier (LNA) which feeds into quadrature mixers. High frequency harmonics are then removed by active filter stages at the output. This circuit features a high dynamic range through the ability to tune the gain of LNA and high linearity in the mixer core. The baseband bandwidth is also tunable. A voltage conversion gain of 35 dB, 3.3 dB DSB noise figure, -3.8 dBm IIP3 when in the high gain mode. This was all achieved in 0.13 μm CMOS with a 1.5 V power supply while consuming 23.3 mW of power.

I. INTRODUCTION

With the proliferation of wireless standards, there is an increasing need to develop a single transceiver that is compatible with many standards[1]. Specifically, the development of software-defined radio has made multistandard receivers an active area of research and development. The compatibility of a multistandard radio boils down to the receiving ability and the frequency range of the front-end. This drives the need for wideband front-ends that operate over a large range of frequencies. This project is concerned with development of a direct-conversion receiver front-end with frequency range from 0.3 to 2.6 GHz. Also, the front-end will be inductorless for high level of integration and simplicity. The major challenge lies within maintaining sufficient gain, noise figure, linearity and power consumption for the available voltage supply. The overall architecture of the front-end is given in Figure 1. The wideband operation is accomplished through the use of a wideband LNA, mixer and a tunable baseband filter. The absence of inductors greatly reduces the effective area required for the system with the drawbacks of an increase in power consumption and the total noise figure. This design also employs multigated transistors in the mixer to improve linearity as well as a tunable gain for the LNA to also help with the dynamic range of the receiver [1]. This is important because in the crowded frequency spectrum that this receiver targets, a large dynamic range is required.

This paper is organized in the following way. Section II covers the overall block level design. Subsections within II go into details about each of the key components of the front-end. Section III presents and discusses key results of the quadrature front-end. Section IV concludes this paper.

II. OVERALL SYSTEM AND DETAILED DESIGNS

The overall system is a typical direct-conversion front-end as depicted in Figure 1. The three blocks that are designed hereby are the LNA, the mixer core, and the active RC filter.

A. Low Noise Amplifier

The schematic of the LNA is shown below in Figure 2. This topology was chosen for a number of reasons. It offers wideband matching and low noise figure when compared to other topologies such as the common gate [1]. A quick inspection of the circuit entails the following design equations for the input impedance, gain and the noise factor.

\[
R_{\text{in}} \approx \frac{1}{g_{mn}+g_{mp}} \tag{1}
\]

\[
\frac{v_{\text{out}}}{V_{\text{in}}} \approx -(g_{mn} + g_{mp})R_f \tag{2}
\]

\[
F \approx 1 + \frac{1}{(g_{mn} + g_{mp})^2 R_s R_f} + \frac{4(y_n g_{d0n} + y_p g_{d0p})}{(g_{mn} + g_{mp})^2 R_s} \tag{3}
\]

The complementary pair input helps increase efficiency by having the \(g_m\)'s from the n and p devices sum [1]. The biasing of the input NMOS is controlled through \(R_F\). The gain stage is capacitively coupled to a buffer stage to help with reverse isolation from blocks further down the chain as well as helping to drive the large capacitive load of the mixer that follows [1]. This LNA also employs tunable gain through the application of a high voltage to the port \(V_{\text{gain}}\). When this

Figure 1: Receiver front-end architecture[2]
voltage is applied, the gain significantly drops; this helps increase the dynamic range of this receiver front-end. The total power consumed by the LNA is 14.5mW.

![Figure 2: LNA Schematic][1]

B. Mixer

A passive current steering mixer driven by a transconductance stage was adopted in this project. A conceptual diagram of the mixer is given in Figure 3.

![Figure 3: The mixer core architecture][2]

It consists of three main parts: a transconductor, a double balanced passive switching quad, and an active-RC low pass filter which also acts as a transimpedance amplifier to convert current to voltage. The conversion gain of the mixer and the filter stage can be computed as follows [2].

\[
G_C \approx \frac{2}{\pi} G_m \left( \frac{R_f}{1 + jwR_f C_f} \right)
\]

(4)

where \( G_m \) is the transconductance of the first stage and \( 2/\pi \) is the conversion gain of the passive switching quad. The input of the opamp provides a low impedance node to allow proper current switching operation for the passive mixer. The RC feedback also provides first order filtering for the signal before it is converted to a voltage. The design methodology for the individual blocks of the mixer core are detailed below.

**Transconductance Stage:**

As we know that a passive mixer is a highly linear mixer topology which provides a decent noise figure and consumes very little power. A passive mixer stage can be driven by a transconductor/amplifier to get a positive conversion gain from the mixer core. However, this shifts the stringent linearity requirements to the transconductance stage which is the main source of nonlinearity in amplifiers [8]. Therefore, extra care was taken to design the transconductance stage for low noise and high linearity. As illustrated by Figure 4, we adopted a differential complementary pair at the input of the transconductor. This significantly improves the linearity of the amplifier because there is large headroom for a high signal swing at the input and output nodes. Additionally, as described in [7], the main factor in determining IIP3/IMD3 of a FET is the second derivative of \( g_m \). It has been shown that the nonlinear behavior of \( g_m \) can be mitigated by connecting a parallel transistor biased in subthreshold because it cancels out the nonlinear effect of \( g_m \)" and extends the \( v_{gs} \) range for which a transistor can provide linear \( g_m \). This technique is called multigate transistor linearization [8]. The RF signal is AC coupled into the input of the transconductor stage for biasing flexibility and to suppress low-frequency harmonics. Moreover, the parasitic capacitance at the output of the transconductance stage must be minimized as it is directly seen as the source impedance by the active RC filter through the switching quad.

![Figure 4: Transconductance stage schematic][1]

**Switching Quad:**

In this mixer, we used a double-balanced current switching passive quad. It is very similar to a double-balanced Gilbert cell except that the switches do not have any DC bias current. Low flicker noise is very crucial in direct conversion receiver front-ends, and therefore as 1/f noise is proportional to bias current, having zero bias current in the switches is also critical. The proper sizing of the switches is very important for correct functionality of the mixer. The switches must have large W/L to have small \( R_0 \) to minimize the loss in the channel and to get the maximum possible conversion from the passive switches[6]. However, the switches cannot be too large since larger switches will have larger \( C_{gd} \) which corrupts the RF signal by increasing LO-to-RF feedthrough. The switches were sized at \( W/L \) of 10/0.12. The switches must be biased at \( V_m \) so that they weakly turn on during the LO+ cycle.
and avoid having DC bias current. This is a trade-off between 5% LO-to-RF feedthrough and a low $R_{ON}$ of about 100Ω.

C. Opamp and Active RC Filter

Linearity, stability, and a low input impedance to match the output of the mixer were all major design considerations for the active RC filter. The RC filter is realized with a fully differential opamp with negative feedback. The feedback capacitors and resistors will reside off-chip to allow more freedom in the implementation of the circuit. Specifications for the opamp include a maximum open loop gain of 70dB and corner frequency of 20MHz.

This circuit consists of three major stages: a cascode stage, a common source stage, and common-mode feedback. A conventional folded cascode topology is used at the input of the amplifier with cascoded NMOS loading for high gain. This approach simplifies biasing complications due to limited headroom. Tuning the transistor sizes in this first stage can improve the noise figure in the operational amplifier. A reduction in noise figure can be obtained with large channel lengths, large (W/L) ratios in the NFETs, and small (W/L) ratios in the PFETs. With the early gain from the LNA, we can trade some noise performance to conserve power and linearity [9].

The linearity in this stage dominates the linearity performance in the overall receiver. Ultimately, the linearity is controlled by the feedback network as governed by the following equations [10]:

$$HD3 = \frac{a_3}{4a_3(1+\beta a_1)} \left(1 - \frac{2\beta (a_2)}{a_3(1+\beta a_1)} A_{o1}^2\right)$$  \hspace{1cm} (5)

$$IM3 = HD3 + 9.5dB$$  \hspace{1cm} (6)

However, the linearity in the opamp can still degrade the system performance. The circuit applies common-mode feedback (CMFB) to maintain the output level at half the supply voltage. This CMFB uses the cross-coupled topology of paper [9] which sums the differential currents and sets bias of the current mirrors in the cascode.

III. SIMULATION RESULTS

In this section, the results of the system are presented. All values in the report can be reproduced with a 6k resistor and a 6pF capacitor in feedback for 5 MHz of IF bandwidth and the LNA in high gain mode. Figure 6 shows the conversion gain with a 1 GHz LO applied to the mixer core.

The S11 of the system over the expected spectral range is listed for both the high and low gain settings of the LNA assuming a 50Ω source impedance. As illustrated by Figure 7, the S11 remains constant with less than 1dB of fluctuation for minimal power reflection.

The IIP3 of the system with a 1 GHz LO is shown to be -3.8dBm. The linearity improves when the LNA operates in its low gain setting and also improves for lower frequency LO.
The DSB noise figure of the system was measured to be around 3.3dB as illustrated in Figure 8. The 1/f noise corner frequency is reduced to below 1 MHz by the design of the mixer as previously mentioned.

The area of the entire front-end was 772 µm x 554 µm due to the several decoupling capacitors implemented in the circuit, but it is still significantly smaller than an inductor-based model. The layout is shown Figure 10.

The system consumes 23.3mW to give a worst case IIP3 of –8 dBm and a minimal noise figure of 3.3 dB. The rest of the specifications are compared to other recent developments in Table 1.

Table 1: Comparison of System Level Results

<table>
<thead>
<tr>
<th>Parameters</th>
<th>[1]</th>
<th>[2]</th>
<th>[6]</th>
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<tr>
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<td>10 SSB</td>
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* LO 900 MHz, IF 5 MHz  ** LNA in high gain mode  *** Excludes Biasing and LO circuitry

IV. CONCLUSION

A low power, low noise, and highly linear inductorless front-end was presented for direct conversion receivers. The absence of large inductors makes it suitable for integration into large scale digital circuits. The circuit is amenable for software-defined radio with its ability to tune the conversion gain and the IF bandwidth. In conjunction with a quadrature LO that is tunable from 0.3 GHz to 2.6 GHz, this front-end can serve in many different wireless protocols.

REFERENCES


