TSV-based Ultra-High Data Rate Communication Link Circuits for 3D-ICs

by

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3D Integration

• Advantages of 3D Integration
  – Length of global Interconnects are reduced
    • High data rate and low power chip-to-chip communication link
  – Integration of heterogeneous technology
    • Logic, Memory, RF, Sensors, and etc.
  – Dedicated NoC plane for IP block level communication

Logic + Memory (IMEC)

2D planar integration
• Area = $L^2$
• Corner to corner distance = 2$L$

3D integration
• Area = $L^2$
• Corner to corner distance = $\sqrt{2}L$

Multi-stack

Bonding 8 chip stack 512 Mb = 4G DRAM stack (IEDM 2006)
Through Silicon Via (TSV) as 3D-chip Vertical Interconnects

• Through Silicon Via (TSV)
  – High Density vertical Interconnect
  – Enable high data rate chip-to-chip communication

Bondwire Interconnection [ChipPAC, Inc.]

Super contact TSV 3D-IC, [Tezzaron, Inc.]
TSV Characterization

- Multi-stack TSVs in 3D-ICs
  - Insertion loss 0.3 dB with 1 stacked TSV @ 10 GHz
  - Insertion loss < 5 dB with 10 stacked TSV @ 100 GHz

TSV Physical Parameters:
- TSV size: 1.2um x 1.2um
- TSV height: 6um
- Minimum pitch: 2.5um

Inserion Loss (dB) vs. Frequency (GHz)

1-stack TSV E Field Plot

5-stack TSV

10-stack TSV
TSV-based Communication Link Design

- Parallel signal link
  - Simple circuit
  - Large number of TSVs
  - Channel loss degradation
- High data rate serial signal link
  - Minimum vertical interconnection
  - High data rate on signal line
  - Channel loss compensation techniques
Eye Diagram

000

001

010

011

100

101

110

111
Intersymbol Interference

-- Wider spread channel Impulse response
-- Interference from neighboring symbols
-- Recovered symbol = 1(from C) + 2(from B) + 3(from A) + 4(from D)
Inverter-based Parallel Signaling Link

- Simple but effective broadband amplifier
  - Performs well with technology scaling and has good noise margin
  - PMOS restricts bandwidth and single-ended nature makes it susceptible to environmental noise
  - Used as our benchmark
Inverter-based TSV link Results

Eye diagram of received signal
Data Rate: 10 Gbps
Data input: $2^7-1$ PRBS

Limitations of inverter-based chip-to-chip link:
1. Signal damage due to channel loss
2. Limited data rate, require parallel signaling
3. Large of number of TSV vertical interconnects required for parallel data bus

Solution:
1. Ultra-high data rate serial chip-to-chip communication link
2. High speed buffer circuits and adaptive equalization circuits
Current Mode Logic Circuits (CML)

- Shunt Peaking and Negative Feedback
  - Shunt peaking and negative feedback

![Diagram of CML circuit with shunt peaking and negative feedback](image-url)
Current Mode Logic Circuits

• Two circuit techniques applied to increase broadband amplification out to 40GHz, or 80Gb/s
  – Shunt Peaking
    ▪ Place load inductance in series with resistor will create impedance component that increases with frequency
      ▪ Offsets capacitive component that decreases with frequency
        ▪ \[ Z(s) = (sL + R) \left| \frac{1}{sC'} \right| = \frac{R}{sC'} + 1 \]
  – Negative Feedback
    ▪ With enough gain in one amplifier, two can be cascaded with negative feedback which will trade gain for bandwidth
      ▪ \[ BW = (1 + \beta A_0) \times \omega_p \]
CML Circuits Channel Simulation

Eye diagram of received signal
Data Rate: 80 Gbps
Data input: $2^7-1$ PRBS

CML Buffer through 5-stack TSV

CML Buffer through 10-stack TSV
Equalization--Principle

---Channel: low pass effect
---Equalizer: counter the high frequency attenuation
Equalizer Circuit

--T-bridged Inductors vs. Transformer
--Tunable Resistor
--Adaptive frequency responses to compensate for different types of channel loss
On-chip for Transformer for Shunt and Double-series Inductive Peaking

- Shunt and double-series inductive peaking CML design
  - Need to consider the parasitic capacitances of on-chip transformers
  - Full wave simulation (HFSS) based transformer geometry optimization gives accurate RF passive device design
Equalization for Multi-stack 3D-ICs

--Different stacks feature in different loss
--Flexibility to accommodate different stacks of TSV
Equalizer-based Multi-stack TSV link

With Equalization

Without Equalization

(Data rate=80 Gbps ; PBRS=2^{10}-1)
Layout

CML with active negative feedback

Equalizer
## Benchmark Table

<table>
<thead>
<tr>
<th></th>
<th>[Ref1]</th>
<th>[Ref2]</th>
<th>CML Buffer</th>
<th>Equalizer</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13 µm CMOS</td>
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<td>0.13 µm CMOS</td>
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<td>Supply</td>
<td>1.5V</td>
<td>1.5 V</td>
<td>1.2 V</td>
<td>1.2 V</td>
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<td>Power</td>
<td>30mW</td>
<td>30 mW</td>
<td>24 mW</td>
<td>12 mW</td>
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<td>Circuit Configuration</td>
<td>Inductive peaking</td>
<td>Inductive peaking with negative feedback</td>
<td>Inductive peaking with negative feedback</td>
<td>Shunt and double-series peaking</td>
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<tr>
<td>Data Rate</td>
<td>40 Gbps</td>
<td>80 Gbps</td>
<td>80 Gbps</td>
<td>80 Gbps</td>
</tr>
</tbody>
</table>


Conclusion

• Inverter link
  -- Data rate : < 10 Gbps
  -- Simplicity
  -- Rail-to-rail swing

• CML link
  -- Data rate : 80 Gbps
  -- Low voltage swing
  -- Channel specific design required

• Equalizer
  -- Data rate : > 80 Gbps
  -- Low voltage swing
  -- Flexibility to accommodate different stacks of TSV
Thank you!