TSAV-based Ultra-High Data Rate Communication Link Circuits for 3D-ICs

Nathan Roberts, Qiong Wu, and Zhengzheng Wu

Abstract—A generic state-of-the-art TSV channel has been characterized using inverter as buffer, the simulation result shows that 1-stack TSV has a channel loss of 0.1 dB at 5 GHz, which is able to handle 10 Gbps data rate signal. However, when more stacks of TSVs is employed to transmit the signal, the increased channel loss will destroy the data. A CML buffer is designed for lossy 10-stack TSV channel, and signal integrity is maintained with data rate up to 80 Gbps. Moreover, an equalizer for accommodating different number of stacks of TSV by tuning the control voltage is demonstrated, which is suitable for multilayer chip-to-chip communication.

Index Terms—TSV, Equalizer, CML, 3D-IC

I. INTRODUCTION

The increasing demand in high data rate and diversified functional integration is continuously driving the semiconductor technology roadmap. It is believed that the new technology trend can no longer be addressed by only transistor size scaling predicted in Moore’s Law, while three-dimensional integrated circuits (3D-ICs) are emerging as a new promising solution [1]. The realization of hybrid 3D-ICs by stacking logic chips with high density memory dies, analog/RF modules, and integrated sensors has shown great promise, which is referred to as “Beyond Moore” scaling [2]. Meanwhile, it becomes difficult to implement high quality signal links based on traditional bondwires due to the difficulty of reducing the footprint and the signal loss when a large number of pads and bondwires are used for chip-to-chip interconnection. These problems can be solved by the through silicon vias (TSVs) [2], which greatly reduce the size of vertical chip-to-chip interconnections. As a result, high density and high bandwidth chip-to-chip data link is achievable.

In this study, high speed buffers and adaptive equalizing circuits are designed for 3D-IC chip-to-chip communication via TSVs. Ultra-high data rate wired communication circuits are implemented in 130nm CMOS technology. Moreover, based on the recent advancement in multi-stack 3D-IC technology, an adaptive circuit scheme is demonstrated for multi-layer chip-to-chip communication, which can have potential application in implementing signal buses for next generation TSV-based network-on-chip (NoC). The circuit design, simulation and TSV link channel simulation results will be reported in the following sections.

II. TSV CHARACTERIZATION AND CHIP-TO-CHIP COMMUNICATION LINK CONSIDERATIONS

The advancement in 3D-IC technology has lead to ultra small TSV diameters and ultrathin silicon wafers in multi-stack chips [1-2]. In our study, a state-of-the-art 3D-IC process [1] is utilized, which gives minimum TSV size of 1.2μm x 1.2μm, minimum pitch of 2.5 μm, and stacked wafer thickness of 6 μm. For characterizing the signal transmission quality through TSVs, HFSS full wave simulation is utilized. Fig. 1 shows the simulated insertion loss through 1-stack, 5-stack, and 10-stack of TSVs. In the simulations, minimum TSV size and pitch are used for high density consideration. The simulation results show that TSV link gives low insertion loss, less than 5 dB at 100 GHz with 10-stacks. Table I compares TSV interconnection with other tradition serial link transmission lines.

![Simulated TSV insertion loss for 1-stack, 5-stack and 10 stack 3D-ICs](image)

Fig. 1. Simulated TSV insertion loss for 1-stack, 5-stack and 10 stack 3D-ICs (with a 3D image of 5-stack inset).

Utilizing this high density TSV technology, chip-to-chip communication link can be achieved via digital circuits in the form of parallel signaling, as will be discussed in the report. However, studies on TSV and circuit interactions have shown that more sparsely spaced TSV could improve the yield in bonding process [1]. Also, the performance impact of TSVs adjacent to transistors needs to be considered [3]. These demands in TSV lateral placement could consume expensive CMOS die size. In our design, we consider that the communication link in multi-stack 3D-IC favors stringent use of TSVs. Also, the design needs to fully account for the losses when multiple layers of stacked chips are in the communication link. These criteria are also applicable in more generic TSV process developed as system-in-package (SiP)
Therefore, in this work ultra-high data rate serial link circuits using single signal line are also implemented for chip-to-chip communication. These circuit implementations will be benchmarked and discussed in the next sections.

<table>
<thead>
<tr>
<th>Material</th>
<th>loss@10Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper cable</td>
<td>-5 dB</td>
</tr>
<tr>
<td>PCB microstrip</td>
<td>-30 dB</td>
</tr>
<tr>
<td>Backplane trace</td>
<td>-27 dB</td>
</tr>
<tr>
<td>Si carrier</td>
<td>-17 dB</td>
</tr>
<tr>
<td>TSV (in this work)</td>
<td>-0.3 dB</td>
</tr>
</tbody>
</table>

### III. CHIP-TO-CHIP LINK CIRCUIT DESIGN

#### A. Inverter-based Link Circuits

The simplest broadband buffer considered for link circuit is the CMOS inverter. Its zero standby power and large gain compared to its small area make it an ideal buffer. It also performs well with technology scaling and has large noise margin. There are, however, a number of disadvantages, specifically due to the PMOS transistor which will limit the bandwidth. In addition, the single-ended nature of the inverter makes it susceptible to environmental noise [4].

In this work, the inverter-based circuits are first studied for benchmarking, for exploring the limitations in data rate and signal loss through TSV based on a pure digital implementation. Using a minimum sized inverter at both the transmitting and receiving end, different TSV scenarios were tested, including 1 stack of TSVs, 5 and finally 10 stacks. Simulation results show when data rate is 10 Gbps, sending data across a single TSV using an inverter reveals little loss in signal quality and preserves a very large eye opening in the transmitted data (Fig. 2(a)). However, sending data through 5 TSV stacks by inverter buffers cannot provide signal fidelity due to the channel loss introduced by long lossy TSV stacks, as is demonstrated in eye diagram in Fig. 2 (b).

![Fig. 3. (a) Signal across limited bandwidth channel. (b) Illustration of intersymbol interference](image)

To extend the bandwidth beyond that of the typical inverter and to compensate for the channel loss, CML (current mode logic) buffer is utilized for high data rate links. The CML buffer designed employs both shunt peaking and negative feedback for a differential output voltage swing of 1V. The shunt peaking is achieved by placing an inductor in series with the load resistor in the differential amplifier. This topology provides an impedance component that increases with frequency by offsetting the impedance seen by the load capacitance, which decreases with frequency. The gain of the amplifier is the product of $g_m$ and $Z(s)$, the latter being:

$$Z(s) = \left( sL + R \right) \left| \frac{1}{sC} \right| = \frac{R}{sLC + sRC + 1}$$  \hspace{1cm} (Eq. 1)

As can be seen in Eq. 1, the addition of $L$ in both the numerator and denominator contribute to 1.85 times extension in the bandwidth [5]. Additionally, two CML buffers with sufficient gain can be placed in cascade with a negative feedback added. The addition of negative feedback will trade gain for increased bandwidth [6]. As is shown in Fig. 4, the resulting CML buffer is a 2 stage shunt-peaked differential amplifier with negative feedback. The simulated frequency response shows that the bandwidth is extended to around 40GHz, with an input differential voltage swing of 500mV 80Gbps data rate. The buffer compensates the loss of 5-stack and 10-stack TSV transmission line at 40GHz. Transient simulations were run using a 25ps clock and a 2⁷-1 PRBS input, with a data rate of 80 Gbps. At the 10-stack case the
eye diagram shows an opening of 361mV with an RMS jitter of 4.3ps. The eye signal to noise ratio is 7.92, as is shown in Fig. 5. The extracted bathtub bit-error-rate (BER) plot using the transient simulation results is plotted in Fig. 6.

![CML Buffer schematic](image)

**Fig. 4. CML Buffer schematic**

![Eye diagram](image)

**Fig. 5. Eye Diagram of received signal with 2^7-1 PRBS input for CML Buffer through a 10-stack TSV**

![BER plot](image)

**Fig. 5. Extracted Bathtub BER plot for CML buffer through a 10-stack TSV**

### C. Adaptive Equalizer Circuit for Multi-stack 3D-IC

For multi-stack chip-to-chip communications, the channel implementation and circuit design should ensure that the signal transmission through different layers maintain high fidelity. Excessive channel loss compensation could lead to peaking when communication is through low loss channel, and energy is wasted. Therefore, it would be beneficial to implement self-adaptive techniques that account for various conditions. In multi-stack TSV links, longer TSV shows higher loss, for example 10-stack TSV will have a much higher loss in high frequency than 1-stack TSV. Therefore, equalizer circuits are designed which is capable of dynamically tuning for accommodating different conditions of TSV channel loss.

The equalizer circuit is based on a CML buffer circuits with shunt and double-series inductive peaking, as is shown in Fig. 6. For the purpose of saving area and improving circuit performance, an on-chip transformer with patterned ground shield is utilized for double-series peaking [5]. The transformer geometry is designed and optimized through HFSS fullwave simulation. The final equalizer circuit design can ensure optimized frequency response when channel loss through TSV link changes when different layers are in communication. A PMOS transistor is added to the CML circuit for adaptive tuning. The the frequency response of the equalizer is controlled by the gate voltage of the PMOS connected between the two branches. The PMOS is working in linear region which acts like a tunable resistor. Therefore, the total load resistance of the CML buffer can be varied by changing the control voltage ($V_{eq}$), resulting in the change in frequency response. Fig. 7. shows the frequency response of the equalizer when ($V_{eq}$) is 0V, 0.1V and 0.2V. The equalizer is working more like a “de-emphasizer” which reduces the DC gain of the buffer. This may lead to a decrease in the output swing. However, it can significantly improve the eye diagram.

![Equalizer schematic](image)

**Fig. 6. The schematic of the equalizer**

![Frequency response](image)

**Fig. 7. Frequency response of the equalizer circuit**

Fig. 8. shows that for three different TSV channel, namely, 10-stack, 5-stack and 1-stack, the overall frequency response after dynamic equalizing can be fairly flat to guarantee the high speed signal integrity. Fig. 9 demonstrates that the effect of having the equalizer in channel simulation, showing that the eye diagram is significantly improved by the equalizing.
The extracted BER bathtub plot for a 10-stack TSV link by employing adaptive equalizer is sketched in Fig. 10.

![BER Batman plot](image)

**Fig. 8.** The equalizer frequency response including TSV loss

![Eye Diagrams](image)

**Fig. 9.** The eye diagram of received signal with $2^7-1$ PRBS input after equalizing (a) 1-stack (b) 5-stack (c) 10-stack; Without equalizing (d) 1-stack (e) 5-stack (f) 10-stack

**Fig. 10.** Extracted Bathtub BER plot for equalizer through a 10-stack TSV

IV. CONCLUSION

In this report we characterized a TSV link using a state-of-the-art 3D-IC process and designed circuits that could boost performance through multiple TSV stacks. We implemented an inverter as our benchmark and improved upon its metric using multiple bandwidth and signal integrity improvement techniques, involving shunt peaking, negative feedback, equalization, and transformer peaking. The results show we can effectively transmit data at 80 Gbps through up to 10 stacked TSVs links in 3D-ICs.

V. APPENDIX

A. Circuit performance Comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>CML Buffer</th>
<th>Equalizer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology 0.13 μm CMOS</td>
<td>0.13 μm CMOS</td>
<td>0.13 μm CMOS</td>
</tr>
<tr>
<td>Supply</td>
<td>1.5 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Power</td>
<td>30 mW</td>
<td>24 mW</td>
</tr>
<tr>
<td>Circuit Configuration</td>
<td>Inductive peaking with negative feedback</td>
<td>Inductive peaking with negative feedback</td>
</tr>
<tr>
<td>Data Rate</td>
<td>80 Gb/s</td>
<td>80 Gb/s</td>
</tr>
</tbody>
</table>

B. Layout

![Layout Diagram](image)

**Fig. 11.** CML Buffer and equalizer layout

REFERENCES


