Bluetooth Receiver

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***Abstract*—A Bluetooth radio front end is developed and each block is characterized. Bits are generated in MATLAB, GFSK endcoded, and used as the input to this receiver model in Cadence. The output is then analyzed for various bit sequences, and input to a MATLAB demodulator. This circuit has 67 dB of gain, a 1dB compression point of -21.9 dBm, and draws 7.86 mW from 1.2 V_{DD}. This circuit was designed in 0.13µm IBM CMOS process.**

***Index Terms*—Receiver, Bluetooth, GFSK**

I. Introduction

Bluetooth was developed in 1994 by Ericsson to provide short-range, wireless data links with 1 Mb/s data rate. Since then, Enhanced Data Rate (EDR) schemes have adopted π/4-DPSK and 8-DPSK modulation schemes to achieve data rates of 2 and 3 Mb/s, respectively. Bluetooth has been integrated into numerous devices including cell phones, computers, speakers, printers, keyboards, and almost all devices currently employing wireless technology. The important figures of merit for any receiver include power consumption, noise figure, input referred 1 dB compression point, gain, and sensitivity. We will evaluate our receiver against two published receivers over the last six years using these as our comparison.

II. GFSK

Bluetooth uses Gaussian frequency shift keying, in which bits are encoded as frequency deviation from the carrier using a Gaussian filter. Figures 1a and 1b illustrate this concept. Figure 1a illustrates FSK, in which the frequency deviation occurs abruptly with each bit change, realized in time as a tone multiplied by a square pulse. In frequency this is equivalent to a sinc function convolved with an impulse, which is infinitely wide, with non-negligible side-lobes. Figure 1b illustrates the gradual frequency deviation from the carrier accomplished by replacing the square pulse of the FSK implementation with a Gaussian filter. Because a Gaussian pulse in time is Gaussian in frequency, this modulation scheme is realized in time as a Gaussian pulse multiplied with a tone, which is a Gaussian pulse convolved with an impulse in frequency. Due to the infinitely attenuating nature of a Gaussian function, the bandwidth of the FSK signal is lessened using GFSK.

III. Receiver Architecture

Figure 2 illustrates a system level block diagram of our receiver. This receiver takes a single ended input, and outputs

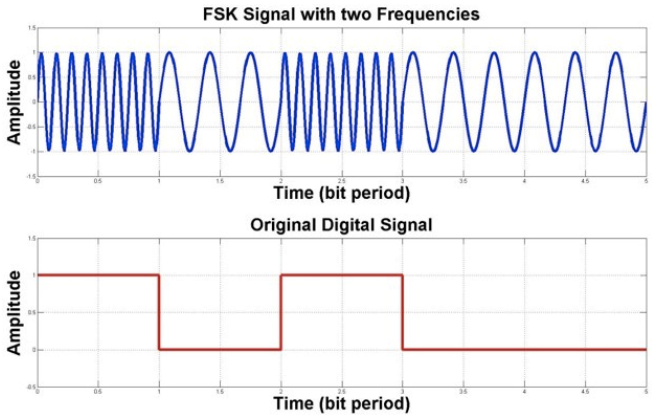

Fig. 1a. Frequency Shift Keying

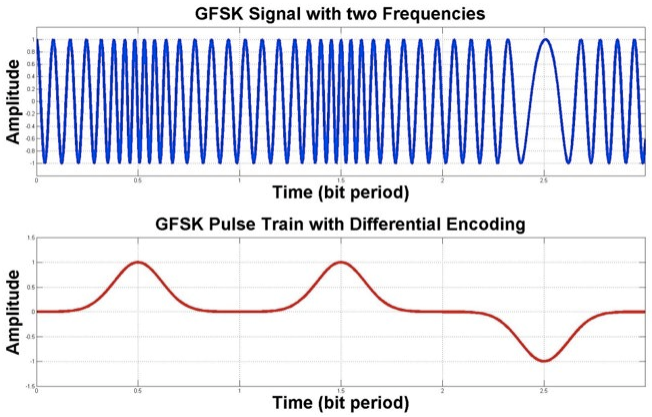

Fig. 1b. Gaussian Frequency Shift Keying

in-phase and quadrature down-converted signals. Our system uses direct down-conversion to avoid image rejection. This is made feasible by not transmitting data at the carrier frequency, which would be difficult to extract from the large DC output characteristic of direct down-conversion.

The first stage of our system consists of an LNA and preamplifier to provide high gain with low noise. This stage also acts as an active balun, converting the single ended input to a differential output. The next stage is the mixer, which uses the differential output from the LNA and the differential output of the VCO as its inputs. The VCO is an LC oscillator for less phase noise than a ring oscillator, at the expense of slightly higher power. The last block in our construction is an active low pass filter, which also acts as a balun. The output from this block is then demodulated in MATLAB. In the sections that follow we analyze each block individually.

IV. LNA and Preamplifier

The first stage of our system consists of an LNA and a

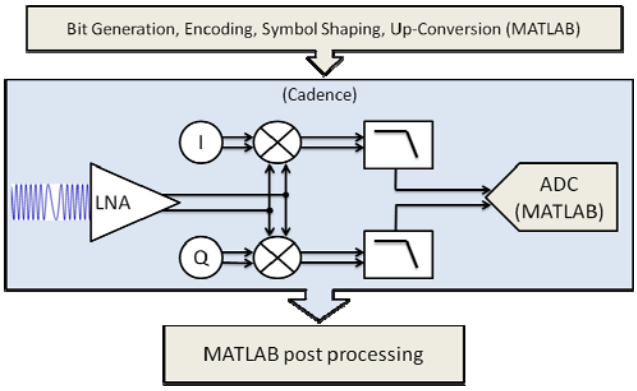

Fig. 2. System Block Diagram

preamplifier. The LNA is a cascoded common source amplifier that is degenerated for input matching. This circuit is illustrated in Figure 3, and the resonant frequency can be calculated as in Equation 1.

$$\omega_0 = \frac{1}{\sqrt{C_{GS}\left(L_G + L_S\right)}} \qquad \textbf{Eq. 1}$$

The input impedance at ω_0 was calculated in class, and is included as Equation 2.

$$Z_{IN} = L_S\left(\frac{g_m}{C_{GS}}\right) \qquad \textbf{Eq. 2}$$

From Equation 2, we can see that the real component of the input impedance can be matched to the 50 Ω source impedance using g_m, C_{GS}, and L_S. Furthermore, the output load is tuned to ω_0, using C_L and L_D, which is used to attenuate out-of-band frequencies, while allowing the desired signal to pass to the preamplifier. The desired current density through M1 in the LNA is achieved by mirroring I_{BIAS} and sizing M1 appropriately. M2 is used for cascoding in order to achieve reverse isolation, limiting LO leakage to the antenna. With this design we are able to achieve 14 dB of voltage gain with 2 dB noise figure and 13.5 dB reverse isolation. The 1 dB compression point is -21 dBm, consuming 876 µW from 1.2 V_{DD}.

The preamplifier is illustrated in Figure 4, and serves as an active balun in addition to providing additional gain. The input from the LNA passes through the decoupling capacitor, C_{BIG}, and appears over C_{GS1} of the preamplifier. The gate of M3 is biased with a DC voltage to keep it in saturation, which serves as an AC ground. The output of this amplifier is approximated in Equations 3a & 3b, illustrating how this amplifier acts as an active balun.

$$V_{OUT-} = -g_{m1}\left(g_{m2}r_{o1}r_{o2}\right)V_{GS1} \qquad \textbf{Eq. 3a}$$

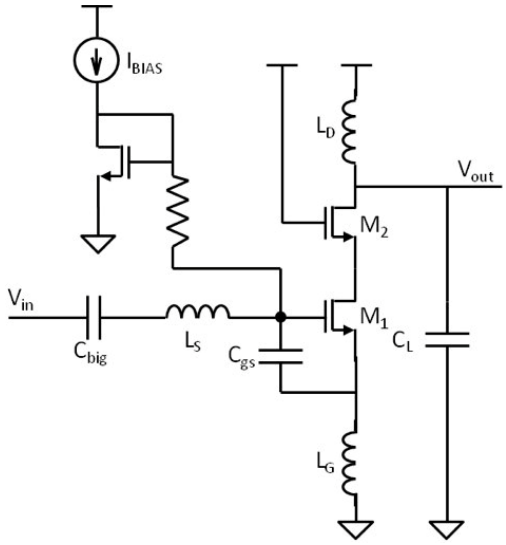

Fig. 3. LNA

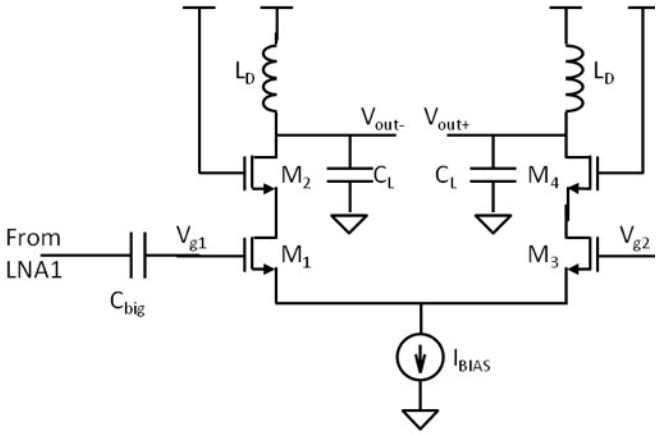

Fig. 4. Preamplifier

$$V_{OUT+} = g_{m3}\left(g_{m4}r_{o3}r_{o4}\right)V_{GS1} \qquad \textbf{Eq. 3b}$$

These equations are in the ideal case, with a tail source of infinite impedance. Finite tail source impedance causes slight amplitude mismatch between V_{OUT-} and V_{OUT+}.

This amplifier uses cascode transistors M2 and M4 for higher output impedance and gain, as well as improved reverse isolation. The preamplifier has a noise figure of 6 dB, 15 dB voltage gain, 13 dB reverse isolation, and a 1 dB compression point of -8 dBm, while consuming 990 µW from 1.2 V_{DD}.

V. VCO

The VCO is realized as an LC tank oscillator, which provides better phase noise than a ring oscillator. The circuit construction is illustrated in Figure 5. The tuning capacitors were originally realized as source-drain connected NFETs, but the back gate effect from LO leakage through the substrate was amplified in the preamplifier, overwhelming the desired signal. By using drain-source connected PFETs, we achieved

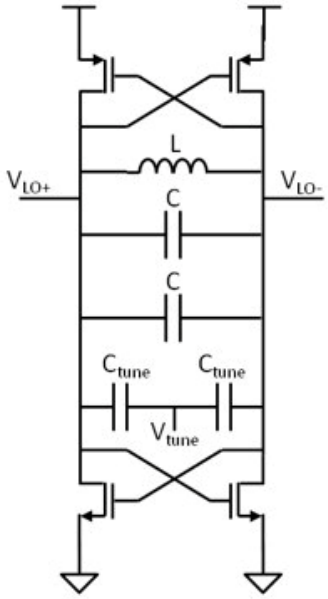

Fig. 5. VCO

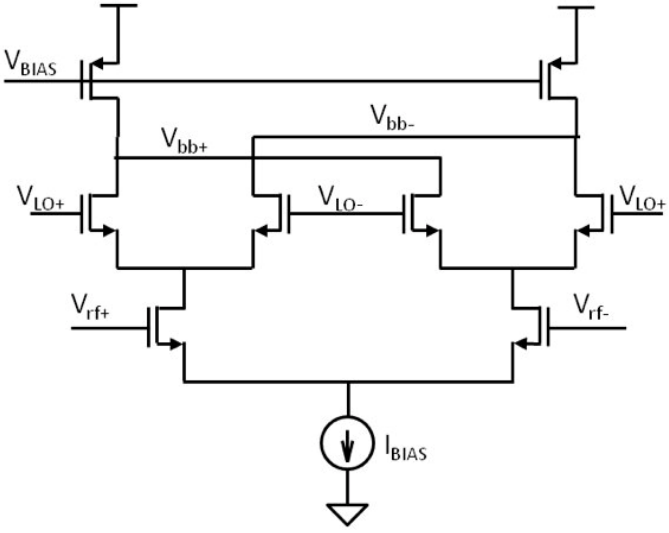

Fig. 6. Double-Balanced Gilbert Cell Mixer

better isolation due to the isolated well. We later learned that there are designated varactors in the kit, but did not employ them in our design. The parallel capacitors, both labeled C, are parallel MIM capacitor with equal capacitance, connected oppositely. The purpose of doing this is to simulate similar loading to both sides of the VCO for proper oscillation and duty cycle. The inductor in the LC tank is a symmetrical inductor, which is also to mimic equal loading to both sides of the tank. This inductor has a center tap which can be used to DC bias the output signal. We did not employ this feature because this circuit is self-biasing and we wanted to avoid an additional voltage reference. However, this feature can be extremely useful because optimization of the mixer might require a DC voltage at the LO input that cannot be achieved using the self-biasing of the VCO.

Our VCO operates between 2.41GHz and 2.49 GHz with a voltage tuning range of 400-600mV, requiring a DAC

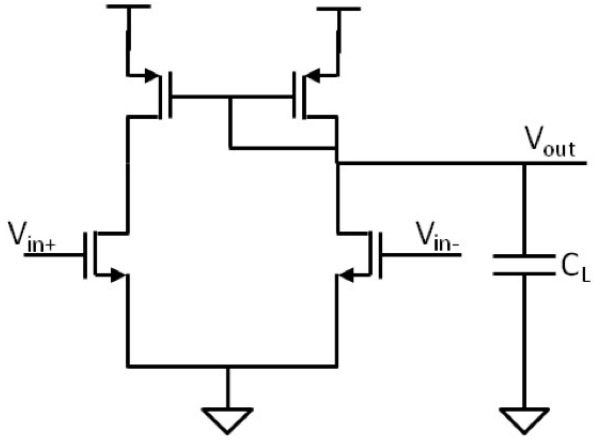

Fig. 7. Low Pass Filter

accuracy of at least 2.5mV. However, the frequency response to tuning voltage is nonlinear, having roughly square root dependence. This implies that the step size would have to be less than 2.5mV/channel (given a 1MHz channel) over certain channels, requiring even stricter requirements on the DAC. However, changing the ratio of C:C_{tune} can increase the tuning step size.

This VCO has an output amplitude of 350 mV centered at 750 mV, consuming 562 μW from 1.2 V_{DD}.

VI. Mixer

Our mixer is a double-balanced Gilbert Cell mixer. Using direct down-conversion we are able to avoid image rejection, but the DC output of the mixer stage must be the DC input to the next stage because we can no longer AC couple stages at baseband. Figure 6 illustrates our mixer. The LO transistors commutate the RF signal from one side to the other at ω_0. In this configuration, the DC bias current through each side of the output doesn't vary in time (ideally), and only the RF signal is commutated from side to side. Therefore, the LO is not present at the output, and only the IF frequency is present at the output. Because we are modulating to baseband, our IF is zero and only the demodulated signal is present at the output. Equation 4 illustrates the output of the mixer.

$$V_{BB} = \mathrm{sgn}\left(V_{RF}\right) \qquad \textbf{Eq. 4}$$

This mixer has a 1 dB compression point of -4dBm, input-referred 3.27 nV/$Hz^{½}$ thermal noise floor with 200 kHz corner frequency input referred, and 11dB noise figure at ω_{mod}, where ω_{mod} is the maximum frequency deviation from the carrier. The mixer consumes 1.98 mW from 1.2 V_{DD}.

VII. Low Pass Filter

After down-conversion, the signal will need to be low-pass filtered to remove the higher modulation terms. This can be done with a passive filter, but in order to achieve additional

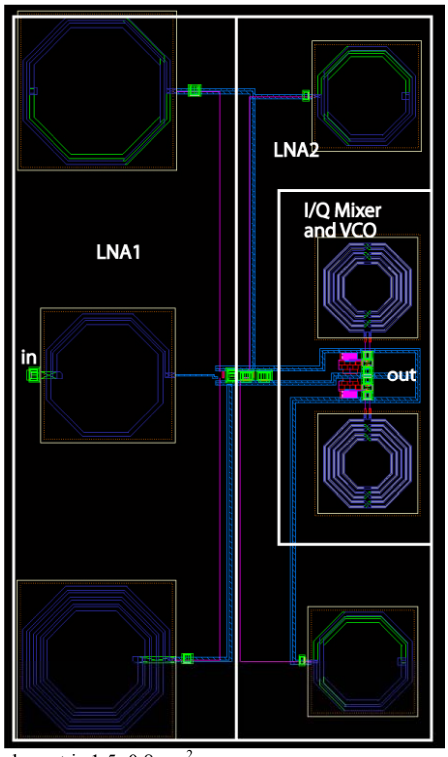

Fig. 8. The layout is 1.5x0.8mm^2.

gain, we have chosen to use an active filter. Using an active filter also acts as an active balun, recombining the differential signal to a single ended output. Figure 7 illustrates our filter. It is a differential amplifier with a current-mirror load, which provides the balun functionality. By choosing an appropriate value of C_L, we can make the output node the dominant pole and use this circuit as a low-pass filter with a 3 dB cutoff frequency of $1/(R_{out}C_L)$. This stage could also employ a variable tail current source in order to achieve variable gain, as the gain of this stage is g_mR_{out}, with g_m being a function of current density.

This stage provides 19.2 dB of gain, has a 1 dB compression point of -2.1dBm, 750 kHz bandwidth (C_L = 7pF), and consumes 136uW from 1.2V_{DD}.

VIII. Layout

Figure 8 illustrates the layout of our chip. The inductors in the VCO are symmetrical inductors, while the others are not. The in-phase and quadrature paths of the circuit have also been laid out symmetrically to try and match these signal paths. The LNAs have been placed as far as possible from these parts of the circuit to try and minimize LO leakage from the mixer and VCO to the earlier stages. This layout is 1.5x0.8mm^2.

IX. Demodulation

In demodulating the output signal, we found each received bit results in an output pulse whose time constant is defined

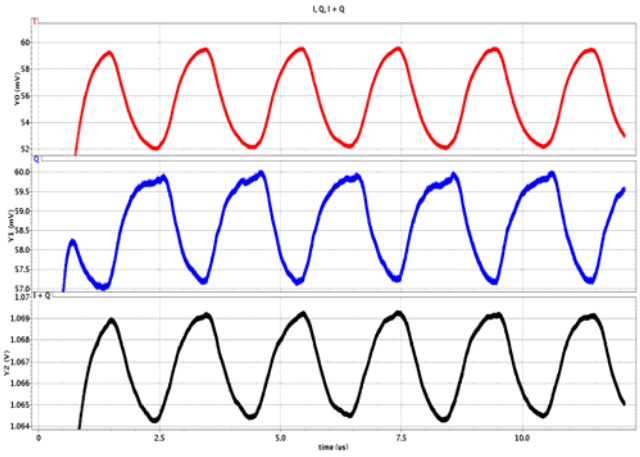

Fig. 9. Output for [010101010101] input at -80 dBm. In-phase (red), quadrature (blue), and the sum of the two (black) are presented, respectively.

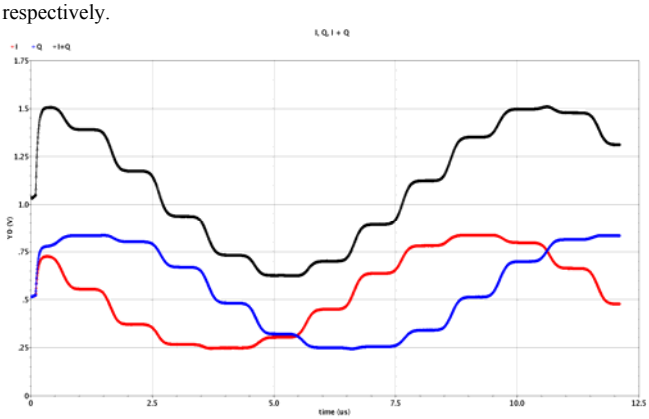

Fig. 10. Output for [111111111111] input at -50 dBm. In-phase (red), quadrature (blue), and the sum of the two (black) are presented, respectively.

by the bandwidth of the low-pass filter. Figure 9 illustrates the output for an input of 010101010101. The output has the expected bit rate of 1 MHz, with a rising edge for an incoming zero bit, and a falling edge for an incoming one bit. This leads to a concern that the output might saturate high or low for an input with an imbalance of ones or zeros.

Figure 10 addresses this concern, and illustrates the output for an input of 111111111111. We notice that the edge initially falls with each bit as expected, but eventually begins to rise. This can be explained by the phase shift that occurs with each incoming bit. Because the bits are encoded as a frequency deviation from the carrier, the phase offset between the LO and signal that results from each incoming bit is the integration of the frequency deviation over the bit interval. This is visualized as the area under each Gaussian bit pulse in Figure 1b. We can see in this figure that the area, and therefore deviation, is constant for each bit, and varies only in sign. This would be different for various modulation schemes, but would still be known to the receiver, and therefore deterministic from the received data.

Figure 11 illustrates the phase shift for Binary GFSK as a rotation in the S-plane by a constant angle ϕ for each incoming bit. By ensuring that the pilot that precedes each data packet contains an equal number of ones and zeros, we

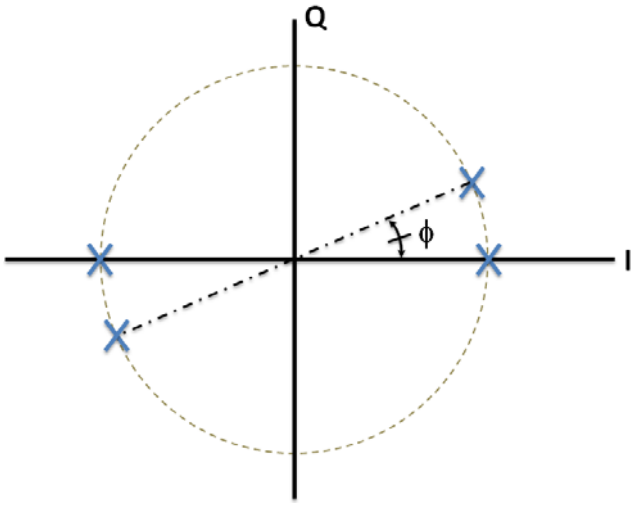

Fig. 11. Binary GFSK constellation rotation due to phase offset.

can ensure that there is no phase offset resulting from this part of the signal. Therefore, by representing bits 0 and 1 as symbols -1 and 1, respectively, we can calculate the phase offset for a given packet of length k using equation 5.

$$\phi_{offset} = \sum_{n=1}^{k} S_n * \phi, \qquad S_n \in (-1,1) \qquad \textbf{Eq. 5}$$

By maintaining the packet length short enough, we can ensure that the phase deviation will not exceed tolerable bounds.

Lastly, in Figure 9 we note the rising edge triggered by the incoming signal, which begins at 100ns. This energy can be detected by the radio as an alert of incoming data, which can be used to wake up the radio if a low power mode is desired.

X. Future Work

We were disappointed that we did not have enough time or manpower to conduct a full noise analysis of this circuit. We would have liked to determine the input referred noise variance for this circuit to generate bit streams with varying SNR values at the input. By demodulating the output and calculating the BER for each SNR, we could create a waterfall curve for this circuit and compare that with the ideal BPSK waterfall curve. This data would also determine the sensitivity for our receiver based on the required BER for a Bluetooth receiver. However, this simulation would take days, as we would have to run at least 1000 bits per SNR value to determine a BER of just 10^{-3}.

We would also have liked to write a more extensive demodulation algorithm in MATLAB, testing it over various conditions, and to have incorporated additional modulation schemes using complex encoding to achieve higher data rates.

TABLE I
Performance Comparison

	2004 [2]	2008 [3]	This Work
NF	-	13.11	~16.5
Sensitivity	-87	-	-
Gain [dB]	70	~90	67
IIP3 [DBM]	-21	-20.8	-21.9
VDD [V]	2.7	1.2	1.2
P_{VDD} [mW]	135	15.42	7.86
Tech. (CMOS)	0.25µm	0.13um	0.13um

XI. Conclusion

In this paper we have presented a Bluetooth radio front end that has 67 dB of gain, a 1 dB compression point of -21.9 dBm, and draws 7.86 mW from 1.2 V_{DD}. This chip was designed in IBM 0.13µm CMOS process. A comparison of this chip and previous works is presented in Table 1.

Acknowledgment

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