A Low-Power Zigbee Receiver using a Self-Oscillating Mixer

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***Abstract*—Low power, ad-hoc wireless networks have become quite popular due to their versatility and robustness. Since these networks consist of a large number of devices in close proximity, the link budget requirement on individual receivers is quite relaxed. Some important requirements include minimal power consumption (which increases lifetimes of battery-powered devices), and smaller chip area (which reduces manufacturing costs and simplifies implementation). In this project we present a low power, low IF receiver front end for Zigbee applications in the 2400 – 2483.5 MHz band. An LNA with a phase splitter is implemented in the front end to obtain quadrature RF signals. This stage is followed by a single cell consisting of a VCO and a mixer, which reduces size and decreases power consumption. Finally, a transimpedance stage generates an amplified differential voltage.**

***Index Terms*—Front end, LMV cell, low power, RF receiver, self-oscillating mixer, transimpedance amplifier, Zigbee**

I. Introduction

REMOTE monitoring systems that use wireless sensor nodes can be used in a number of applications including indoor climate control, cattle health monitoring, and soil moisture measurement. In many of these applications, replacing sensor batteries can be very costly, time-consuming, and in some cases, impossible. There is currently a strong demand for sensors with lifetimes of several years. One way to meet this demand is to minimize the power consumption of the devices. The IEEE 802.15.4 protocol, which Zigbee is built upon, defines a process for forming ad-hoc networks between multiple devices. This is why Zigbee is a popular for wireless sensor networks, and why Zigbee devices are designed to consume very little power.

Zigbee receivers have been implemented using several different types of architectures. A popular architecture is the direct conversion receiver. This design does not suffer from the image frequency problem, but it is very susceptible to the 1/f noise of the transistors and typically requires some kind of DC offset cancellation.

An alternate architecture is the low-IF receiver. This type of system does not require offset cancellation and can be designed to minimize the effects of 1/f noise. However, the image rejection problem cannot be ignored. The low-IF architecture was selected for this project because of the reasons stated above and the image problem can be addressed with a complex IF filter, downstream of the mixers.

Recently, current reuse techniques have been developed to combine multiple stages into a single circuit block [1][2]. This technique offers the potential for significant power reduction in receivers and the ability to shrink die area.

One of the other novel features of recent receiver architectures is the use of bond wires as inductors. Chip inductors have quite a low Q, which means they draw a lot of current when added to an LC tank. Bond wires have an inherent inductance associated with them, they can achieve high Q values, and they don't take up nearly as much space as chip inductors. For this reason, almost all of the inductors in this work are implemented using bond wires.

II. Receiver Architecture

The receiver architecture that was chosen was the low power quadrature receiver presented by Tedeschi, et al. [1]. In this architecture a current reuse technique is used by the implementation of a self-oscillating mixer (SOM). The SOM is a single block which consists of an LC tank stacked on top of two I and Q downconversion mixers. Since the LC tank signal is not split into in-phase and quadrature components, the incoming RF signal is split instead. An RC-CR filter is used to perform this task. The output of the SOM is a current signal which is converted back to a voltage and amplified by a transimpedance amplifier (TIA). An LNA is placed at the front of the receive chain to reduce the overall system noise figure. A system diagram of the receiver is shown in Fig. 1.

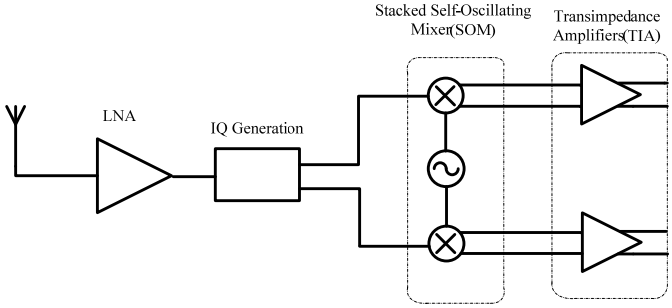

Fig. 1. Zigbee Receiver System Diagram

A. Low Noise Amplifier

The LNA used in this design is a single-ended cascode common-source amplifier with inductive degeneration. Using a cascoded topology has several advantages: there is reduced interaction between the tuned input and the tuned output [6],

the effect of C_{gd} of the input transistor is reduced, and high gain is achieved at the output. The main purpose of inductive degeneration of the input transistor is to input match the amplifier to 50 ohms, which is one of the standardized output impedances of any off-chip bandpass filter. Equation (1) below represents the input impedance of the LNA. An additional inductor L_G and capacitor C_1 are added to the circuit as shown in Fig. 2 to aid with input matching.

$$Z_{IN} = \frac{g_m}{(C_{gs}+C_1)} L_s + j\left(w(L_G + L_S) - \frac{1}{w(C_{gs}+C_1)}\right) \quad (1)$$

At the output, inductor L_L and capacitor C_L were selected to resonate along with the input impedance of the RC-CR filter at the desired center frequency of 2.45 GHz.

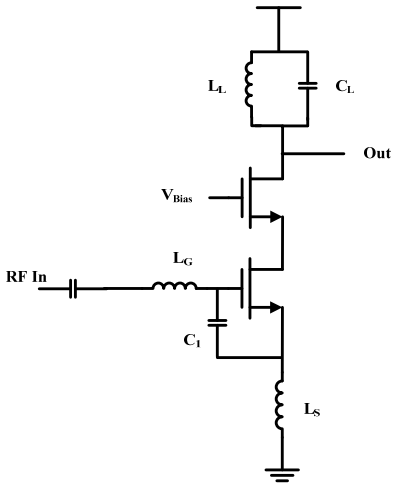

Fig. 2. Cascoded LNA

As per the Friis equation, it is important to have high gain and low noise figure in the first block of the receiver chain in order to minimize the overall system noise figure. The noise figure of the cascoded LNA topology is known to be dependent on the quality factor of the input resonant tank (Q_{IN}), the cutoff frequency of the input transistor (ω_t), and the current density through the transistor. By iteratively solving the design equations in MATLAB, we were able to bias our amplifier for low power and low noise performance.

Inductors L_L and L_S have been implemented as bond wire inductors. In this design we have modeled bond wire inductors with an inductance of 1 nH/mm, a series resistance of 0.5 Ω/mm, and we have also accounted for pad capacitances of 100 fF at each bond pad. Bond wire inductors are advantageous because they have a very high Q factor and do not take up any chip area. However, only 0.5nH-2.5nH inductors (wire lengths 0.5mm-2.5mm) can be practically realized. In [1], the Q of the wire bond inductors was estimated to be 35. To be conservative, a Q of 30 was used in these simulations.

B. RC-CR Filter

An RC-CR filter has been implemented as the load to the LNA to obtain quadrature RF signals. This block relies only on passive elements to generate a 90° phase shifted signal, hence no additional power is consumed. However, this simple design suffers from a signal attenuation of 6 dB and a large NF of 6 dB. Equation (2) shows the transfer function of the two outputs driving a capacitive load, C_L.

$$A_{VI} = \frac{1}{1+sR(C+C_L)} \ , \ A_{VQ} = \frac{sRC}{1+sR(C+C_L)} \quad (2)$$

As reported in Fig. 8, another inherent drawback of this design is the dependence of the output signal amplitude on the frequency. The amplitudes of the two outputs are equal only at the zero frequency ω = 1/(2πRC). The maximum amplitude mismatch that is seen in this design over the entire Zigbee spectrum is 4%. Since Zigbee uses an O-QPSK modulation scheme for data transmission, phase mismatch is more of a concern than amplitude mismatch. Fig. 8 shows that the phase difference between the two outputs is constant (89.2°) over frequency, justifying the use of this filter in our design. It can also be noted that the overall mismatch is independent of the additional load, as this only impacts the pole of the circuit.

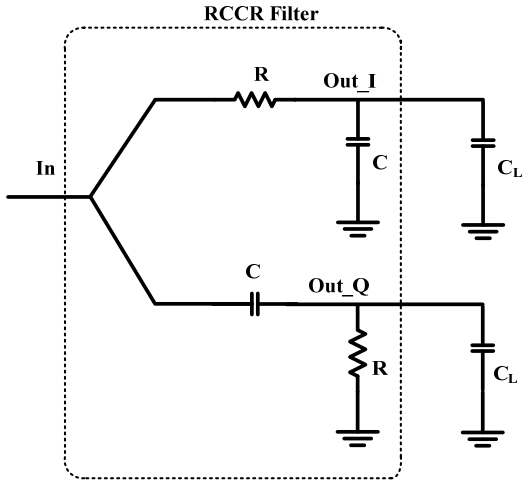

Fig. 3. RC-CR Filter with Capacitive Load

For robustness, the value of capacitor C in the RC filter has to be made much larger than C_L to reduce attenuation. Since the overall input impedance of this circuit is approximately 1/Cs, having a very large filter capacitor lowers the input impedance. In this design, the value of C_L (from the input of the SOM) is 320 fF. Designing an RC-CR filter to drive this load requires a very large filter capacitor, and reduces the LNA gain. To avoid this problem, additional inductors are added at the input stages of the SOM to resonate with C_L at the design frequency. This makes it possible to design the filter with smaller capacitors.

C. Self-Oscillating Mixer

The SOM block consists of a differential LC tank stacked on top of the I and Q mixers. Each mixer uses a pair of cross-coupled transistors on top of a pair of switches which direct the current back and forth through the IF load, as shown in Fig. 4. The current through each branch is set by the tail transistor, which also acts as the transconductance stage of the mixer.

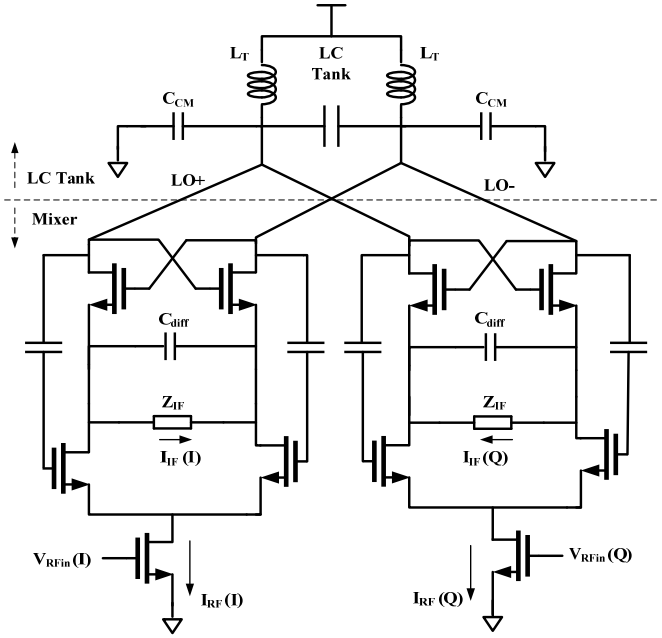

Fig. 4. Schematic of Single Oscillator Mixer

A differential LC tank topology with capacitances C_{CM} to ground was used as the VCO. The justification for this topology is explained later in this section. To ensure that the LC tank oscillates, the equivalent parallel resistance of the tank must be greater than the negative resistance presented to it by the cross-coupled transistors. The impedance shown to the tank by a single mixer is given by (3). Assuming that C_{diff} is large and C_{gs} of the cross-coupled pair is small, this expression reduces to $-2/g_m$. This resistance is halved when the second mixer is connected in parallel. Therefore, a large g_m for the cross-coupled transistors and a large Q_{tank} are desirable. To achieve a large quality factor for the LC tank, wire bond inductors were used in this circuit block as well. Any additional inductance needed could be added off-chip.

$$R_{DOWN} = -\frac{g_m + j\omega\left(2C_{diff} + C_{gs}\right)}{j\omega C_{diff}\left(g_m - j\omega C_{gs}\right)} \tag{3}$$

The two outputs of the LC tank, LO+ and LO-, were connected to the four switching transistors in such a way that switches diagonal from one another were conducting at the same time. This performed the commutating action of the current through the IF load. In parallel with the IF load is a large capacitor which presents a high impedance at f_{IF} and a low impedance at f_{LO} and f_{RF}. This minimizes LO leakage, improves conversion gain, and ensures that only a real impedance is presented to the LC tank above.

The conversion gain of the circuit is defined as the ratio of the amplitude of the output current at f_{IF} to the amplitude of the tail current at f_{RF}. If there is a non-negligible parasitic capacitance at the mixer output nodes, then these capacitors will shunt current away from the IF load, reducing the gain. For this reason, a differential LC tank is used [1]. This tank includes capacitors C_{CM} which present a low impedance to the output nodes at f_{RF}. This lower tank impedance allows for more of the RF current to flow through the IF load, maintaining a conversion gain close to $2/\pi$. The complete expression for conversion gain using the differential tank is given by (3).

$$CG \cong \frac{1}{\pi}\frac{2 + j\omega_{LO}C_{CM}\left(j\omega_{LO}L_T\right)}{1 + j\omega_{LO}\left(C_{par} + C_{CM}\right)\left(j\omega_{LO}L_T\right)} \tag{4}$$

Finally, the tail transistor converts the input RF voltage to a current. To maximize the gain through the entire mixer, the g_m of the tail should be made as large as possible. However, this introduces a trade-off because a larger g_m requires more power consumption. This tail transistor also sets the bias current for the circuit and must be sized appropriately to do so.

The output impedance of the SOM is limited by the inductance in the tank and by the Q of the tank, as shown in (4). Since these two values tend to be quite small, this also becomes a limitation on the maximum voltage the mixer can produce across the IF load. To avoid this problem, a virtual ground with a very low impedance at f_{IF} is connected to the mixer output and the current is measured instead of the voltage.

$$R_{OUT} = 4\omega_{LO}L_T Q \tag{4}$$

D. Transimpedance Amplifier (TIA)

The TIA implements a virtual ground that senses the down converted signal current of the SOM at the intermediate frequency. Implementing a virtual ground with a low input resistance minimizes the current loss and also improves the linearity [2]. We chose the TIA architecture shown in Fig. 5 which is based on the gain-boosted cascode configuration. A common mode feedback loop at the output stage is used to maintain appropriate bias for the TIA by drawing current from the LC tank of the SOM.

The TIA also provides a low impedance at the IF output nodes of the SOM. The expression for impedance at low frequency is equal to:

$$R_{IF} = \frac{2}{g_{m1,2}A} \tag{5}$$

where $g_{m1,2}$ is the transconductance of transistors (M_1, and M_2) and A is the gain of the core amplifier [1].

By maximizing the product $g_{m1,2}A$, a better virtual ground (i.e., one with smaller equivalent impedance) is feasible, leading to a greater down conversion gain in the SOM. The transconductance can be augmented either by increasing bias current at the cost of higher power consumption, or increasing the aspect ratio of transistors (M_1, and M_2). Increasing the aspect ratio of these transistors adds more parasitic capacitance at the output nodes of the mixer and consequently, affects the down conversion gain of the mixer and the phase noise. Therefore, it is better to increase gain of the core

amplifier over a large frequency range. This high gain over a large bandwidth (much larger than the Zigbee channel bandwidth, 3 MHz) is achieved by utilizing a differential folded cascode amplifier, as shown in Fig. 6 [1]. The folded cascode amplifier has a large enough bandwidth, high gain, and high stability, but at the cost of limited voltage headroom.

The input stage transistors of the amplifier, Mn_1 and Mn_2, have the most significant effect on the noise of the TIA. Therefore, the lengths of these devices were increased to minimize flicker noise and increase gain. On the other hand, since the parasitic capacitance of these two transistors affects the output stage of the mixer, they should not be made too large [2].

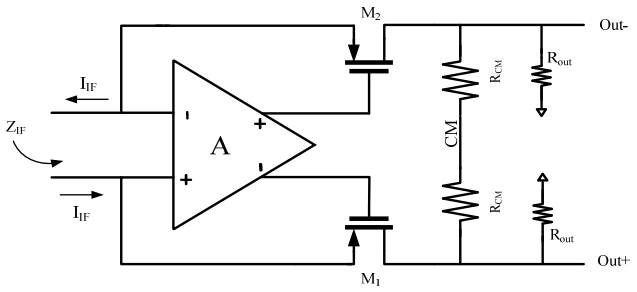

Fig. 5. Gain-Boosted Cascode TIA

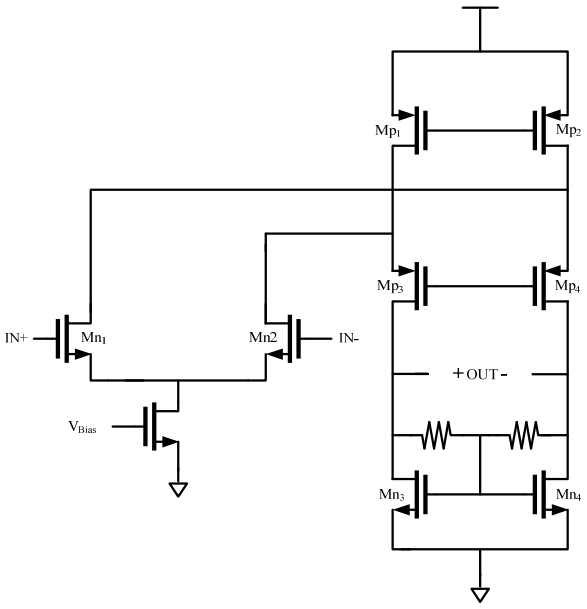

Fig. 6. Differential Folded Cascode

III. Results

A. Low Noise Amplifier

The use of bond wire inductors has allowed us to design an LNA that draws only 1.2 mA of current and provides 22 dB of gain at the center frequency. The input has been successfully matched to 50 Ω and an S(1,1) of less than 18 dB is obtained over the entire Zigbee band as shown in Fig. 7. The average noise figure measured between 2.4 GHz and 2.5 GHz is 2.25 dB. The measured 1dB compression point at the output of the LNA is -10.5dBm.

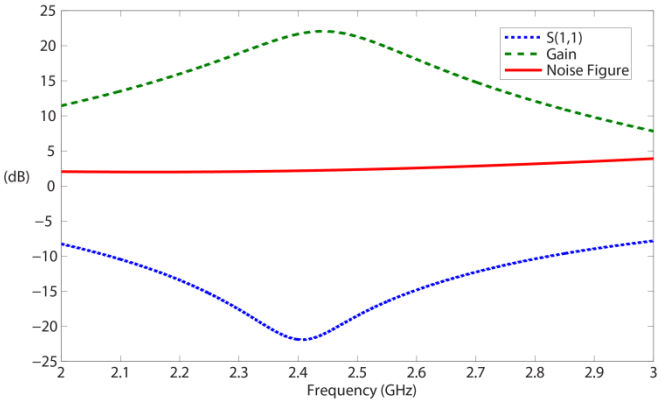

Fig. 7. LNA Return Loss, Gain, and Noise Figure vs. Frequency

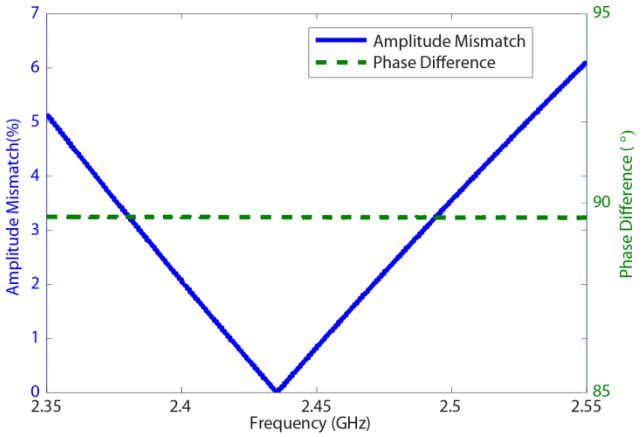

Fig. 8. IQ Mismatch due to RC-CR Filter

B. SOM

Since the Q of the LC tank is so large, the LO voltage swing is also large, allowing for a very small phase noise. The phase noise of the oscillator is -138 dBc/Hz at 3.5 MHz away from the tone. Since the oscillator frequency can fluctuate slightly with bias current, ideal sources were inserted in place of the tank when the mixers were simulated to allow steady state analyses to converge.

The input RF signal was converted from a voltage to a current by the tail transistor. Since the bias current was so low, the transconductance of this transistor was only 8 mS. This meant that the signal suffered a -42 dB loss in the transconductance stage. The input current to output current conversion was 0.62 (approximately $2/\pi$).

The total power consumption of the SOM was 2.2 mW, the noise figure was 21 dB, and the 1 dB compression point was -15 dBm. To make the SOM more linear, the tail transistor could be degenerated. If this had been done, the circuit would resemble the LMV cell [2]. A transient waveform of the SOM output current is shown in Fig. 9. The IF frequency can be clearly seen in this plot, along with the LO frequency on top of it.

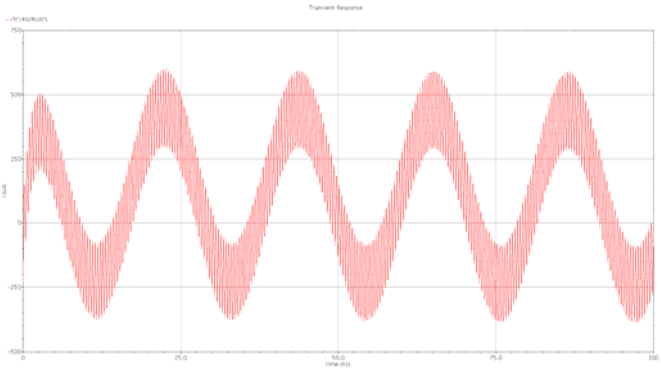

Fig. 9. Transient Response of Mixer Output

C. TIA

In our core amplifier we obtained a gain of 32 dB over an 8 MHz bandwidth, at a bias current of 68uA. This yielded an impedance of 12 ohms at the output nodes of the mixer. The gain of the TIA is 65 dB, which has a significant contribution to the overall gain of the front end receiver.

D. Receiver System

Table 1 compares our work with several other designs. We were able to achieve a very low phase noise (-138 dBc/Hz), and a low power consumption (3.7 mW). The overall gain of our circuit is lower than [1] and [3] because our circuit did not have the complex IF filter at the output stage (i.e., after TIA).

Fig. 10 shows the complete layout of the receiver system. The layout was supposed to be inductor-less, but for training purposes, we included one on-chip inductor (the gate inductance of the LNA). Since most of the inductors of our design were off-chip, we obtained a very small area (0.34 mm^2).

TABLE I
SIMULATION RESULTS AND COMPARISON

Symbol	[5]	[3]	[1]	This Work*
Gain [dB]	33	75	76	36
NF [dB]	7.5	12	10	12
IIP3 [dBm]	-10	-12.5	-13	-21
IF Frequency [MHz]	-	2	3	5
PN @ 3.5MHz [dBc/Hz]	-	-107	-124	-138
Power [mW]	5.4	3.6	3.6	3.72
Integrated Inductors	2	1	0	1
Area [mm^2]	0.23	0.35	0.23	0.34
Vdd [V]	1.35	-	1.2	1.2
Technology [µm]	0.09	0.09	0.09	0.13

*Does not include IF Filter

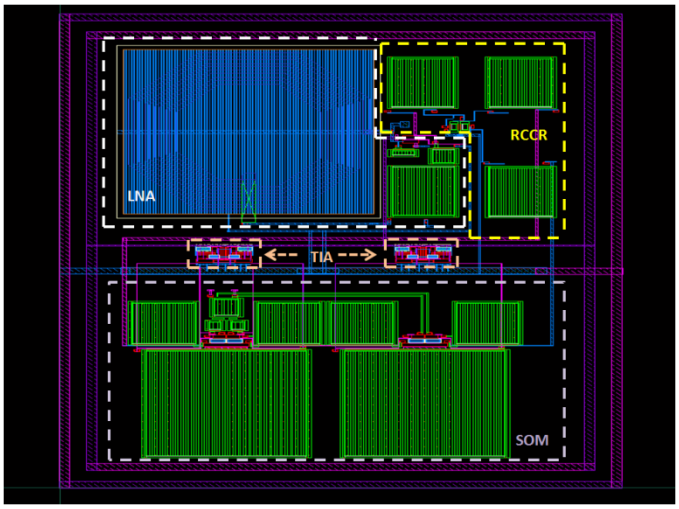

Fig. 10. Circuit Layout of Receiver

IV. CONCLUSION

In this paper we have presented a low power, low IF receiver for Zigbee applications. The receive chain consists of an LNA, an RC-CR quadrature generator, a self-oscillating mixer, and finally two transimpedance amplifiers. The performance of the receiver has been shown to be comparable to the state of the art. This circuit is ideal for use in low power sensor networks in remote monitoring systems.

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