

Quadrature GPS Receiver Front-End in $0.13\mu\text{m}$ CMOS: The QLMV cell

Yee-Huan Ng, Po-Chia Lai, and Jia Ruan

Abstract—This paper presents a GPS receiver front end design that is based on the single-stage quadrature LNA-Mixer-VCO (QLMV) cell. It is a popular low power design architecture that reuses current across different functional blocks. Our design merges the quadrature VCO and mixer into a single block, which is stacked on top of a differential LNA to achieve a low power receiver front end. The application of a double-balanced mixer and gate-modulated VCO topology also helped to reduce the phase noise and provided high quadrature accuracy. This circuit was implemented in $0.13\mu\text{m}$ CMOS with a power consumption of only 2.14mW .

Index Terms—Current reuse, GPS, LNA, mixer, receiver, VCO

I. INTRODUCTION

THE recent popularity of battery-operated mobile devices with location-finding capabilities has contributed to a growing GPS market. This is also evident from the recent U.S. Federal Communications Commission's (FCC) rule to include GPS technology in cell phones [1]. As a result, the demand for low power GPS receivers is huge and the aggressive technology scaling is driving innovations in transceiver architectures with low power supply voltage operation. This paper describes a solution to reduce power consumption that involves a current reuse architecture, i.e., multiple RF circuit blocks using the same dc bias currents are merged to form a single cell.

The quadrature LNA-Mixer-VCO (QLMV) is a RF front end receiver topology that stacks the low noise amplifier (LNA), mixer, and quadrature voltage-controlled oscillator (QVCO) in a single stage. All three components share the same dc bias current and thus minimizing the circuit area and power consumption. Fig. 1 shows the block diagram of a QLMV cell and Fig. 2 shows the circuit schematic.

A key part in the QLMV circuit is to design the QVCO to oscillate at a certain frequency with 90° phase difference between the output signals. Our receiver front end is intended to work with the civilian L1 frequency of 1.57542GHz and generate quadrature signals at an IF frequency of 3MHz . Therefore, the QVCO was tuned to oscillate at around 1.57242GHz . We adopted the gate-modulated scheme (GM-QVCO)

to minimize phase noise and the required voltage headroom [1].

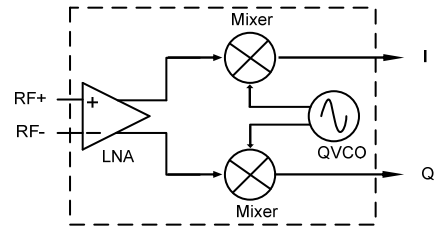


Fig. 1 Quadrature LNA-Mixer-VCO cell (QLMV) block diagram

II. QLMV CELL DESIGN

A. Architecture

As shown in Fig.2, the GM-QVCO is stacked on top of the double-balanced Gilbert mixer, which is atop the differential LNA input stage. For quadrature operations, the differential LNA drives both I and Q channel mixers. The NMOS at the bottom helps to set up the DC bias current that is reused by the LNA, mixer, and QVCO. The advantage of a double balanced mixer is the higher conversion gain (twice that of a single-balanced mixer design). The switching transistors also help to subtract the amplified local oscillator signals. Hence, this results in the cancellation of LO-to-IF feedthrough [1]. This double-balanced architecture also rejects common mode power supply noise. The differential LNA provides immunity to RF-to-IF feedthrough.

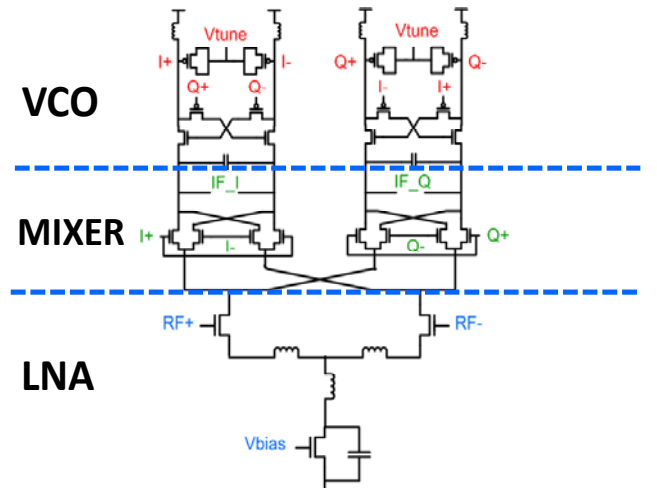


Fig. 2 Quadrature LNA-Mixer-VCO cell (QLMV) schematic

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B. Input Matching

Since the LNA is a type of common source amplifier with inductor degeneration, the input impedance can be calculated as follows [9]:

$$Z_{IN} = \frac{g_m L_{source}}{C_{gs}} + j(\omega(L_{gate} + L_{source}) - \frac{1}{\omega C_{gs}}) \quad (1)$$

To match input impedance at the L1 frequency, ω_0 , we equate the real part of (1) to the source impedance and the imaginary part to zero. Therefore, the input impedance takes the form of a series resonant network with a quality factor of [1]

$$Q = \frac{\omega_0(L_{source} + L_{gate})}{2R_s} \quad (2)$$

where

$$R_s = \frac{g_m L_{source}}{C_{gs}} \quad (3)$$

$$\omega_0 = \frac{1}{\sqrt{(L_{source} + L_{gate})C_{gs}}} \quad (4)$$

From equation (2), we can tune the input match by adjusting the source and gate inductance, L_{source} and L_{gate} .

C. Linearity

The downside of current reuse is poor linearity because the bias current of LNA is the same as that of the QVCO and mixer stages. The IIP3 calculation of a common source LNA is [10]

$$IIP3 = \frac{4}{3} \times \frac{g_m}{K_{3gmA}} \times \omega_1 \omega_2 C_{gs} \quad (8)$$

K_{3gmA} is the second derivative of the transconductance with respect to input [10]. Based on equation (8), a small bias current implies a small g_m of the LNA and hence low linearity. The overall linearity of the QLMV is limited by that of the LNA.

In our analysis, we use a current of 2.14mA to set a compromise between linearity and power consumption, i.e. low dc bias current causes low linearity but circuit consumes minimal power.

III. GATE-MODULATED QVCO

A. Architecture

The gate-modulated QVCO (GM-QVCO) [1] in Fig. 3 consists of two identical LC oscillators coupled using triode region transistors in series with the gates of the NMOS switching devices. These PMOS coupling devices (MI1,2 and MQ1,2) modulate the negative transconductance of the cross-coupled NMOS switching transistors (MI3-4, MQ3-4) to achieve anti-phase injection locking. Consequently, 90° phase difference will result between the output signals.

When compared to the traditional LC oscillator with series coupling approach, this GM-QVCO can operate with low power supply voltage due to the absence of cascade connections.

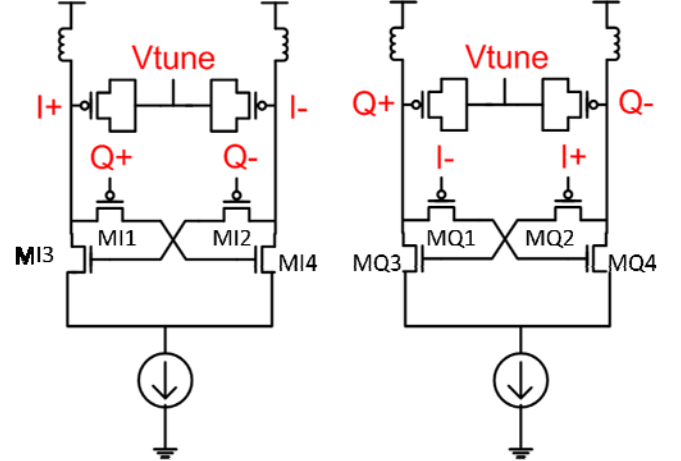


Fig. 3 GM-QVCO with PMOS coupling device and NMOS switching pairs

This technique can also reduce the phase noise significantly since gate modulation is an ideally noiseless coupling scheme [1]. Since the PMOS coupling transistor (MI1 or MI2) is connected to the gate terminal of the switching transistor (MI4 or MI3), which has high impedance, its drain noise current circulates locally through MI1 and would not be injected into the output node I+. However, the downside to this approach is that it increases the parasitic capacitances at the output nodes of the oscillator. This has negatively affected the tuning range of the varactors, which are made up of the drain-source connected PMOS transistors.

The QVCO proposed by Cheng, et al. [1] uses NMOS devices for gate coupling. When we simulated this approach in Cadence, the QVCO could not oscillate at the desired frequency. It was observed that the high threshold voltage of the NMOS transistors due to body effect had caused them to turn off. This was easily fixed by replacing them with PMOS transistors. Since each PMOS N-well is separated from each other, we can connect the body terminals to its source terminals and thus reducing the threshold voltage.

B. Oscillation Frequency

In order to have our VCO oscillate at the desired LO frequency of 1.57242 GHz, we adjust the inductance and capacitance according to the following equation

$$\omega_{Lo} = \frac{1}{2\pi\sqrt{L_T C_T}} \quad (9)$$

C. Start-up condition

If no current is injected into the LC tank when V_{DD} is first turned on, the QVCO circuit will not oscillate. Therefore, we designed a simple start-up circuit to ensure oscillation will occur. This simple circuit (Fig. 5) consists of two PMOS transistors and a capacitor.

When VDD is turned on, current will flow from the supply

rail to LC tank through MS2. This will keep going on until the capacitor CS is fully charged. At this point, MS2 becomes off and the start-up circuit stops supplying current.

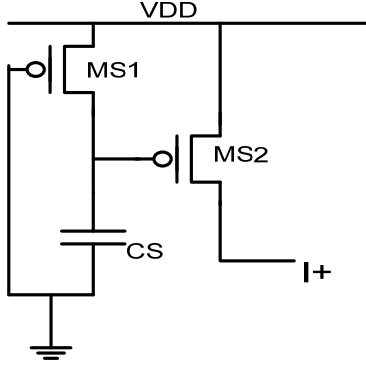


Fig. 5 Start-up Circuit

IV. LNA + MIXER

A. Architecture

The LNA-mixer and the QVCO are biased by current source M_b as shown in Fig. 6. To optimize the LNA noise figure, M_b should have minimum channel length and small width [11].

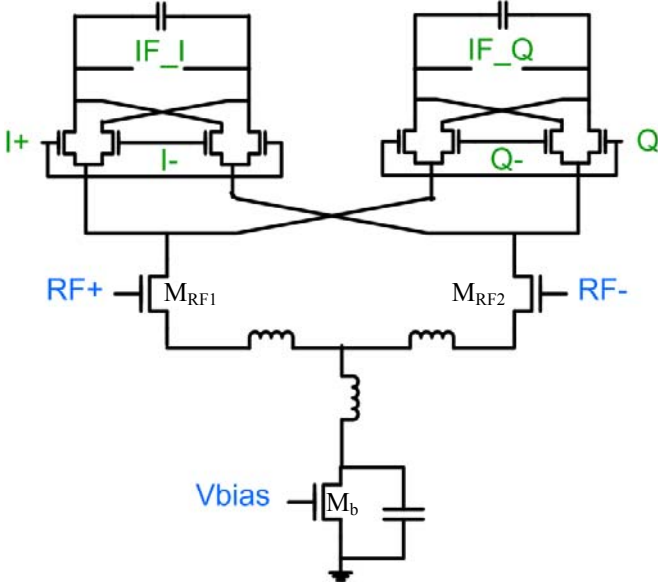


Fig. 6 LNA and Mixer schematic

B. Design challenge

Major challenges of the LNA-mixer block and the entire QLMV cell is to maintain low noise figure with acceptable gain while maintaining low power consumption. Due to low voltage headroom and body effect, LNA-mixer current source transistor, M_b , and LNA input transistors, $M_{RF1,2}$, may be turned off easily while trying to achieve high gain for LNA. The LNA-mixer must be biased very carefully. Another major problem is the inductors for the matching network of the LNA. The integrated inductors have relatively low Q and

will limit the overall performance of the LNA-mixer such as the LNA transconductance, G_m , according to the following equation

$$G_{m,LNA} = Q_{RLC} \cdot g_{m,MRF} \quad (10)$$

$G_{m,LNA}$ is the dominant factor in the overall gain of the block. It affects both the gain and noise figure of the QLMV cell. From (10), higher Q_{RLC} provides higher $G_{m,LNA}$, and Q_{RLC} is limited by the Q of the inductor in the LC tank. Thus, the inductance cannot be too big. This is because large inductance will make the Q_{RLC} very low. At the same time, small inductances (e.g. below 500pH) are impractical. Therefore, the challenge is to find the optimum inductance and proper bias point that can provide high G_m for the LNA-mixer block. Also, current source transistor with large width is needed to reject flicker noise, and relatively small width LNA input transistors are preferred to reduce LNA noise figure. In order to overcome the above challenges, the design methodology in the following section will be applied in the design process

C. Design Methodology

Design goal of the LNA is to have low noise figure and acceptable gain while maintaining power match. Since the designer has very limited control over the Q of the inductor and also has no control over how the inductor can be implemented. Therefore, it is advisable to first choose the source and gate inductance that will provide the appropriate quality factor. In the LNA-mixer block, M_b and $M_{RF1,2}$ must be operated in saturation region, so the switching pairs of the mixer can be biased to operate in triode region in order to save voltage headroom. Current mirrors are used to bias M_b and $M_{RF1,2}$ in order to provide stable bias points. Current budget for the QLMV cell is about 2mA, and upper bound of the LNA-mixer voltage headroom is set to be no more than 0.6V in order to save headroom for the QVCO. After choosing the inductance, C_{gs} can be designed according to the resonance constraint provided by (4). Transistor width of $M_{RF1,2}$, W_{RF} , can be found according to

$$C_{gs} = C_{gsw} \cdot W_{RF} \quad (11)$$

where C_{gsw} is the gate to source capacitance per unit width

The required g_m value can be found by

$$R_s = (g_m / C_{gs}) L_s \quad (12)$$

Next step is to use large signal analysis to find the right size of the current source transistor that can provide the required g_m value while keeping in mind that size of this transistor should be large in order to reject flicker noise as mentioned above.

After calculating the design parameters, we ran simulations to verify that M_b and $M_{RF1,2}$ are both operating in saturation

region. The noise figure at 3MHz versus VCO input power is shown in Fig. 7.

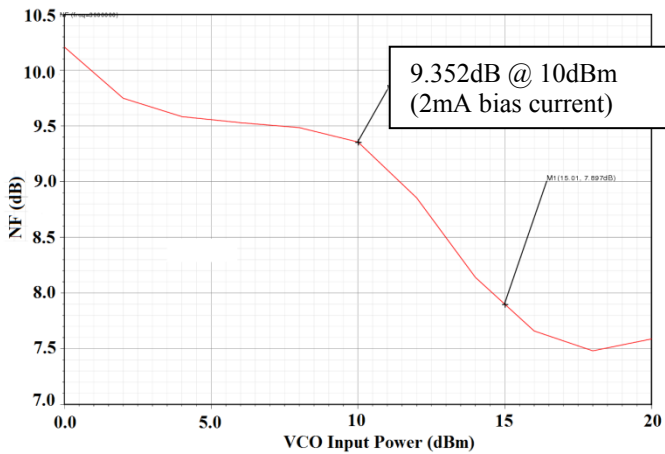


Fig. 7 Mixer's noise figure

V. SIMULATIONS & RESULTS

The GPS receiver front end was simulated with IBM 0.13 μm CMOS process. The layout of our QLMV is shown in Fig. 8. The die area is 1460 μm x 720 μm . The circuit is drawing a current of 2.14mA with a supply voltage of 1V. Thus, the power consumption of the QLMV cell is 2.14mW.

Fig. 9 shows the output signals (I+, Q+, I-, Q-) of the QVCO oscillating at a frequency of 1.5712GHz with almost 90° phase difference. We were not sure how to use Cadence to measure the phase error directly. But from looking at the plot of Fig. 9, we calculated the quadrature phase error to be less than 4°. Fig. 10 shows the measured phase noise; it is -112.3 dBc/Hz, which is lower than measured data of [1] and [4]. Therefore, our circuit is capable of providing low phase noise, high quadrature accuracy, and low power.

However, the noise figure of 48dB (Fig.11) is far too big for a receiver front-end. We believe that this is because both the source inductance and the transistor sizing of the LNA were not optimal. As a result, the gain of the first stage was not large enough to minimize noise contributions from the mixer and QVCO. More effort should also be spent on enhancing the quality factors of the input matching and the LC tank to improve the noise performance of the QLMV cell.

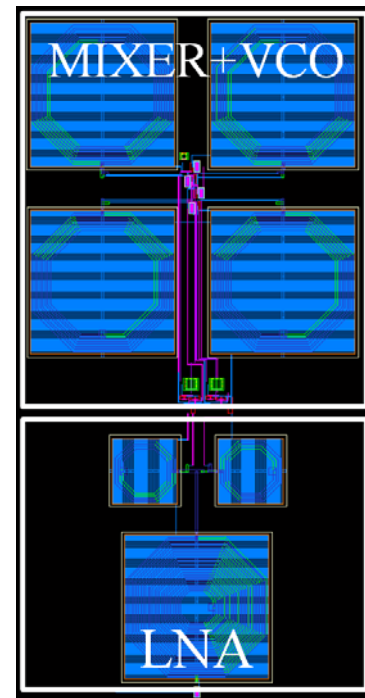


Fig. 8 QLMV cell layout

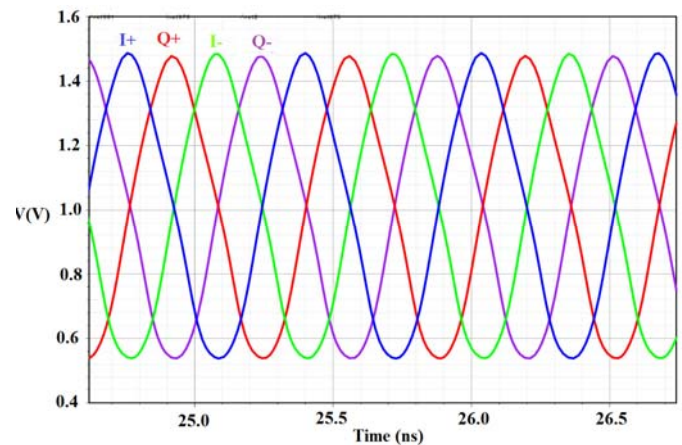


Fig. 9 QVCO output signals

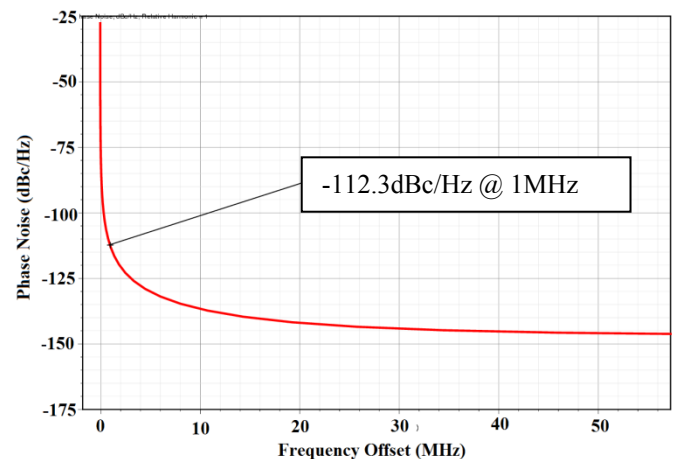


Fig. 10 Measured phase noise

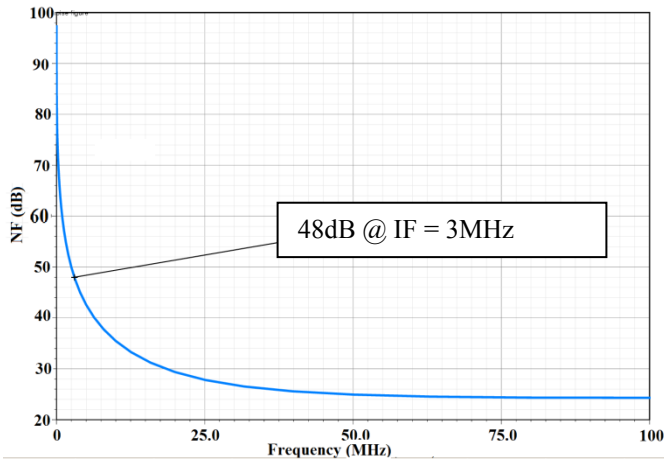


Fig. 11. QLMV noise figure

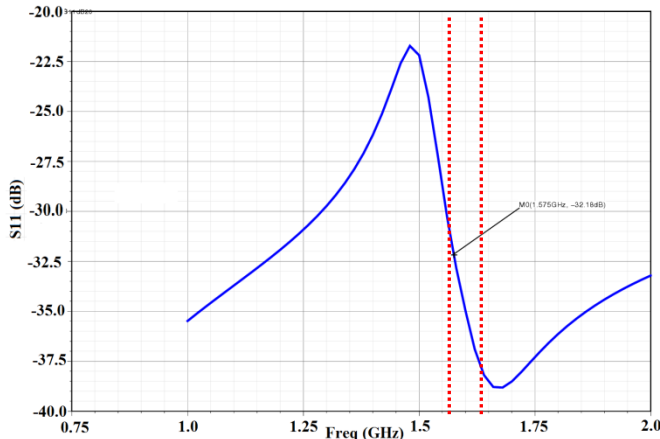


Fig. 12. S11 result

Fig.12 shows the input matching of the receiver. It is well matched to 50Ω around the L1-band GPS carrier frequency of 1.57542GHz; i.e., S_{11} is less than -30 dB from 1.55GHz to 1.65GHz.

VI. DATA COMPARISON

	This Work	[1]	[4]
Technology	0.13 μ m CMOS		
RF frequency	1.57542GHz		
Power (mW)	2.14	1	5.4
Conversion Gain (dB)	27.7 ¹	42.5	36
Phase Noise @ 1MHz (dBc/Hz)	-112.3	-110	-104
NF (dB)	48	6.5	4.8
P1dB (dBm)	-68	-40	-31
IIP3 (dBm)	-57	-30	-19
S11 (dB)	< -30	< -10	< -10
Current (mA)	2.14	1	4.5
Supply Voltage (V)	1	1	1.2
Area (mm ²)	1.05	-	1.5

Table. 1 Data Comparison

1 - Calculated from transient analysis

VII. CONCLUSION

We were able to design, simulate, and layout a stacked

quadrature LMV cell in less than a month. The novel design of the gate-modulated QVCO along with double-balanced mixer provided low phase noise and accurate quadrature signals. The receiver also managed to achieve minimal power consumption. Given more time, we would like to analyze the circuit further to improve its noise figure. A potential future work would include integrating fully differential transimpedance amplifiers to maintain high sensitivity.

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