Chopper–CDS Amplifier

Group 3
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Chopper Amplifier

- Input signal is at near DC (e.g. EEG)
- Up-convert before amp. to avoid 1/f noise

[1] JSSC '10
Chopper

- Similar to commutating mixer

\[ V_{CH} = \text{sign}(\phi_1) V_{SIG} \]
Correlated Double Sampling

- Down-conversion by sampling
- Add a zero at DC

\[ V_{out} = V_{in} \left[ 1 - z^{-\frac{1}{2}} \right] \]
Chopper + CDS operation

- $V_{in} = \text{sign}(\phi_1) V_{SIG} + V_{os} + V_n$
- $V_{out} \sim (1 - z^{-1/2})V_{os} + (1 - z^{-1/2})V_n + (1 + z^{-1/2})V_{SIG}$

  0          HPF          2

- DC offset $V_{os}$ is cancelled
- Noise $V_n$ is filtered (suppress 1/f)
- Signal doubles (6 dB gain)
  (since signal changes sign every half cycle)
Signal Transfer function

- +6dB signal gain at low frequency
Noise Transfer Function

- Filter out noise and DC at amp output
Chopper vs. CDS
Amplifier Design

- Large offset $\rightarrow$ output saturation
- Bandpass response is required

![Amplifier Design Graph]

$51\text{dB} @ 400\text{kHz (}f_{ch}\text{)}$
Bandpass Telescopic Amp.

Gain suppression @ low freq.

DC : source degeneration
AC : differential pair

[1] JSSC '10
Circuit Implementation

1st order RC LPF

CMFB

$V_{out}^-$

$V_{CM}$

$V_{out}^+$

$V_{in}^+$

$V_{in}^-$

$V_{out}$
Input Offset w/o BPF

- Monte Carlo

\[ \text{\# of iteration : 10K} \]
\[ \mu = 10.54 \mu V \]
\[ \sigma = 1.65 mV \]
AC Simulation w/ Offset

Conventional Amp.

No offset

1σ

6σ

This work (BP Amp.)

0σ~ 6σ
Tran. Simulation w/ Offset

Conventional Amp.

This work (BP Amp.)

No offset

0σ~ 6σ
Chopping Clock Generator

- Constant current reference
- Current starved inverter ring oscillator
- Temperature-insensitive clock

[2] CICC ‘08
Optimal Chopping Freq.

- Gain $> \text{Max} - 3\text{dB}$ $\Rightarrow f_{\text{CH}} = 400\text{kHz}$
- Min. input-referred noise density $= 22.3\text{nV}/\sqrt{\text{Hz}}$

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PNOISE Simulation

Noise Density (V/sqrt(Hz))

Input-referred
Output-referred

22.9nV/√Hz

f_{CH} = 400kHz
Chip Layout

- Circuit blocks
  - Bandpass Amp.
  - Clock generator
  - Chopper
  - CDS

- Area: $228\mu m \times 288\mu m$
- Symmetric Signal Path
## Performance Summary

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<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Process [µm]</td>
<td>0.13</td>
<td>0.18</td>
<td>0.35</td>
<td>0.70</td>
<td>0.35</td>
</tr>
<tr>
<td>V_{DD} [V]</td>
<td>1.2</td>
<td>1.8</td>
<td>5.0</td>
<td>5.0</td>
<td>1.8</td>
</tr>
<tr>
<td>Input Noise [nV/√Hz]</td>
<td>23</td>
<td>37</td>
<td>6</td>
<td>11</td>
<td>95</td>
</tr>
<tr>
<td>I_{DD} [µA]</td>
<td>13.5 (*26.9)</td>
<td>14.4</td>
<td>1500</td>
<td>143</td>
<td>13</td>
</tr>
<tr>
<td>FOM (V_{NI}^2/Δf)* I</td>
<td>7.1 (*14.1)</td>
<td>19.7</td>
<td>51.2</td>
<td>15.8</td>
<td>117</td>
</tr>
<tr>
<td>f_{CH} [kHz]</td>
<td>400</td>
<td>500</td>
<td>200</td>
<td>30</td>
<td>50</td>
</tr>
<tr>
<td>DC Gain [dB]</td>
<td>56</td>
<td>168</td>
<td>150</td>
<td>100</td>
<td>130</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.06</td>
<td>1.14</td>
<td>1.26</td>
<td>1.8</td>
<td>0.64</td>
</tr>
</tbody>
</table>

* Current consumption is doubled for only 1st stage design
Reference


