Chopper–CDS Amplifier

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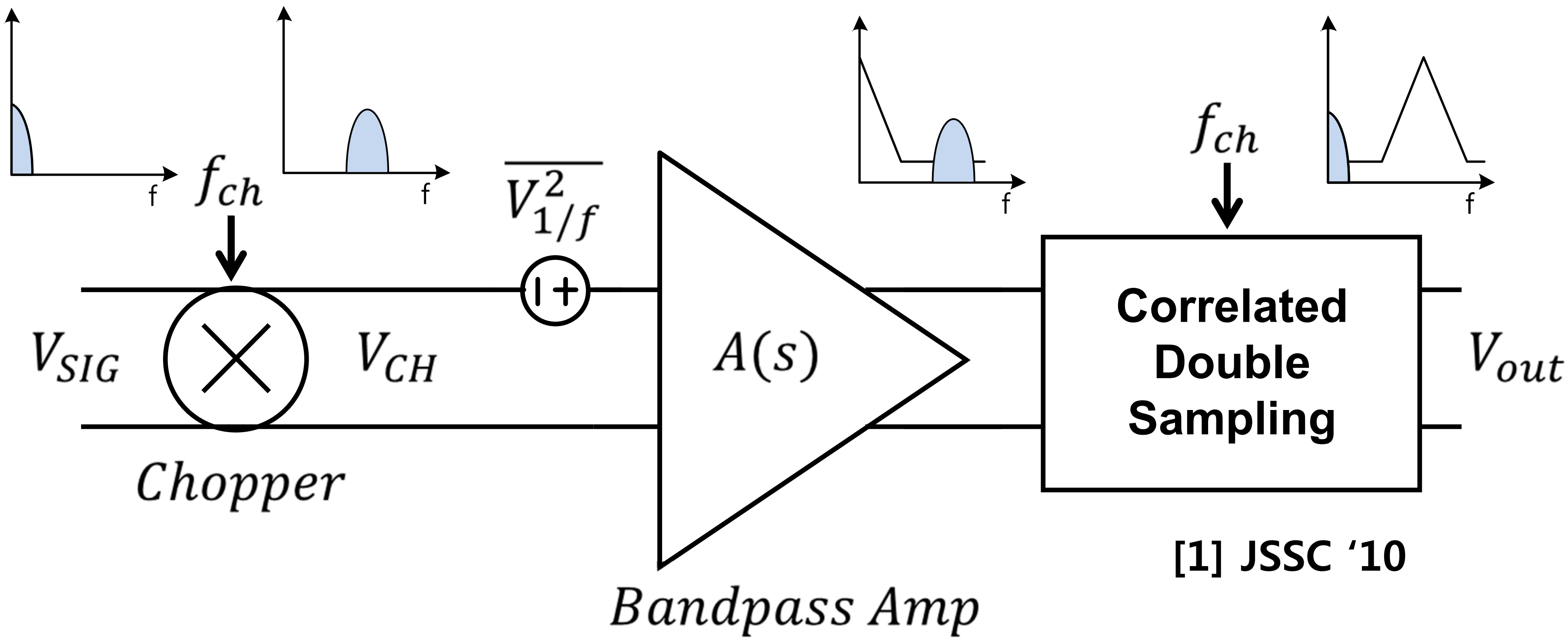
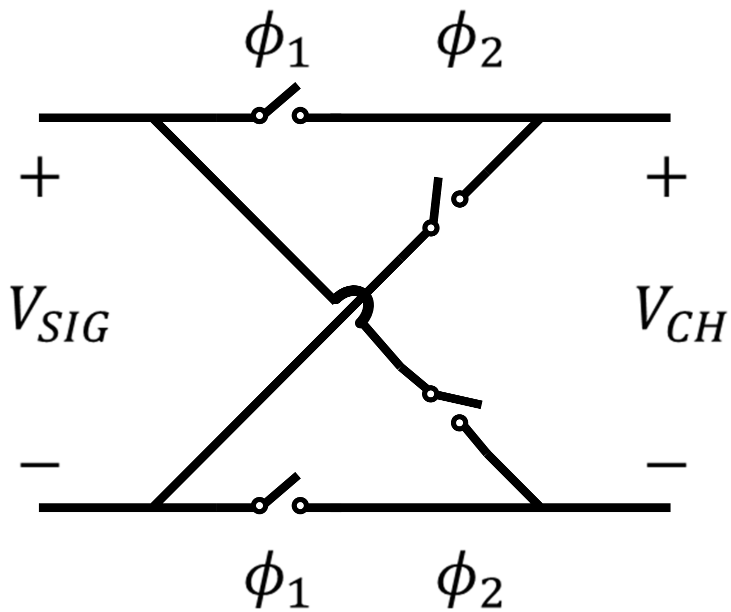
Chopper Amplifier

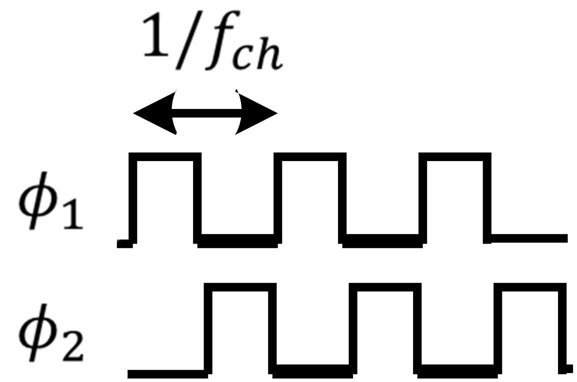
- Input signal is at near DC (e.g. EEG)
- Up-convert before amp. to avoid 1/f noise



Chopper

- Similar to commutating mixer

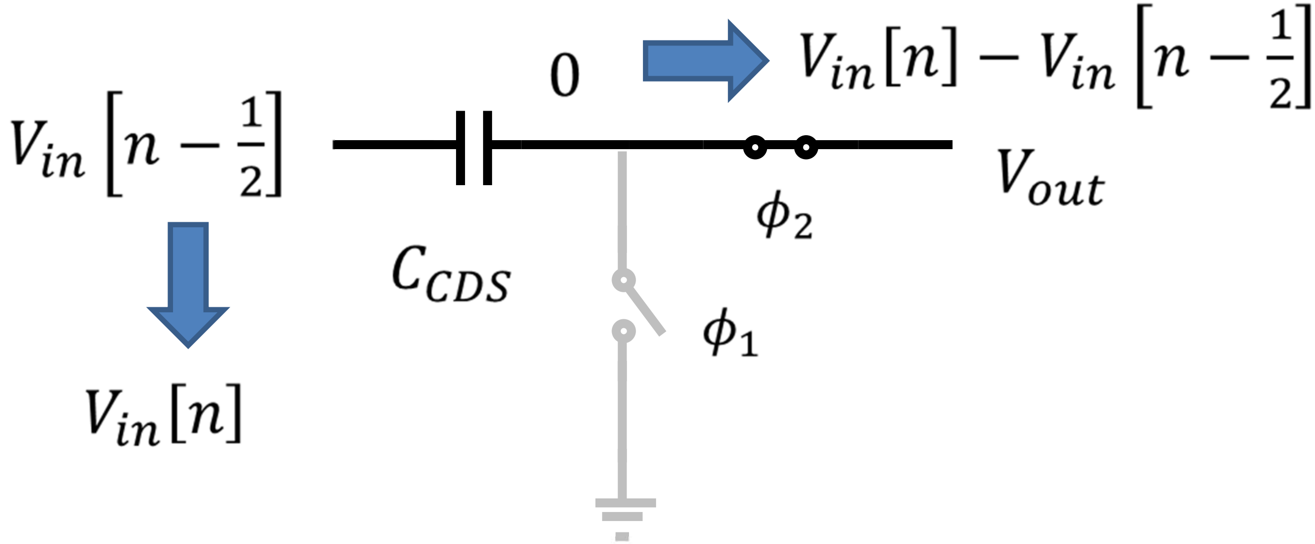




$$V_{CH} = sign(\phi_1)\, V_{SIG}$$

Correlated Double Sampling

- Down-conversion by sampling
- Add a zero at DC



$$V_{out} = V_{in}\left[1 - z^{-\frac{1}{2}}\right]$$

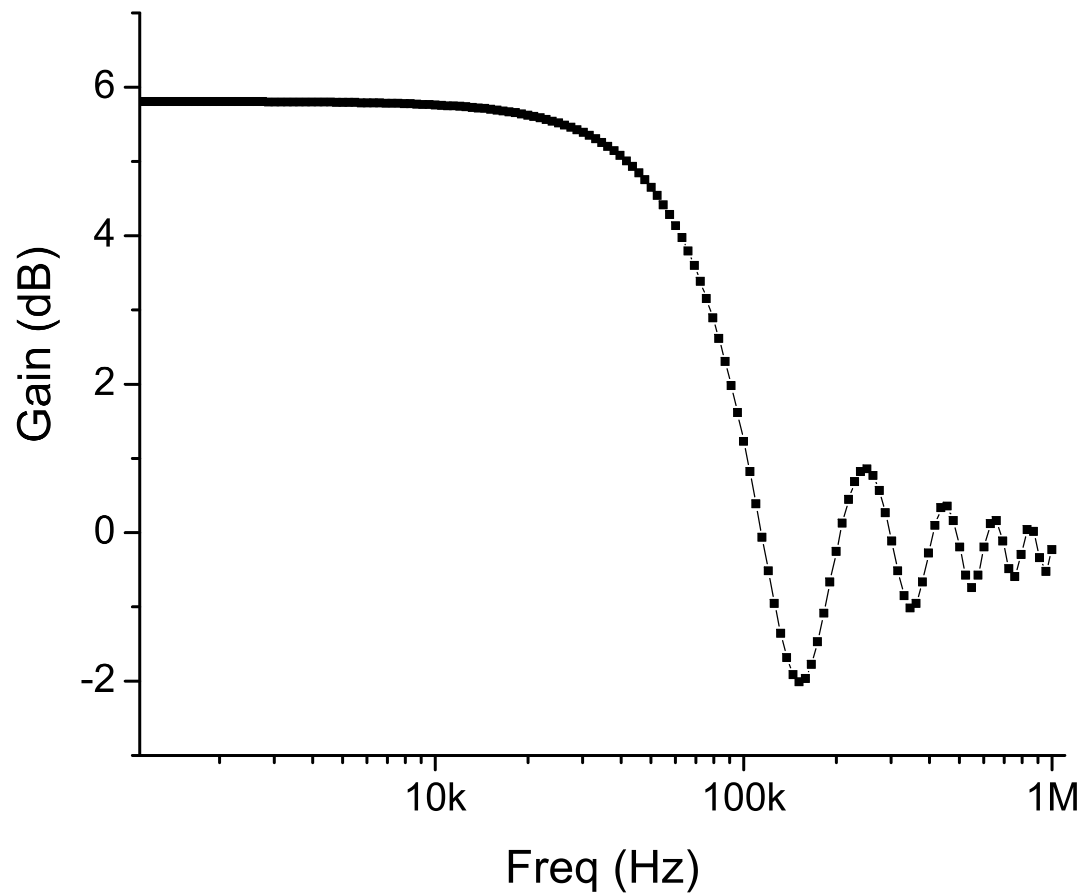
Chopper + CDS operation

- $V_{in} = sign(\phi_1)\, V_{SIG} + V_{os} + V_n$
- $V_{out} \sim \underbrace{(1 - z^{-1/2})}_{0} V_{os} + \underbrace{(1 - z^{-1/2})}_{HPF} V_n + \underbrace{(1 + z^{-1/2})}_{2} V_{SIG}$

  - DC offset V_{os} is cancelled
  - Noise V_n is filtered (suppress 1/f)
  - Signal doubles (6 dB gain)
    (since signal changes sign every half cycle)

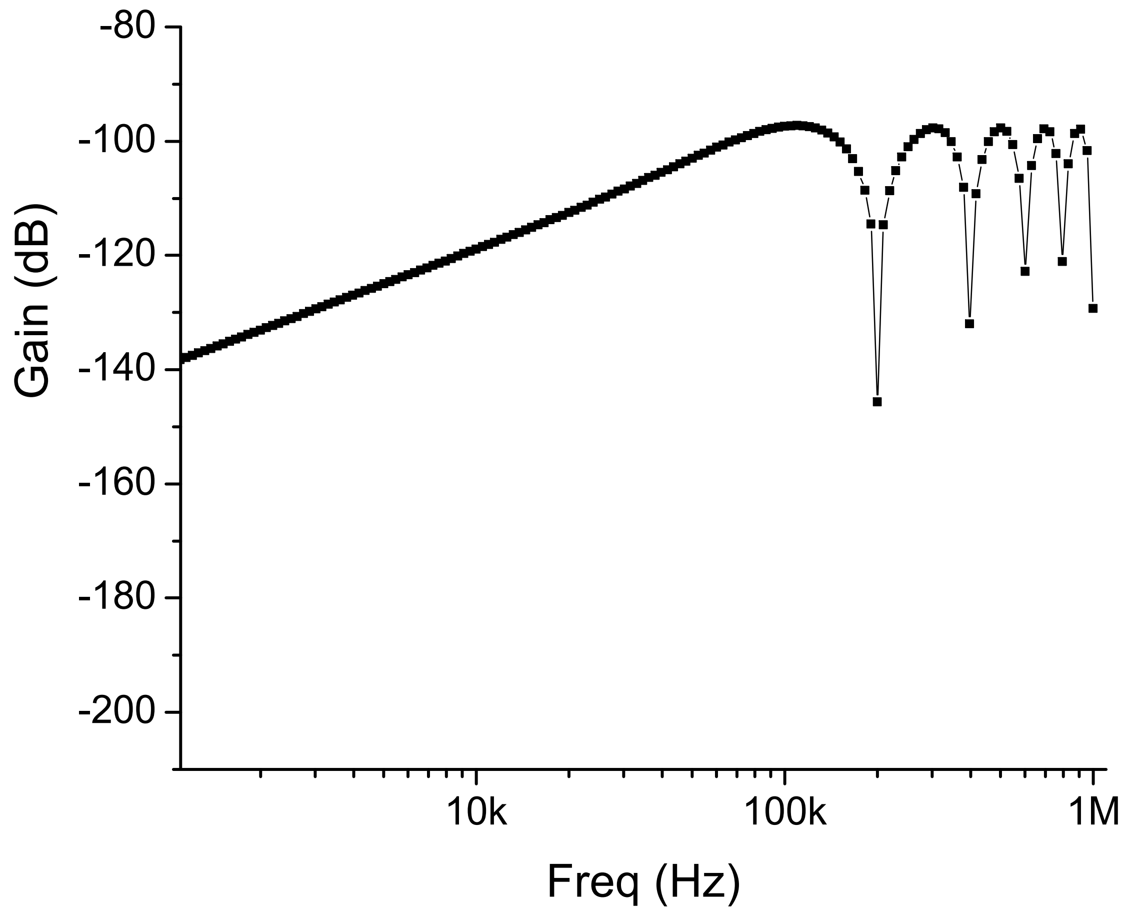
Signal Transfer function

- +6dB signal gain at low frequency

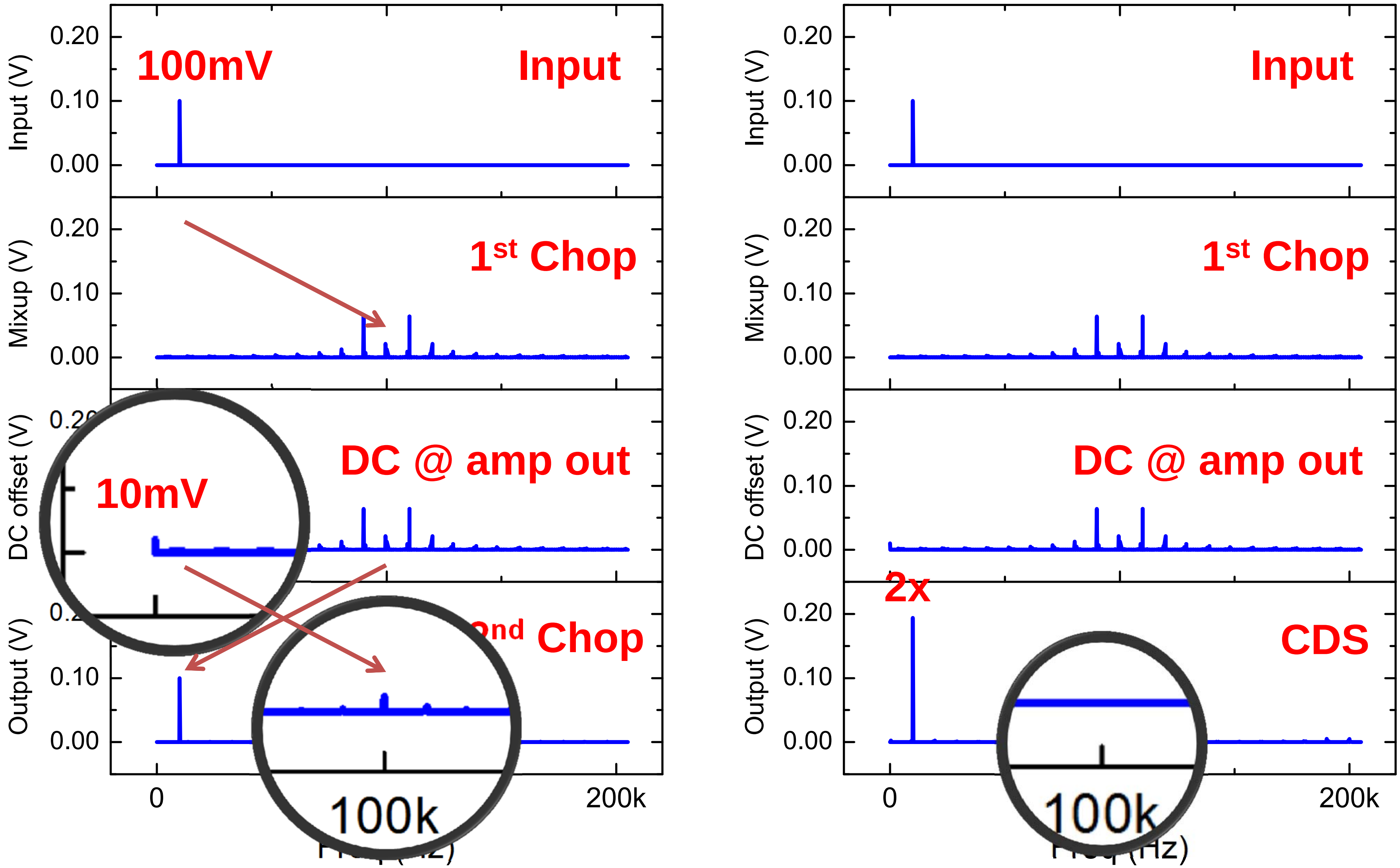


Noise Transfer Function

- Filter out noise and DC at amp output

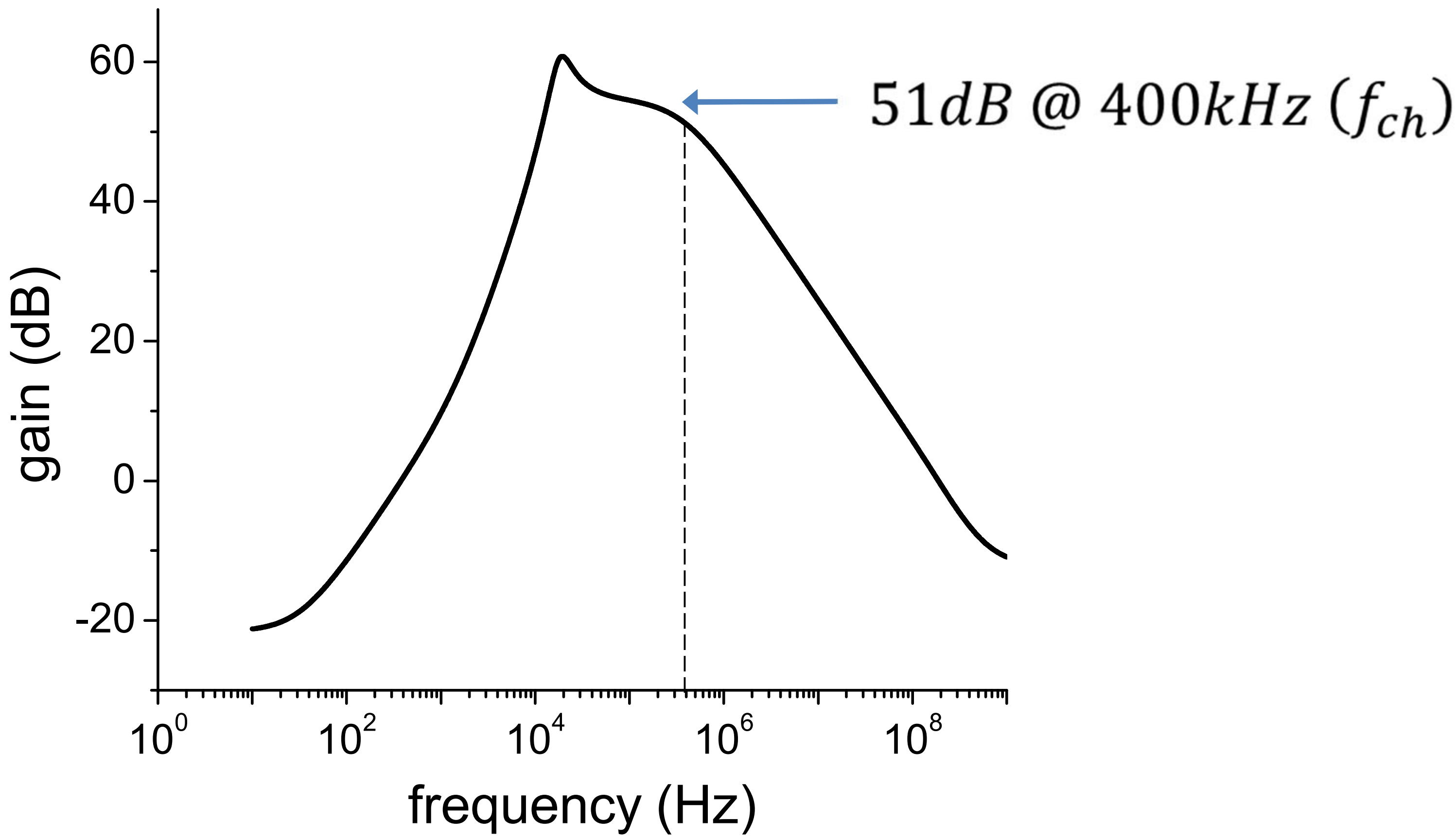


Chopper vs. CDS



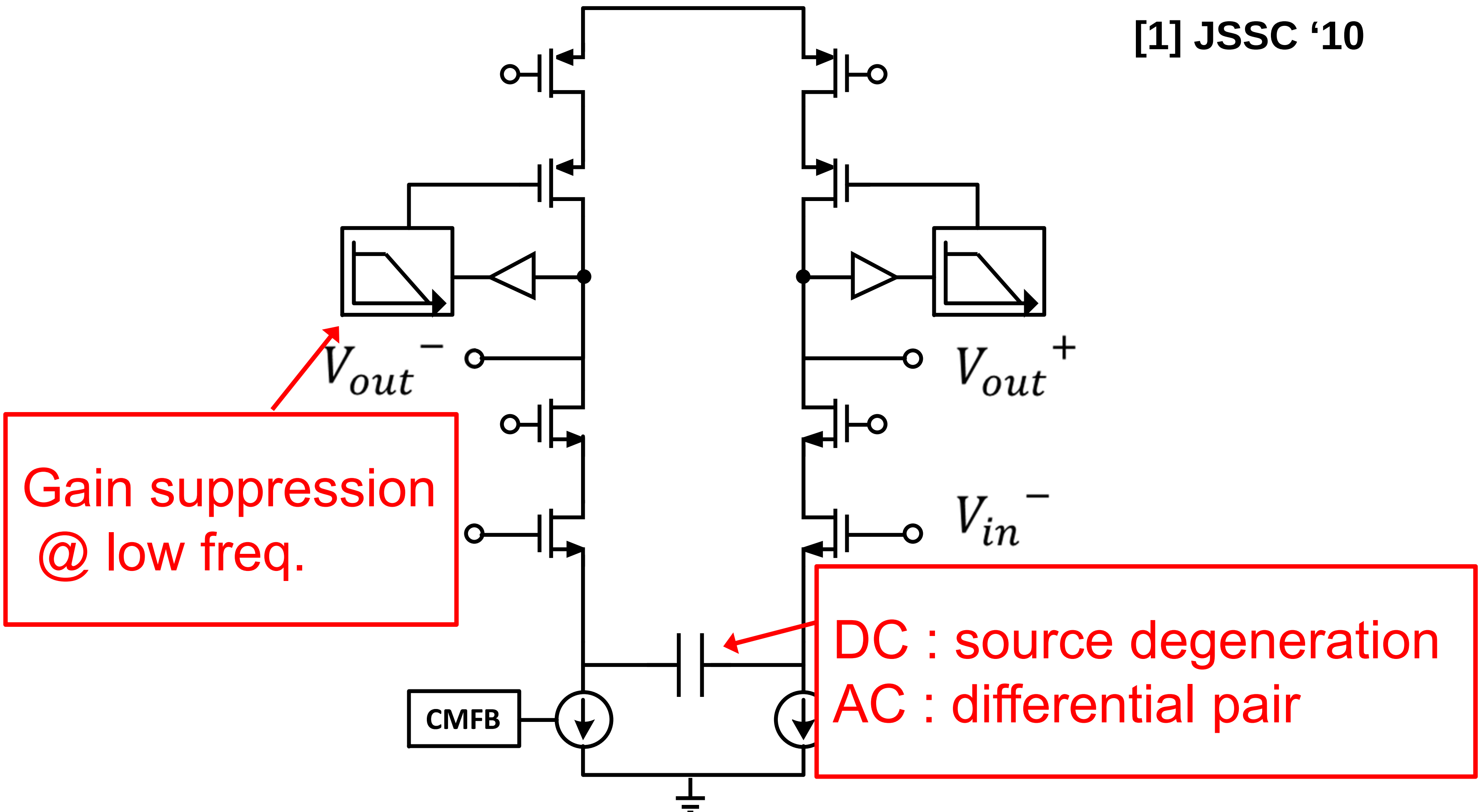
Amplifier Design

- Large offset → output saturation
- Bandpass response is required

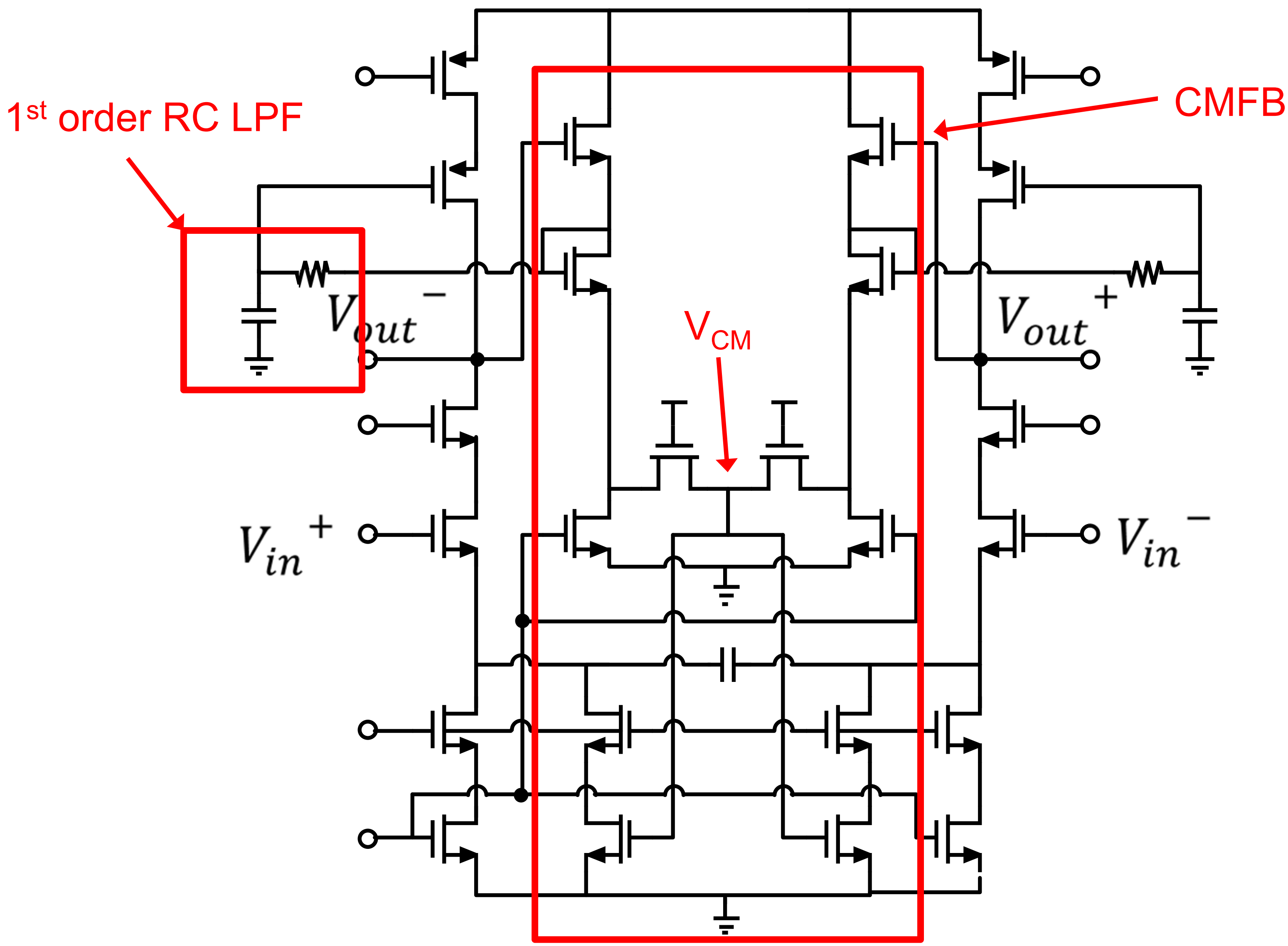


Bandpass Telescopic Amp.

[1] JSSC '10



Circuit Implementation

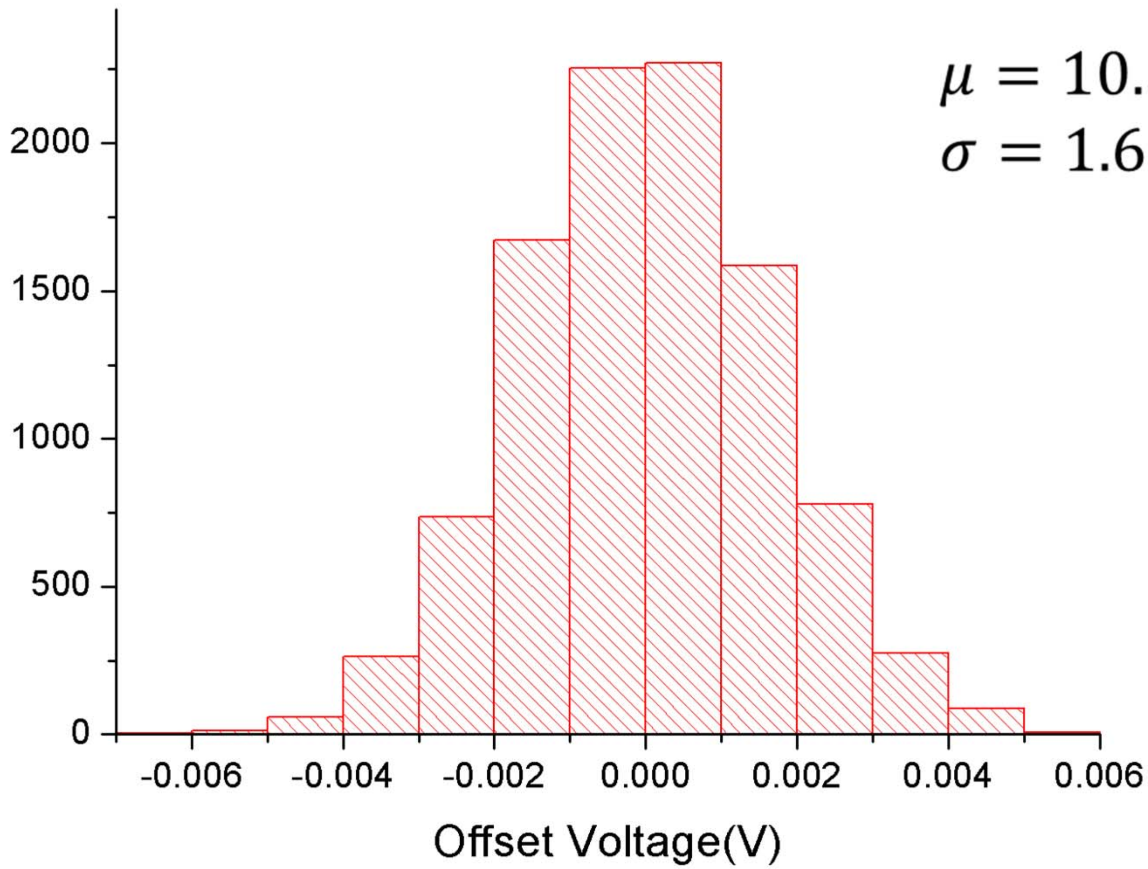


Input Offset w/o BPF

- Monte Carlo

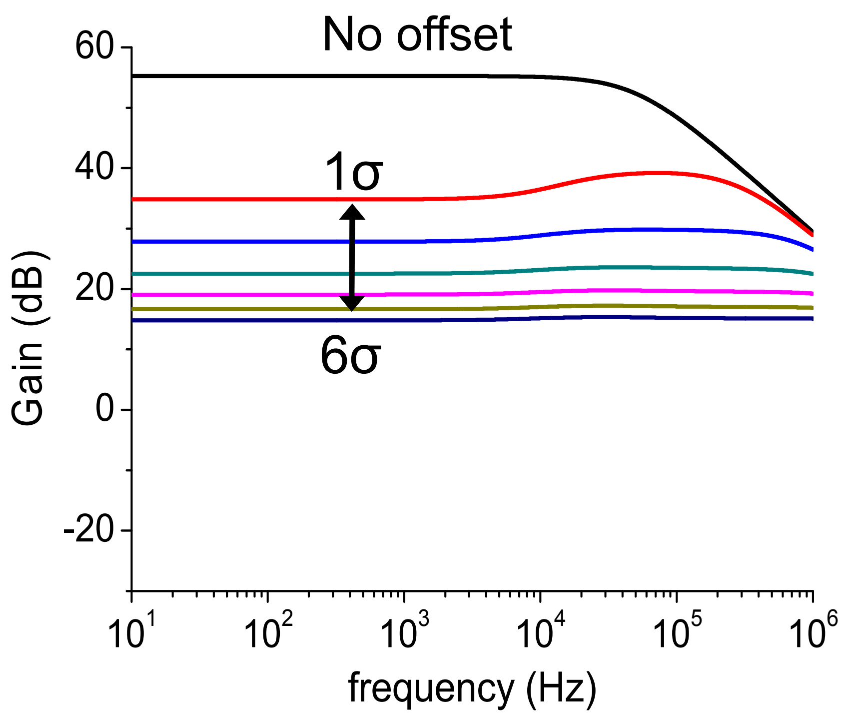
# of iteration : 10K

$$\mu = 10.54\mu V$$
$$\sigma = 1.65mV$$

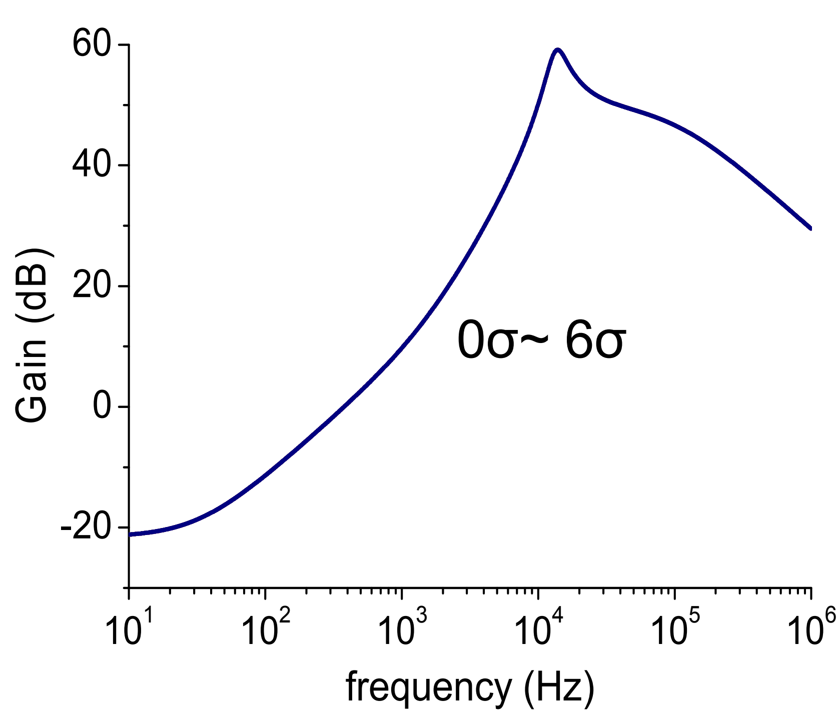


AC Simulation w/ Offset

Conventional Amp.

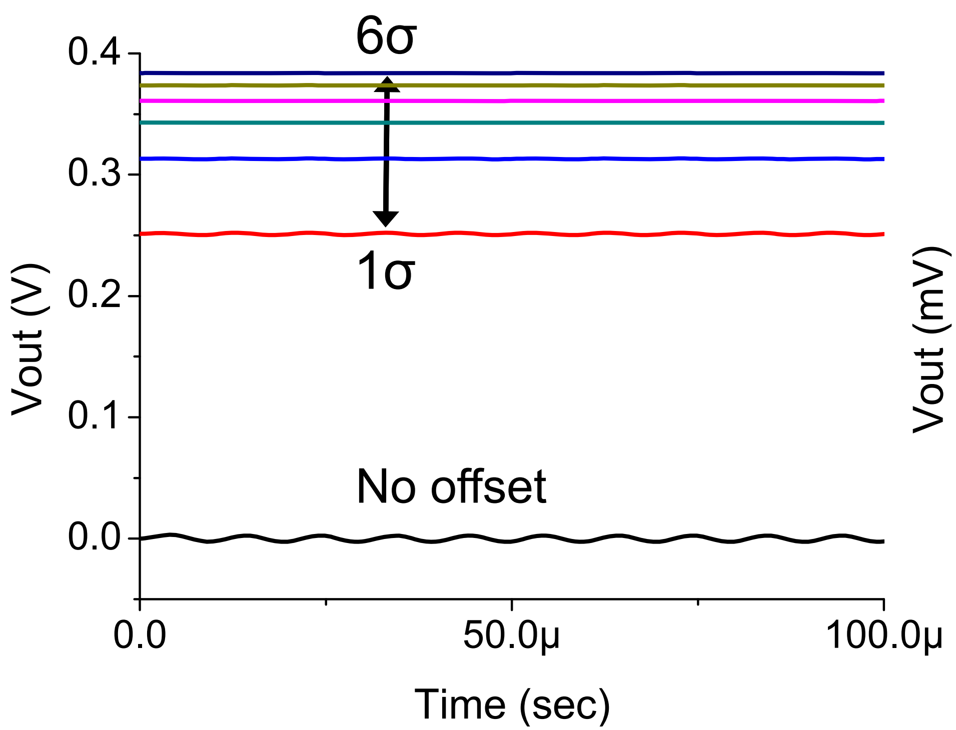


This work (BP Amp.)

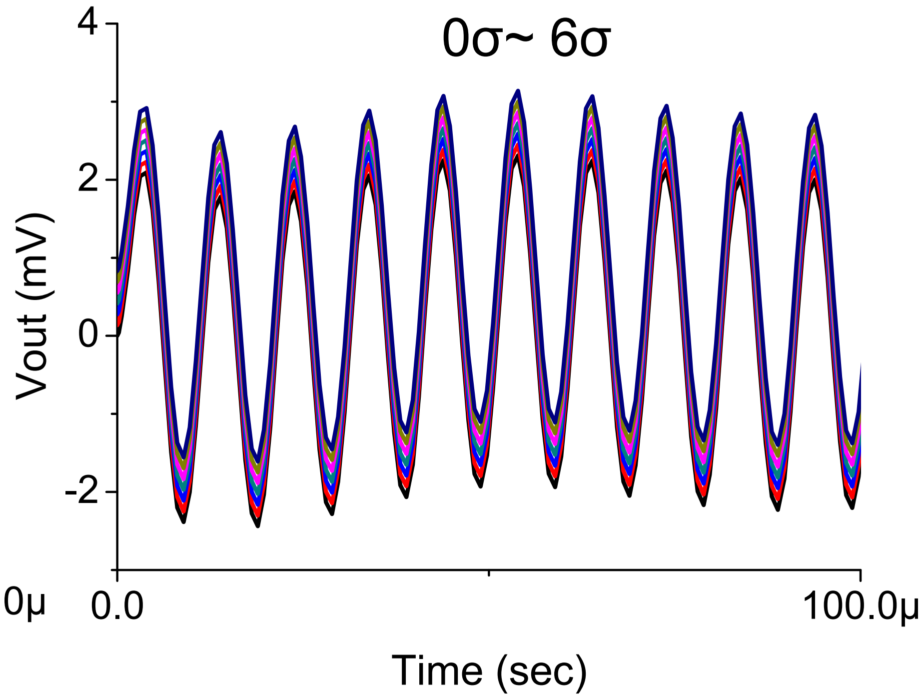


Tran. Simulation w/ Offset

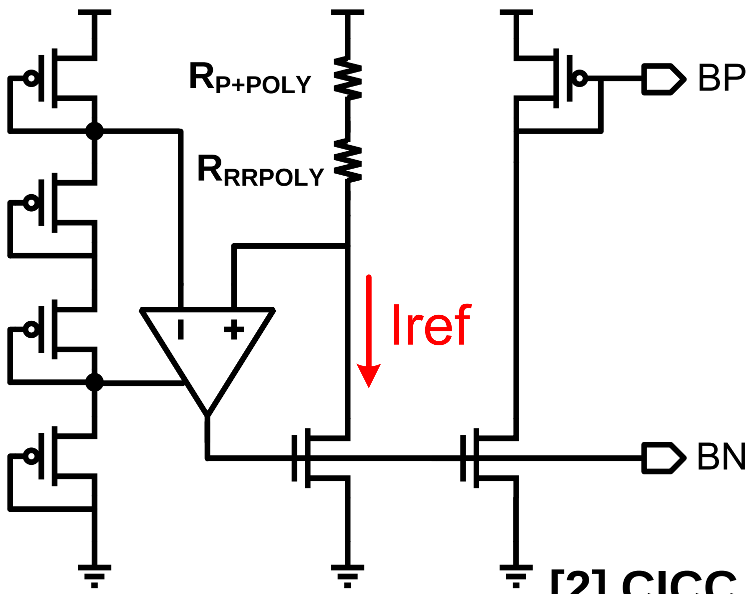
Conventional Amp.



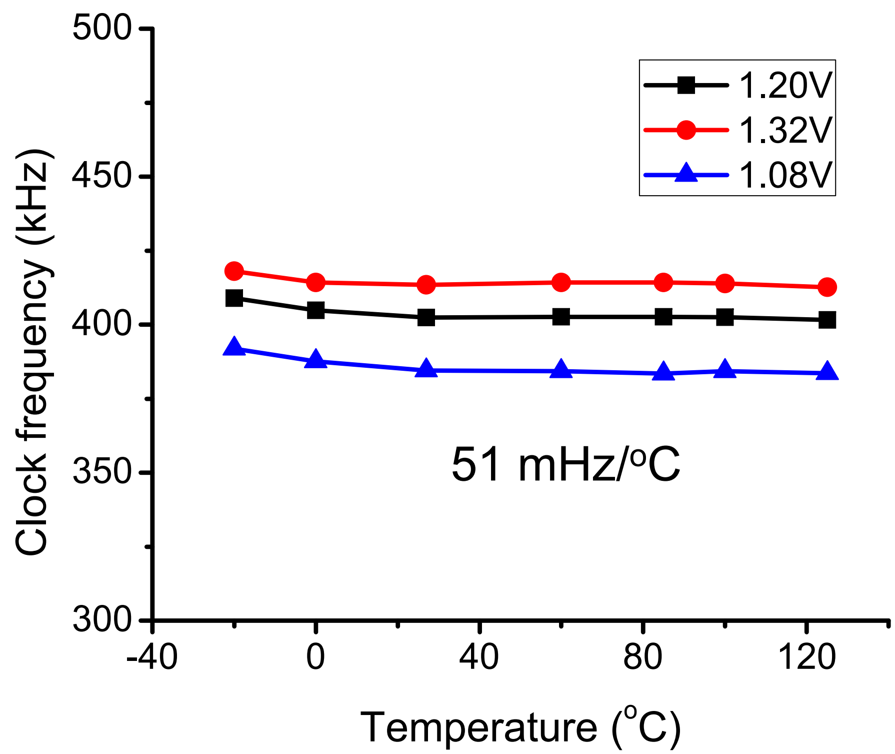
This work (BP Amp.)



Chopping Clock Generator

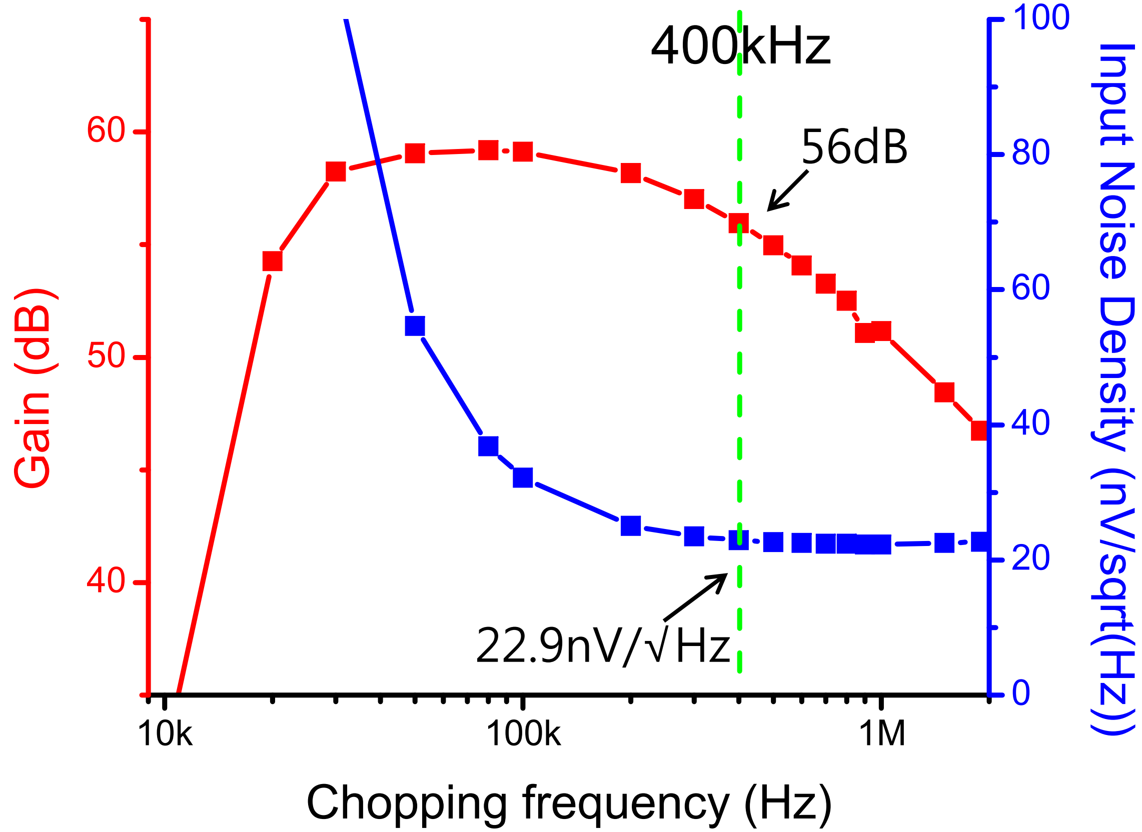


[2] CICC '08



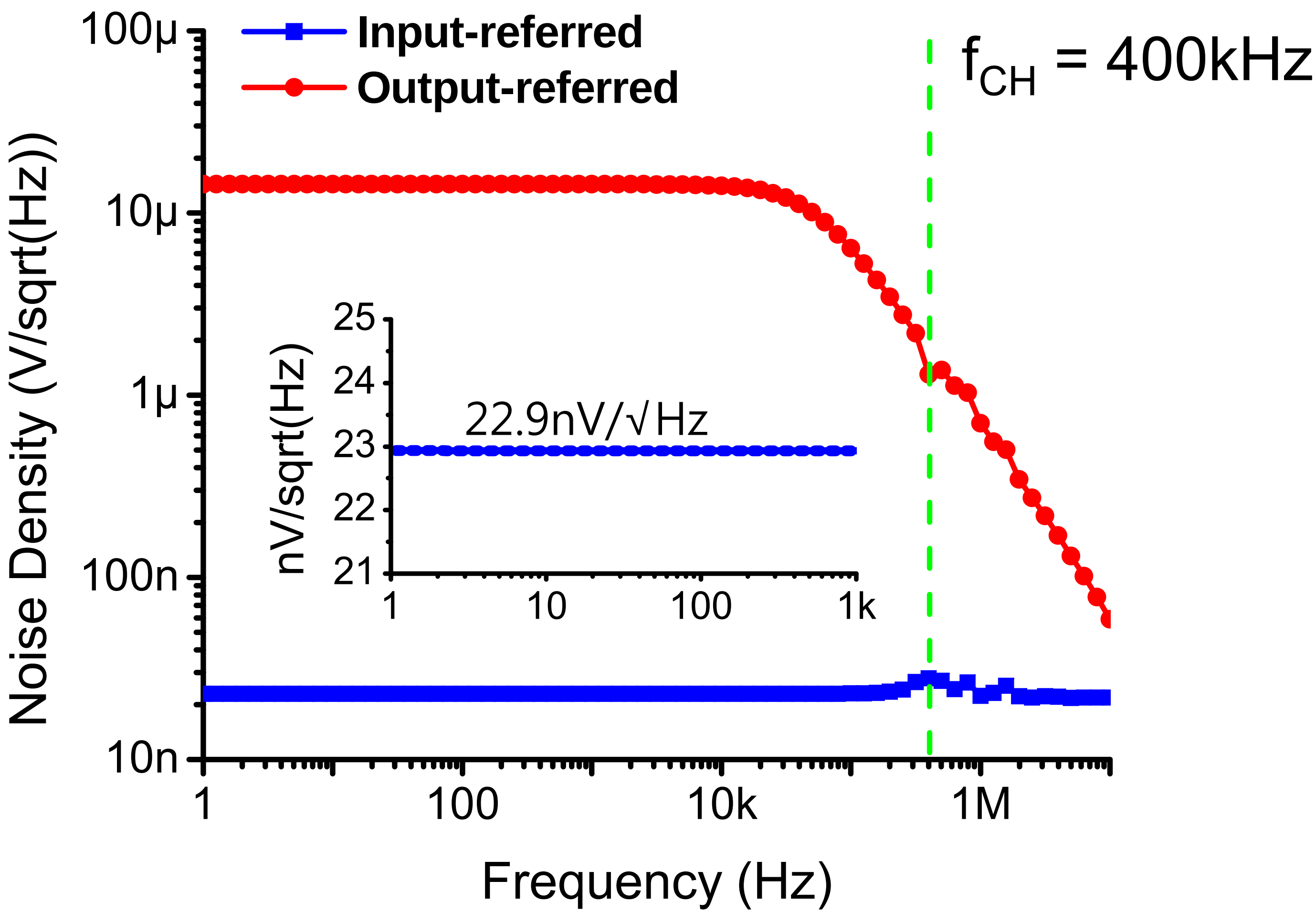
- Constant current reference
- Current starved inverter ring oscillator
- Temperature-insensitive clock

Optimal Chopping Freq.



- Gain > Max – 3dB → f_{CH} = 400kHz
- Min. input-referred noise density = 22.3nV/√Hz

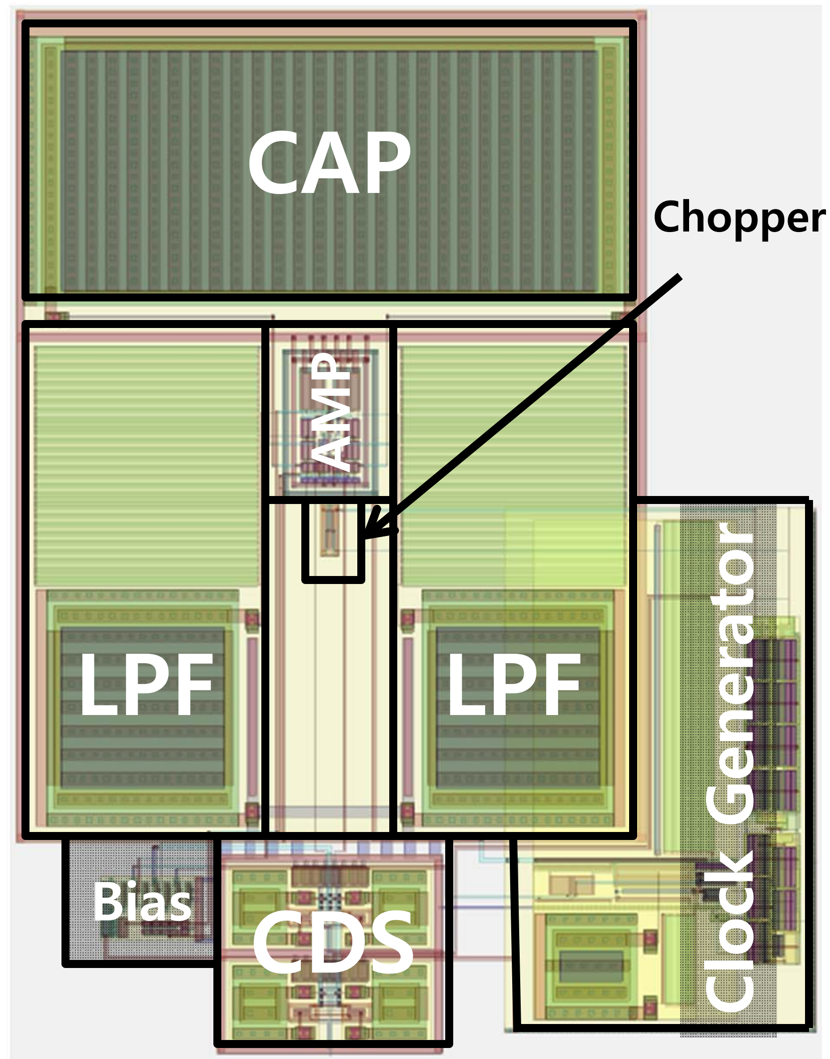
PNOISE Simulation



Chip Layout

- Circuit blocks
  - Bandpass Amp.
  - Clock generator
  - Chopper
  - CDS

- Area : 228μm x 288μm
- Symmetric Signal Path



Performance Summary

	This Work	JSSC '10 [1]	ISSCC '11 [3]	ISSCC '10 [4]	JSSC '10 [5]
Process [μm]	0.13	0.18	0.35	0.70	0.35
V_{DD} [V]	1.2	1.8	5.0	5.0	1.8
Input Noise [nV/√Hz]	23	37	6	11	95
I_{DD} [μA]	13.5 (*26.9)	14.4	1500	143	13
FOM $(V_{NI}^2 /\Delta f)^* I$	7.1 (*14.1)	19.7	51.2	15.8	117
f_{CH} [kHz]	400	500	200	30	50
DC Gain [dB]	56	168	150	100	130
Area [mm²]	0.06	1.14	1.26	1.8	0.64

* Current consumption is doubled for only 1st stage design

Reference

[1] M. Belloni, E. Bonizzoni, A. Fornasari, and F. Maloberti, "A Micropower Chopper—CDS Operational Amplifier", *IEEE J. Solid-State Circuits*, vol. 45, no 12, pp. 2521-2529, Dec., 2010.

[2] Y. Lin, D. Sylvester, and D. Blaauw, “An Ultra Low Power 1V, 200nW Temperature Sensor for Passive Wireless Application,” *CICC*, pp. 507-510, Sept., 2008.

[3] Y. Kusuda, “A 5.9nV/√Hz Chopper Operational Amplifier with 0.78μV Maximum Offset and 28.3nV/°C Offset Drift,” *ISSCC Dig. Tech. Papers*, pp. 242-243, Feb., 2011.

[4] Q. Fan, J.H. Huijsing, and K.A.A. Makinwa, “A 21nV/√Hz Chopper-Stabilized Multipath Current-Feedback Instrumentation Amplifier with 2μV Offset,” *ISSCC Dig. Tech. Papers*, pp. 80-81, Feb., 2010.

[5] Y. Kusuda, “Auto Correction Feedback for Ripple Suppression in a Chopper Amplifier,” *IEEE J. Solid-State Circuits*, vol. 45, no 8, pp. 1436-1445, Aug., 2010.