A Chopper-CDS Amplifier

Jihyun Cho, Jaeyoung Kim, and Inhee Lee

***Abstract*— µV-level signals from sensors are amplified by many instrumentation amplifiers, which require high gain, low offset, and low input noise. µW-level power is also needed for portable applications. In this paper, a low power spur-free precision amplifier is designed using two offset cancellation technique, chopper stabilization and correlated double sampling (CDS). CDS cancels its offset and low frequency noise by 1-z^{-1} while the combination method processes input signals by 1+z^{-1}. The amplifier has low DC gain to prevent output saturation, but has high gain at the chopping frequency for input signals. A temperature-insensitive clock generator is included to reduce variation of the chopping frequency over temperature. The proposed circuit, designed in 0.13 µm CMOS process, consumes 13.5 µA with 1.2 V supply voltage and achieves the input-referred noise density of 22.9 nV/√Hz.**

***Index Terms*—Chopper, CDS, low-noise amplifier, low offset, ripple reduction.**

I. Introduction

In many applications, such as biosensors, the input offset and noise of the first amplifier limits the overall performance. Many offset-cancellation and noise rejection techniques have been proposed [1]-[5]. These techniques can generally be categorized into two parts: autozero technique and chopper technique. Autozeroing includes correlated double-sampling (CDS) [2],[3], and a ping-pong opamp [4], while chopper includes a chopper amplifier [1],[5], and chopper-stabilization [2].

A. Autozeroing

The basic principle of autozeroing is to cancel the offset in two phases. During the two phases, the one sampled data is subtracted from the other so that the offset is cancelled out. In addition, the 1/*f* noise is also removed during autozeroing. However, there is a limitation that the sampling frequency should be quite larger than the 1/*f* corner frequency, and the reduced 1/*f* noise is still higher than the thermal noise at higher frequency.

B. Chopping

Chopping is another technique to reject 1/*f* noise. The input signal is up-converted to the chopping frequency, amplified, and down-converted to the baseband. During the process, 1/*f* noise is not amplified, while amplifying the input signal. Still, the offset exists at the chopping frequency and its odd harmonics after demodulating the input signal.

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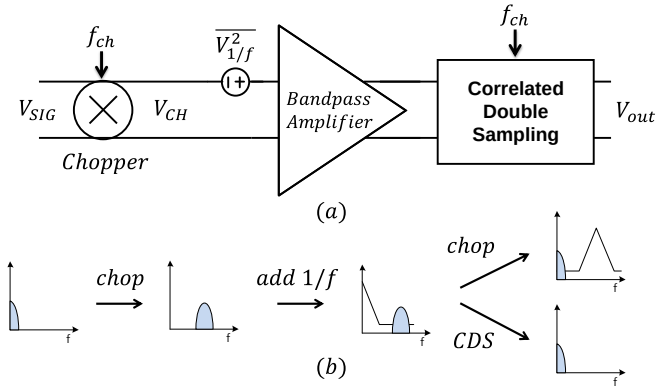

Fig. 1. (a) Overall block diagram of Chopper-CDS amplifier [1] (b) signal spectra at each stage.

C. Chopper-CDS

Belloni proposed the chopper-CDS operational amplifier to resolve the limitations of autozeroing and chopping [1]. The input signal is modulated to the chopping frequency by the chopper, amplified by the bandpass amplifier, and demodulated by CDS. The bandpass amplifier is used to prevent output saturation.

In this work, a low power chopper-CDS amplifier is designed. In the section II, the operational principle of chopper, CDS, and their combination is introduced. Section III and IV describes the bandpass amplifier and the temperature-insensitive chopping clock generator, respectively. Simulation results will be shown in section V and is followed by the conclusion in section VI.

II. Chopper and CDS

A chopper amplifier is designed to amplify very low frequency signal such as EEG and ECG. In this frequency range, there is huge 1/*f* noise added by amplifier. If we use a conventional amplifier with low-pass response, the noise and signal cannot be separated by filtering in the following stages. To avoid the 1/*f* noise, a chopper amplifier up-converts the signal before the noise source, in this case the amplifier. Fig. 1 shows an overall block diagram of a chopper-CDS amplifier, and the signal spectra at each stage. At first, a chopper up-converts the baseband signal V_{SIG} to the chopping frequency f_{ch}. Then the chopped signal V_{CH} is amplified by a bandpass amplifier which is designed to have a large gain only near the chopping frequency. Since this amplifier has 1/*f* noise, it will appear in the spectrum of the amplifier output. To make the desired signal at baseband, a down-converter is required at the final stage. It can either be another chopper or CDS, but CDS offers benefits in terms of signal quality [1]. If another chopper is used for down-conversion, it will perform not only the

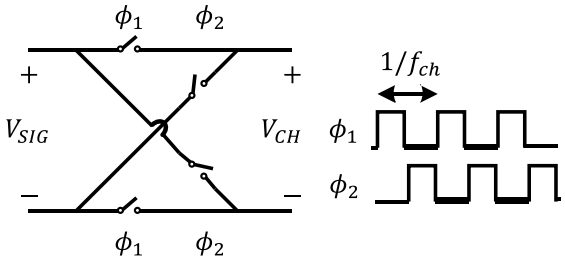

Fig. 2. Chopper and non-overlapping chopping clock

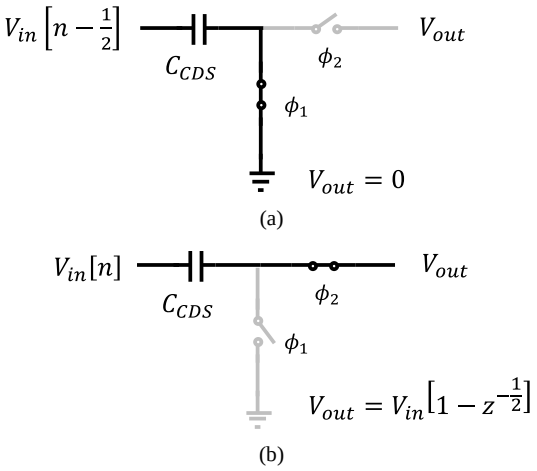

Fig. 3. CDS Operation (a) first sampling (b) second sampling.

down-conversion but up-conversion of the 1/f noise to the chopping frequency, resulting in huge ripple at the output signal. On the other hand, CDS can remove low frequency components at its input, preventing a tone at the chopping frequency. The difference of chopper and CDS as a down-converter is illustrated in Fig. 1(b). Following sub-sections will describe the detailed operation of the chopper, CDS, and combination of them.

A. *Chopper*

A chopper is used to up-convert or down-convert signals. As shown in Fig. 2, a chopper is a commutating mixer with non-overlapping clock signals ϕ_1 and ϕ_2 with chopping frequency f_{ch}. When ϕ_1 is high the output is directly connected to the input whereas it changes the sign during the other phase. The input and the output is related by

$$V_{CH} = sign(\phi_1) \times V_{SIG}. \quad (1)$$

B. *CDS*

CDS provides two functions in this system. First, CDS performs sampling twice, resulting in folding in frequency domain. If we operate this circuit at f_{ch}, it will down-convert the signal from f_{ch} to DC.

The main contribution of CDS in this system is that it filters unwanted signal out and provides an extra gain for desired signal. As shown in Fig. 3, CDS has a series capacitor between the input and the output node. It provides highpass filtering by adding a zero at DC. Fig. 3 describes this operation. During ϕ_1 the input is sampled in C_{CDS}. After a half sample period later, the switch changes, as well as the input signal. During this process, the amount of charge in C_{CDS} should be conserved making the output voltage follow the input voltage change. In this case, the input voltage change is the difference of two sampled signals. As a result, using z-transform, the output voltage can be expressed by

$$V_{out} = V_{in}\left(1 - z^{-1/2}\right). \quad (2)$$

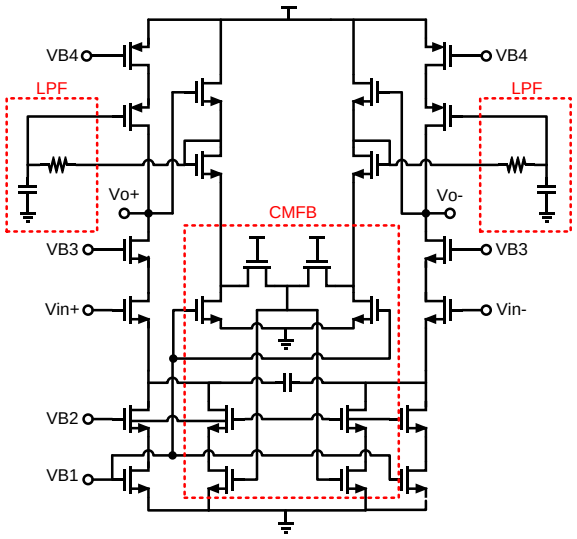

Fig. 4. Differential telescopic amplifier with a lowpass filter and a capacitor coupled to the differential pair [1].

C. *Chopper and CDS combination*

According to the Fig. 1(a), CDS sees three components at its input node, chopped signal V_{SIG}, amplifier offset V_{os}, and 1/f noise V_n. Assuming that the amplifier gain is 1, and from (1) and (2), the output of CDS is

$$V_{CDSout} = (1 - z^{-1})(V_{os} + V_n) + (1 + z^{-1})V_{SIG}. \quad (3)$$

Since the offset voltage is constant, it is completely cancelled by this operation, and the 1/f noise is removed by highpass filtering. In the last term of (3), the transfer function is the sum of two sampled signal, and it is due to the fact that the chopped signal changes its sign every half period of chopping. As a result, the signal of interest doubles at low frequency. In other words, CDS provides 6 dB extra gain.

III. Band Pass Amplifier

Output saturation is one of the main consideration in designing the amplifier. Since the amplifier is used in open loop, meaning that post calibration cannot be applicable, process variation and device mismatch can cause fatal performance degradation. Accordingly, invulnerability to the input offset voltage is critical for implementing the amplifier. Two techniques are used for preventing the saturation of the output signal: lowpass gain suppression and a capacitor coupled to the differential pair.

A. *Lowpass gain suppression*

A low pass filter, a simple RC filter ($R = 10M\Omega, C = 10pF$),

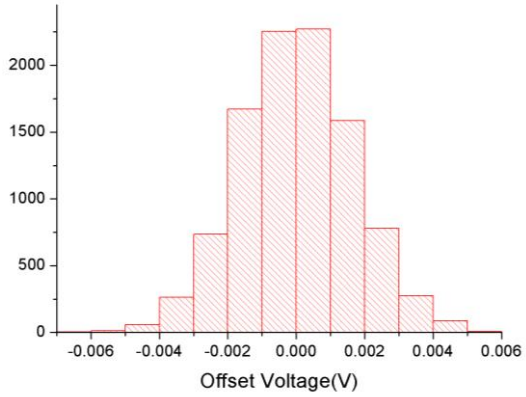

Fig. 5. Monte Carlo Simulation (10k Iterations) ($\mu = 10.54\ \mu V, \sigma = 1.65\ mV$).

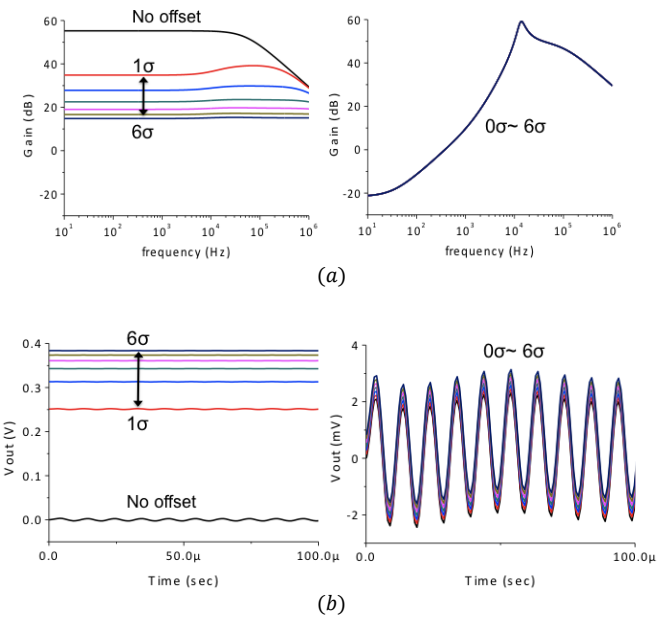

Fig. 6. (a) AC simulation and (b) transient simulation results in both cases: conventional amplifier on the left and the bandpass amplifier on the right.

is connected between the output node and the gate node of a PMOS in Fig. 4. Since the gain of the amplifier is reduced by feedback loop, the gain suppression is limited to low frequency range, while maintaining high gain at the desired frequency.

B. *Capacitor coupled to differential pair*

A capacitor of 150pF is connected between pair in Fig. 4. The capacitor opens each source of the differential pair at DC so that source degeneration drops the overall gain. In contrast, sources are ac-grounded so that the gain at ac is affected by the capacitor, which helps the amplifier to be insensitive to the input offset.

C. *Monte Carlo Simulation*

To simulate the sensitivity of the amplifier to the input offset, its standard deviation due to the process variation and device mismatch should be known. Ten thousands of times of Monte Carlo simulation were run to acquire the input offset voltage of

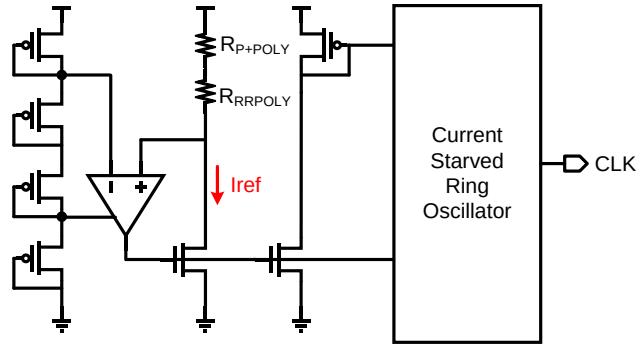

Fig. 7. Temperature-insensitive clock generator [6].

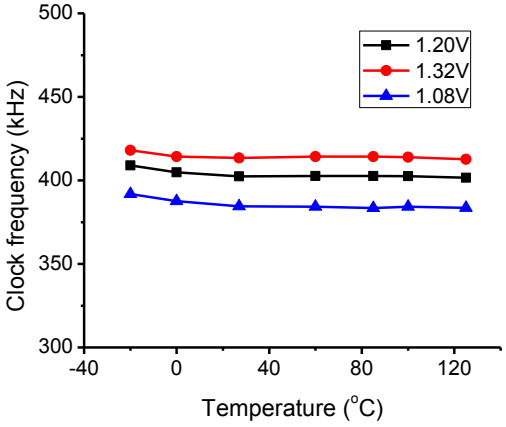

Fig. 8. Clock frequency variation over temperature.

the designed amplifier. As shown in Fig. 5, the mean is 10.54 μV, and the standard deviation is 1.65 mV.

D. *AC and Transient Simulation*

Fig. 6(a) shows ac simulation results of two cases: (1) the conventional amplifier, which is without lowpass gain suppression and a capacitor coupled to the differential pair, and (2) the amplifier including them. The gain of the conventional amplifier is largely affected by changing the input offset voltage. However, the gain of the amplifier with a low pass filter and a capacitor is independent of changing the input offset voltage.

The transient simulation results are shown in Fig. 6(b). The output signal of the conventional amplifier is saturated as the input offset voltage increases, while the output signal of the designed amplifier is rarely affected by the change of the input offset voltage up to 6σ so that we can guarantee the proper operation under process variation and device mismatch.

IV. Chopper Clock Generator

In order to provide constant chopping frequency over temperature, a temperature-insensitive clock generator is designed as shown in Fig. 7. An amplifier forces constant voltage over R_{P+POLY} and R_{RRPOLY} by a feedback loop [6]. If the power supply voltage is not changed, constant current flows through them by

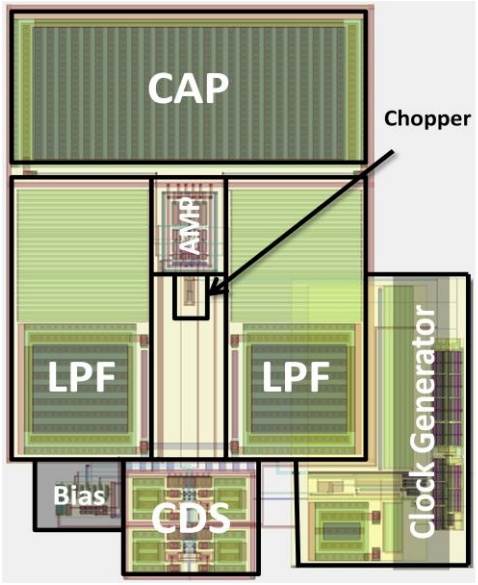

Fig. 9. Chip layout.

$$I_{ref} = \frac{V_{DD}}{4 \times R_{SUM}} \quad (4)$$

where R_{SUM} is the sum of R_{P_POLY} and R_{RRPOLY}. Temperature coefficient of a resistor still causes current to be changed over temperature. Two different types of resistors are combined together to cancel their temerature coefficient out. Compared to R_{P+POLY}, R_{RRPOLY} has the opposite sign and 15 times larger temerature coefficient. Clock frequency is set by R_{P+POLY} while R_{RRPOLY} is used to reduce its temperature variation.

The constant current through these resistors is fed to a current starved oscillator by current mirrors. The oscillator has 5-stage inverter chain, and it is followed by a non-overlaping clock generator. As shown in Fig. 8, clock frequency changes by 7.4Hz from -20 °C to 125 °C, which is 51 mHz/°C temperature dependency.

When the power supply voltage is changed, the period of clock is changed by

$$\Delta T_P = \frac{N C_O \Delta V_{DD}}{\Delta I_{ref}} \quad (5)$$

where N is the number of stages, and C_O is the total capacitance at the output of each inverter stage. Since the variation of I_{ref} is proportional to the power supply voltage, the period remains the same. However, the gain of the amplifier and the accuracy of current mirrors have dependency on the power supply voltage. Thus, clock frequency shows 120 Hz/V variation with ±10 % power supply voltage change.

For the process variation, this circuit is required to be calibrated once using an off-chip resistor by adding or subtracting current in the feedback path.

V. Simulation Results

This chip is designed in a 0.13 µm IBM CMOS process. The total area is 0.06 mm^2. The die photo is shown in Fig. 9. In this chip, the bandpass amplifier takes most area since it has large capacitor and lowpass filters.

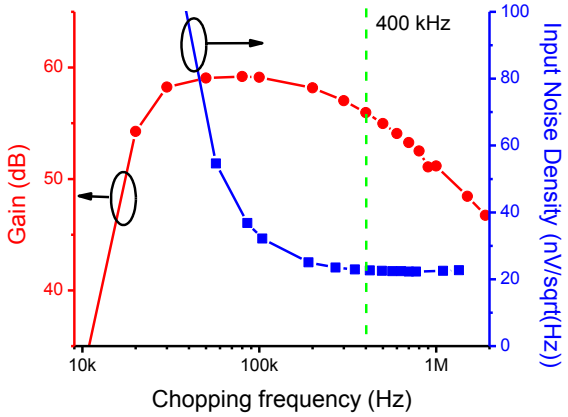

Fig. 10. Simulated gain and input-referred noise density with different chopping frequency.

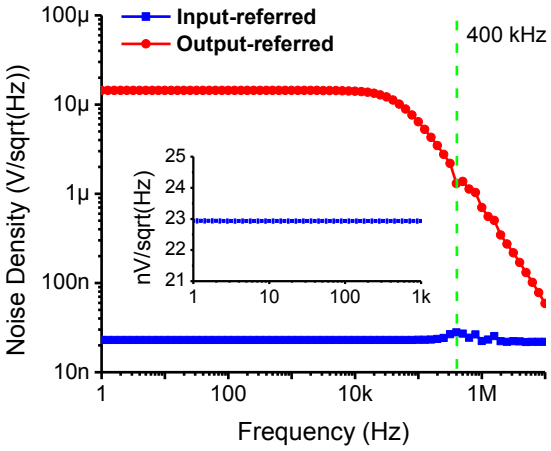

Fig. 11. Simulated input and output-referred noise density with 400 kHz chopping frequency.

Fig. 10 shows gain and input-referred noise density with different chopping frequency. There is a trade-off between those factors. Higher frequency modultes input signals farther from 1/f noise, so it gives better noise performance. On the other hand, the gain of the chopper amplifier is higher in lower frequency since the amplifier itself loses its gain after the first pole. Bandpass characteristic of the amplifier makes the gain decrease below 50 kHz chopping frequency. Gain is the important factor in terms of noise. According to the Friis' formula, noise from the following stages is divided by the gain of previous stages. Here, we only gave up gain by 3 dB from the maximum value of 59 dB and chose 400 kHz as the chopping frequency. In this point, input-referred noise density is almost the same as the minimum value of 22.3 nV/√Hz. Therefore, 56 dB gain and 22.9 nV/√Hz are achieved with 400 kHz chopping frequency.

Fig. 11 is the PNOISE simulation result with 400 kHz chopping frequency. The input-referred noise density shows

TABLE I. COMPARISON OF PERFORMANCE

	This Work	JSSC '10 [1]	ISSCC '11 [7]	ISSCC '10 [8]	JSSC '10 [9]
Process [µm]	0.13	0.18	0.35	0.70	0.35
V_{DD} [V]	1.2	1.8	5.0	5.0	1.8
Input Noise [nV/√Hz]	23	37	6	11	95
I_{DD} [µA]	13.5 (*26.9)	14.4	1500	143	13
****FOM**	7.1 (*14.1)	19.7	51.2	15.8	117
[kHz]	400	500	200	30	50
DC Gain [dB]	56	168	150	100	130
Area [mm^2]	0.06	1.14	1.26	1.8	0.64

* Current consumption is doubled for only the first stage design.

** FOM = $(V_{NI}^2/\Delta f)* I_{DD}$.

22.9 nV/√Hz in low frequency range. In the output-referred noise density, there is no spike at the chopping frequency which represents no up-converted 1/*f* noise at the output. This is done by replacing the second chopper in the conventional chopper amplifier to CDS block.

Table 1 lists the recent previous works on chopper amplifiers and compares the key circuit parameters to this work. Most chopper amplifier has more than one stage to boost their DC gain higher than 120 dB. In this paper, one stage amplifier is designed with lower gain. To evenly compare with other references, current consumption is doubled when the figure of merit (FOM) is calculated. The FOM is widely used in the recent papers [9],[10], in which the input-referred noise density and current consumption is considered together. By this way, FOM shows this work is better than other references. There could be large noise from the following stages to increase total gain. However, the noise of the first amplifier that we designed will dominate other factors by the Friis' equation. Therefore, we believe the performace of this work will not be degraded much but stay near to that of state-of-the-art works.

VI. CONCLUSION

The paper designed a low power spur-free precision amplifier using two offset cancellation technique, chopper stabilization and CDS. CDS cancels its offset and low frequency noise by $1-z^{-1}$ while the combination method processes input signals by $1+z^{-1}$. The amplifier has low DC gain to prevent output saturation, but has high gain at the chopping frequency for input signals. A temperature-insensitive clock generator is included to reduce variation of the chopping frequency over temperature. The proposed circuit, designed in 0.13 µm CMOS process, consumes 13.5 µA with 1.2 V supply voltage and achieves the input-referred noise density of 22.9 nV/√ Hz.

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