RF transmitter with Cartesian feedback

Alexandra Holbel, Fu-Pang Hsu, and Chunyang Zhai, *University of Michigan*

Abstract—**This paper presents a 2.4 GHz transmitter with Cartesian Feedback for use in Bluetooth applications. The Cartesian feedback is used to improve the linearity of the system, allowing the power amplifier to be designed for efficiency. The Cartesian feedback loop consists of two independent I and Q feedback loops that are coupled only through their phase offset which can be compensated. The upconversion and downconversion mixers use a doubly balanced Gilbert cell topology with strong linearity requirements for the down-converting mixers. The transmitter is realized by the 0.13um IBM CMOS process.**

Index Terms— **Cartesian feedback, Class A power amplifier, RF transmitter**

I. INTRODUCTION

TRANSMITTERS are ubiquitous as our lives become increasingly data oriented. Devices are constantly in communication with other technology and the ability to transfer wirelessly is important. This paper presents a RF transmitter for the 2.4 GHz band to be applied to Bluetooth technology. As power increases, distortion out of the power amplifier increases, so we discuss Cartesian feedback as an effective method for linearizing the transmitter.

Cartesian feedback was chosen as the method of feedback because of its simplicity and robustness to a poor power amplifier model. It is not necessary to characterize the power amplifier completely for a Cartesian feedback system. Other possible feedback methodologies include predistortion, power backoff, and envelope elimination and restoration [1]. The idea behind predistortion is to code in predistorted signals that are chosen based on the input signal. The disadvantage to this method is that it increases complexity and requires a very good power amplifier model, which is difficult to derive.

Power backoff is a simple approach, but reduces power efficiency. Finally, envelope elimination and restoration involves envelope matching in the power amplifier. In this case, the phase matching is critical. Additionally, this is a difficult method to implement with power efficiency. Therefore, Cartesian feedback provides an excellent option for implementing the feedback system.

II. THEORY OF OPERATION

On a basic level, a transmitter consists of an upconversion mixer and a power amplifier attached to an antenna. To linearize the power amplifier, feedback can be wrapped around it. However, at the high frequency output of the power amplifier, it is difficult to stabilize a feedback loop.

Therefore, we can take advantage of the baseband characteristic of the inputs and downconvert the output back to the baseband frequency for the feedback. Figure 1 shows the block diagram of the system.

A Cartesian feedback system is chosen as opposed to a polar feedback system to take advantage of the decoupling of amplitude and phase. In a polar feedback loop, the phase and amplitude are closely linked which makes the design complicated. For a Cartesian feedback system, the quadrature nature of the systems is taken advantage of and the phase and amplitude are decoupled. [1] Instead, two independent but identical I and Q loops are designed. In reality, the I and Q loops are not entirely decoupled. Phase misalignment will still couple the signal between the two channels if not properly corrected. The phase alignment system is outside the scope of this paper. There are many papers discussing the implementation of phase alignment systems so for the purpose of this paper it is assumed that it can be implemented and the phase misalignment is measured and compensated for manually.
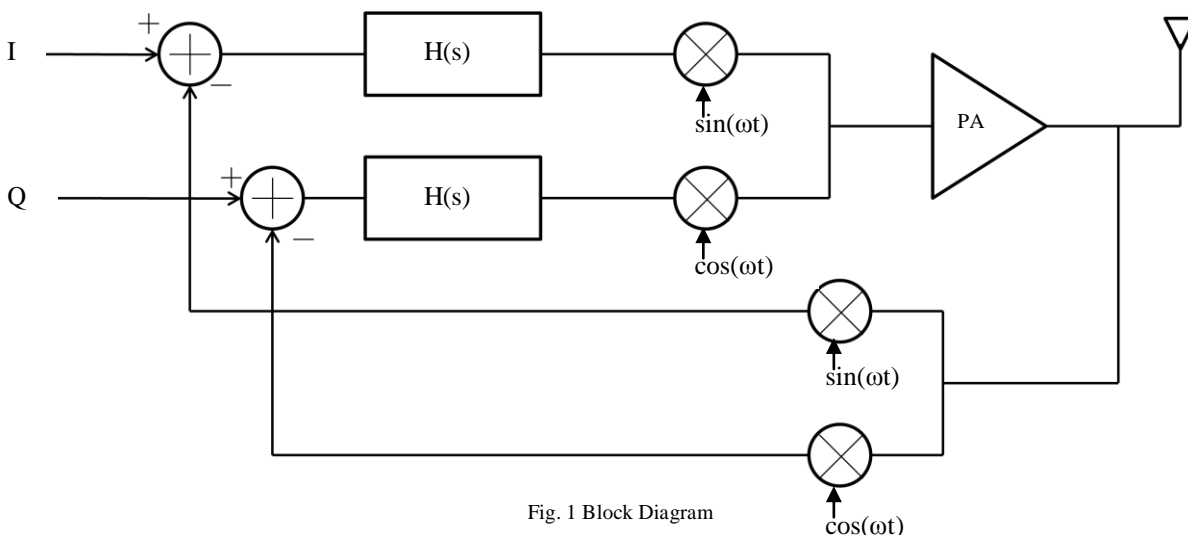

Fig. 1 Block Diagram

III. DESIGN IMPLEMENTATION

A. Mixers

The mixer is an essential component in an RF system and a key building block for modern wireless communication integrated circuits. In the transmitter, the mixer is used to upconvert the baseband signal to RF for transmission and another mixer is used to downconvert the RF signal for baseband feedback. The same mixer is used for both cases and the linearity requirement for the downconversion mixer drives the design [2].

The RF mixer is a three port, nonlinear device. Through the nonlinearity of the MOSFET, two input signals with different frequencies can be multiplied to generate a sum and difference term in frequency. While a passive mixer has better linearity and no power consumption, it suffers from conversion loss and high noise figure. While the linearity is important, that could be compensated for by attenuating the output of the power amplifier to a level that is within the linearity of the downconversion mixer. Therefore, a doubly balanced Gilbert cell topology (Figure 2) was chosen. The doubly balanced topology was chosen for its port to port isolation, higher linearity, and improved suppression of even order spurious products [3].
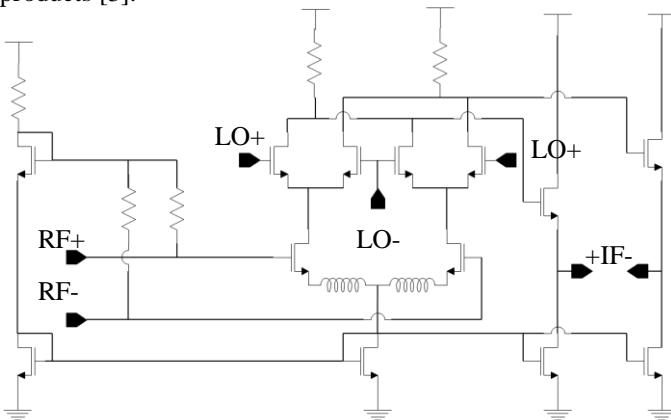

Fig. 2 Mixer Schematic

The switching quad stage is driven by differential LO signals and a transconductance stage that amplify the differential RF signals by g_m. A biasing stage provides the bias points for the transistors. A buffering stage on the output consists of a differential source follower which can transform a high output impedance to a lower impedance in order to provide enough current for driving the next stage [4]. The source degeneration inductors of the mixing stage enhance the 1dB compression point but decrease the conversion gain.

In the steady state, the switching quad stage transistors are operating in subthreshold region in order to minimize the power consumption and only conduct when LO power is provided [5]. They were sized smaller to minimize the parasitic capacitance that decreases conversion gain and increases noise. However, there is also the tradeoff that sizing them too small makes it too difficult to drive the transistor. Therefore, the sizing was optimized for those constraints. The transconductance stage transistors are biased in saturation in order to provide high g_m and sized accordingly.

As expected from mixer design, the output consists of a sum and a difference term in frequency:

$$v_{out} = \frac{2AV_R}{\pi}\left[\sin\left((\omega_{RF} + \omega_{LO})t\right) - \sin\left((\omega_{RF} - \omega_{LO})t\right)\right].$$

Either a lowpass filter or bandpass filter can be used on the output of the downconversion mixer to acquire the desired signal of the two. On the upconversion signal, the power amplifier passes only the RF signal and no filtering is required. The RF signal is at 2.4GHz, the LO frequency is at 2.41GHz and the baseband IF frequency is at 10MHz.

B. Power Amplifier

The power amplifier is the other main building block of a RF transmitter. The power amplifier consumes a large share of the power budget in most transmitters but the linearity of the power amplifier also determines the output capacity. A linear power amplifier provides a clean output spectrum which represents the ability to transmit data at the highest possible rate for a given channel bandwidth [6]. In this work, the power amplifier operates as close to saturation as possible to maximize the power efficiency while trading off linearity. A linearization technique is presented in the next section to achieve a moderately linear power amplifier in this near-saturated region.

A two stage Class A power amplifier with pseudo-differential architecture is chosen (Figure 3). The pseudo-differential architecture helps minimize the coupling of RF energy into sensitive nodes and the power and ground lines which helps alleviate concerns of crosstalk and coupling when the power amplifier is on the same die as the linearization system [1].
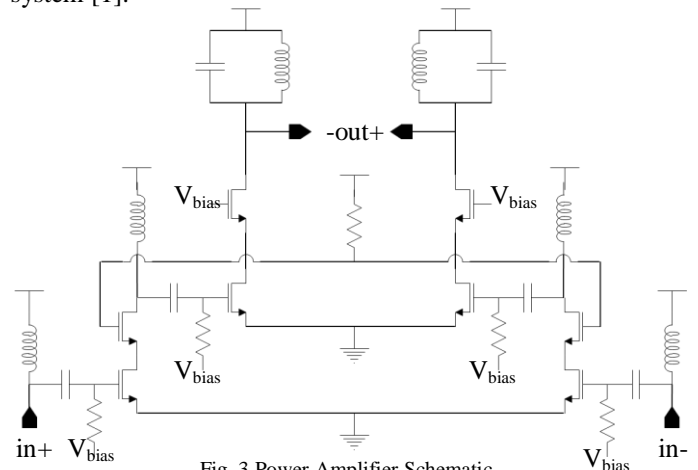

Fig. 3 Power Amplifier Schematic

An inductor is used at the output instead of a resistor to improve the output peak amplitude and increase the power efficiency. Cascode transistors stabilize the amplifier as well as add gain to the output. One tradeoff in this design is headroom. Because the headroom is limited, tail current sources are eliminated in this architecture and therefore the power amplifier lacks common mode rejection. As stated in [1], it is important to decouple the ground terminals of the first and second stage of the power amplifier on the die to reduce the possibility of common mode oscillation.

C. Loop Filter

The loop filter is designed with slow rolloff compensation [7]. The slow rolloff compensation technique approximates the transfer function:

$$H(s) = \frac{K}{\sqrt{s}}$$

which is chosen for its ability to stabilize the system. This transfer function gives a 10dB/decade rolloff and 45 degrees of phase which will be added to the dominate pole of the power amplifier that follows and still have a healthy phase margin. This transfer function is realized by placing alternating poles and zeros. Schematically, this consists of a ladder network of increasing R and C blocks (Figure 4) in parallel. Each "rung" of the ladder multiplies the previous R and C value by a chosen alpha. A bode plot of the system (Figure 5) shows the added poles and zeros which give an approximate 10dB/decade rolloff and the phase boost which brings the phase up to 45 degrees.
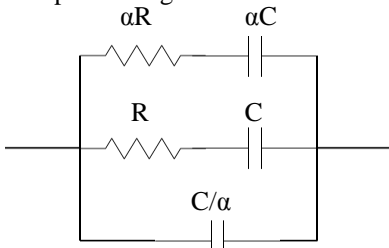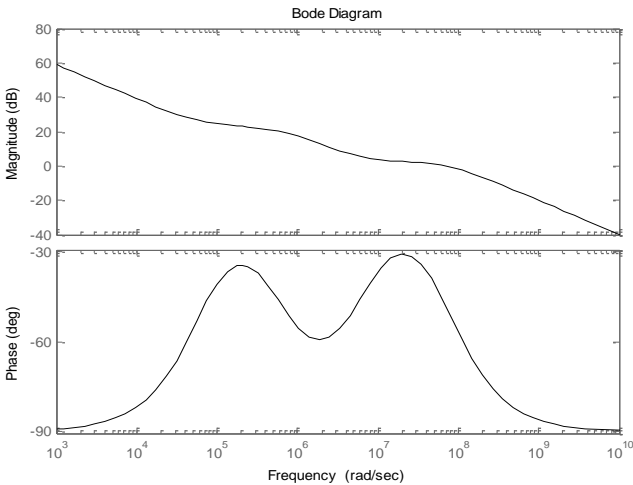

Fig. 4 Ladder Network

Fig. 5 H(s) Bode Plot

IV. SIMULATION RESULTS

Each block was tested independently and then the entire system was simulated both open and closed loop to determine the performance.

A. Mixer Results

The mixer was simulated to test linearity and proper mixing. The isolation was excellent but the power was fairly high, likely due to the buffer output stage. A plot of the 1dB

Compression Point and IIP3 are shown in Figure 6. Table 1 lists complete simulation results.
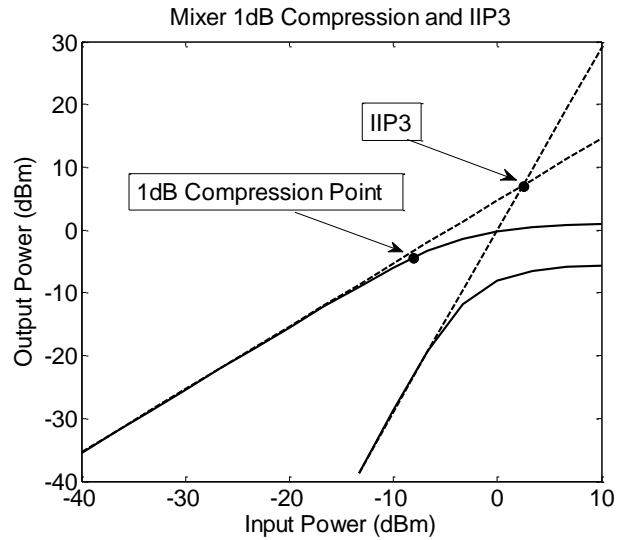

Fig. 6 Mixer P1dB and IIP3 Plot

TABLE 1
MIXER SUMMARY

Specification	Results
1dB Compression (input referred)	-8.02 dBm
IIP3	1.57 dBm
RF to IF Isolation	77.63 dB
LO to IF Isolation	47.50 dB
LO to RF Isolation	95.88 dB
Conversion Gain	4.65 dB
Noise Figure	21.73 dB
Power Consumption	3.64 mW

B. Power Amplifier Results

The power amplifier was simulated to test efficiency and distortion. A power added efficiency (PAE) of 48% was achieved and considered acceptable for a Class A design. A plot of the 1dB Compression Point is show in Figure 7. Table 2 lists complete simulation results.

C. System Results

After simulating the individual blocks, the entire system was simulated both open loop and closed loop to compare results. The I and Q input signals were identical sine waves offset by
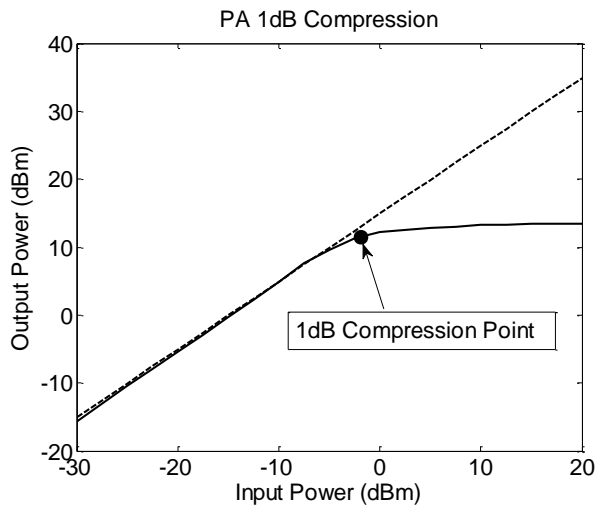
Fig. 7 Power Amplifier P1dB Plot

TABLE 2
POWER AMPLIFIER SUMMARY

Specification	Results
Power Added Efficiency (PAE)	48%
1 dB Compression (input referred)	-1.89 dBm
Max Output Power	12 dBm

90degrees. This gives an ideal output that sweeps a constant amplitude circle in the Cartesian coordinate system (Figure 9a) with an output that has constant amplitude at 2.4GHz (Figure 9b). When simulating open loop, the results indicated amplitude distortion as indicated by the wave on top of the

2.4GHz signal (Figure 9d). This suggests that instead of sweeping an ideal circle in the IQ plane, we are instead sweeping an elliptical shape where the amplitude changes in time (Figure 9c). The loop was then closed and resimulated. The output in Figure 9f demonstrates that closing the loop decreased the amplitude distortion on top of the 2.4GHz signal. Some amplitude distortion still existed, but the output much more closely approximates the ideal circle sweep and only slightly resembles and ellipse (Figure 9e).

Another indication of this distortion reduction is visible in the input signal to the power amplifier. Figure 8a shows the input in an open loop. The signal is already slightly distorted as it has passed through the upconversion mixer. In Figure 8b, we see the input in the closed loop. In this case, the input is further distorted to something closer to a triangle wave, but it gives a much cleaner sine wave output. This is a predistortion to compensate for the distortion in the power amplifier.

The 1dB Compression Point and max output power were also simulated. The results are seen in Figure 10 and Table 3 respectively. As expected, the gain from the closed loop system was decreased, but the 1dB Compression Point was pushed out further. Likewise, the max output power is slightly less, but this was expected.
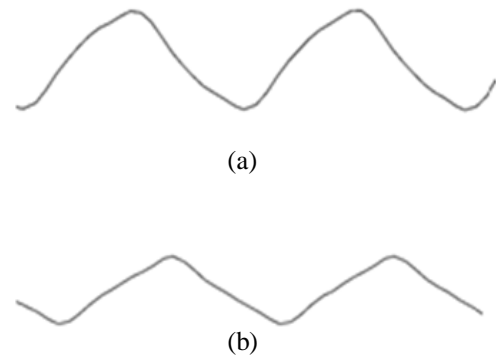

(a)

(b)

Fig. 9 System Input

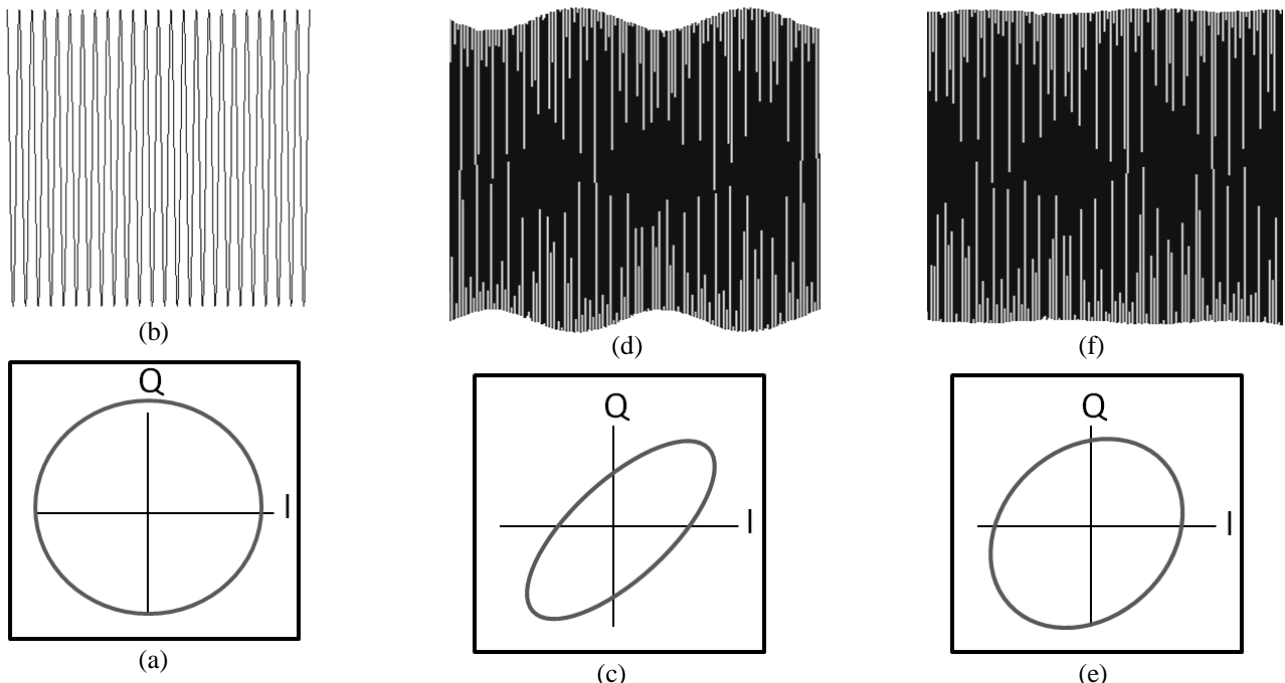(b)

(d)

(f)

(a)

(c)

(e)

Fig. 8 System Output

A comparison to existing literature is also seen in Table 3. Our system is comparable in output power achieved and linearity.

Noise and PAE were not measured for the system since H(s) was implemented with ideal components and would therefore not give accurate results for a real system.

D. Layout

The layout is shown in Figure 11. It is DRC and LVS clean. The layout was designed to be symmetric with the power amplifier in the middle and the mixers on either side. The area of the layout is 1.15mm^2.
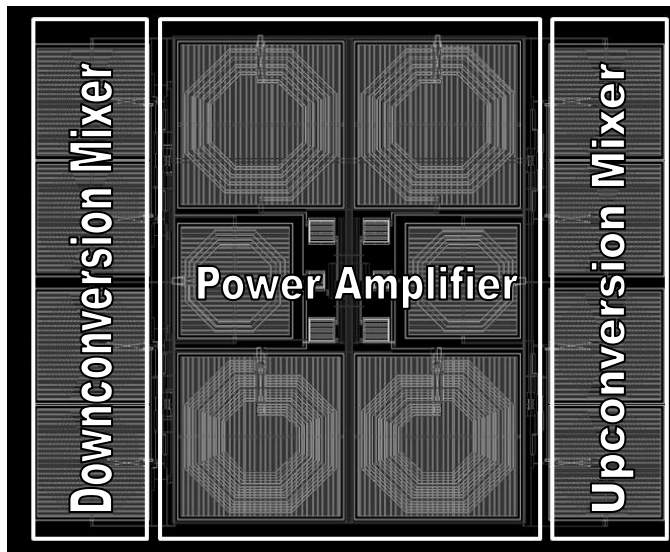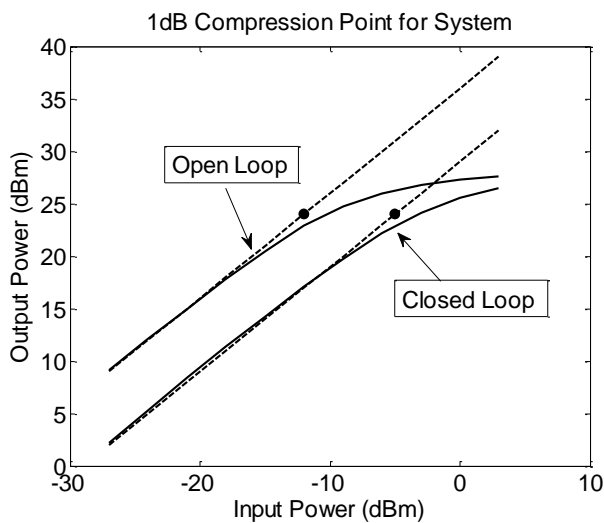

Fig. 11 Layout

Fig. 10 System P1dB Plot

V. CONCLUSION

This paper effectively demonstrates a RF transmitter at 2.4 GHz with Cartesian feedback to improve linearity. Results indicated a reduction in distortion for the closed loop system compared to the open loop system. Future work would include implementing the loop filter with nonideal components, improving the linearity of the downconversion mixer, and implementing a phase alignment system.

APPENDIX

The schematic, layout, and test bench files are stored in **/afs/umich.edu/class/eecs522/w11/groups/group4**

REFERENCES

[1] J.L. Dawson, *Feedback Linearization of RF Power Amplifiers.* United States: Kluwer Academic, 2004.
[2] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge, U.K.: Cambridge Univ. Press, 1998.
[3] Sulivan, P.J.; Xavier, B.A.; Ku, W.H.; , "Low voltage performance of a microwave CMOS Gilbert cell mixer," *Solid-State Circuits, IEEE Journal of* , vol.32, no.7, pp.1151-1155, Jul 1997
[4] Lin, C.-S.; Wu, P.-S.; Chang, H.-Y.; Wang, H.; , "A 9-50-GHz Gilbert-cell down-conversion mixer in 0.13-μm CMOS technology," *Microwave and Wireless Components Letters, IEEE* , vol.16, no.5, pp. 293- 295, May 2006
[5] Hanil Lee; Mohammadi, S.; , "A 500μW 2.4GHz CMOS Subthreshold Mixer for Ultra Low Power Applications," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE* , vol., no., pp.325-328, 3-5 June 2007
[6] Palaskas, Y.; Taylor, S.S.; et al; "A 5 GHz class-AB power amplifier in 90 nm CMOS with digitally-assisted AM-PM correction," *CICC, 2005.*
[7] J.K. Roberge, *Operational Amplifiers: Theory and Practice.* New York: Wiley, 1975.
[8] D. Chowdhury; et al, "A 2.4GHz mixed signal polar power amplifier with low-power integrated filtering in 65nm CMOS," CICC, 2010.
[9] L. Perraud; et al, "A direct-conversion CMOS transceiver for the 802.11a/b/g WLAN standard utilizing a Cartesian feedback transmitter," *JSSC,* 2004.

TABLE 3
SYSTEM SUMMARY

Specification	[8]	[9]	Open Loop	Closed Loop
1 dB Compression (input referred)	-10 dBm	-31dBm	-12 dBm	-5 dBm
Max Output Power	21.8 dBm	8 dBm	24 dBm	22 dBm
Area	-	-	1.15 mm^2	>1.15 mm^2