Analog Front-End Direct Conversion Receiver for 802.11b WiFi Applications

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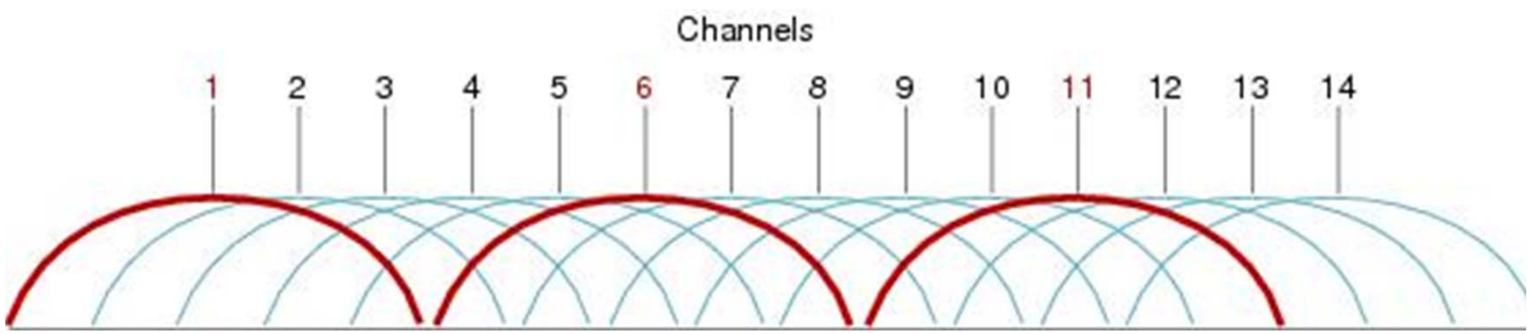
IEEE 802.11b Standard

- Wireless standard for data transmission
  - Supports 1 and 2 Mbits/sec utilizing DBPSK and DQPSK respectively
  - Additional Rates of 5.5 and 11 Mbits/sec are achieved using CCK modulation frequency spreading

IEEE 802.11b Standard

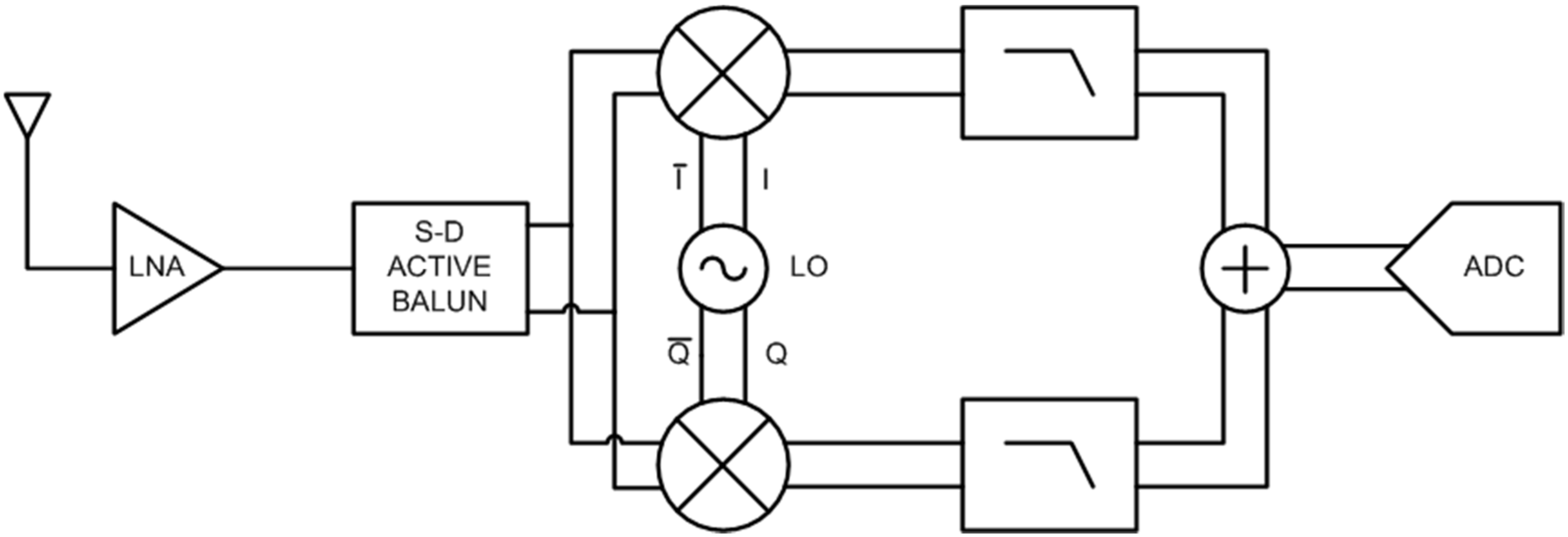
- 802.11b Channels
  - Composed of 14 channels at frequencies 2.412-2.484 GHz spaced 5 MHz apart and 22 MHz wide
  - In North America only first 11 channels are used



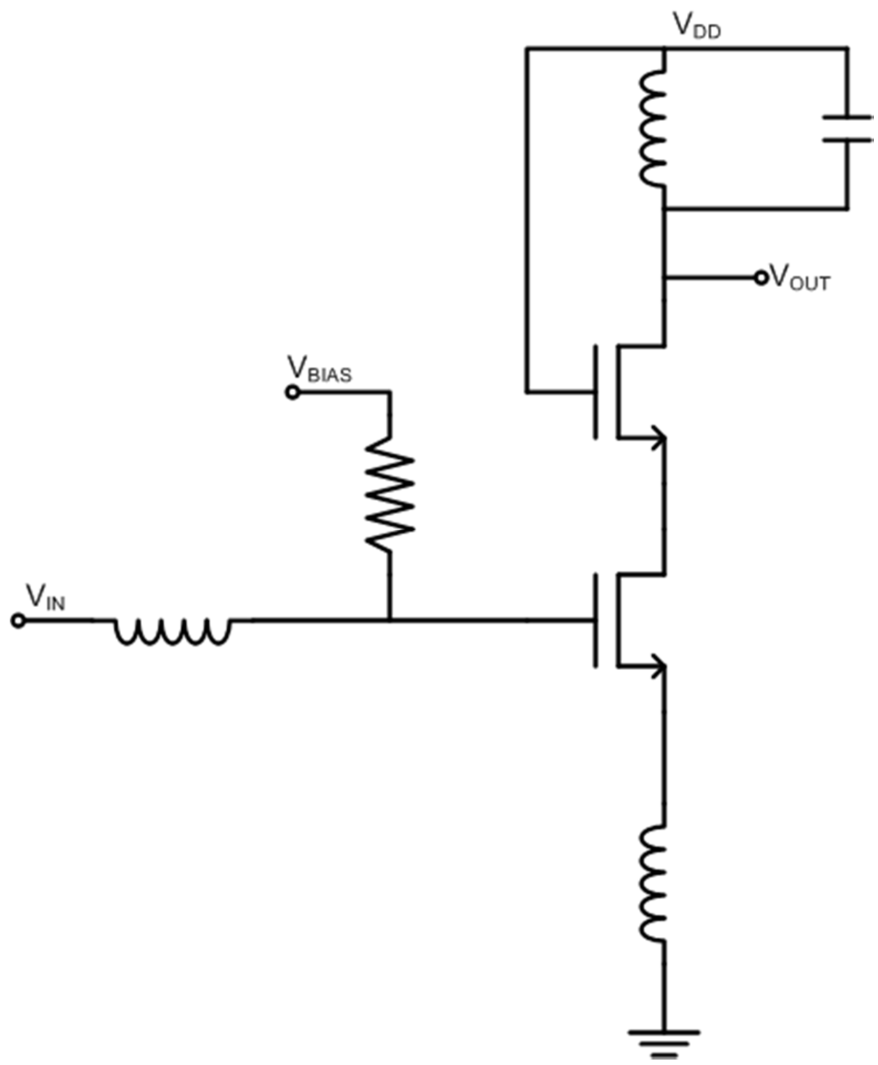
IEEE 802.11b Receiver Specifications

- Input Range -83/-77 dBm to -10 dBm for 5 MHz channel spacing and 11Mb/s
- Adjacent Channel Rejection
  – Adjacent channels defined as ±25 MHz apart
  – Rejection must be 27 dB or greater

Receiver Architecture



LNA Design

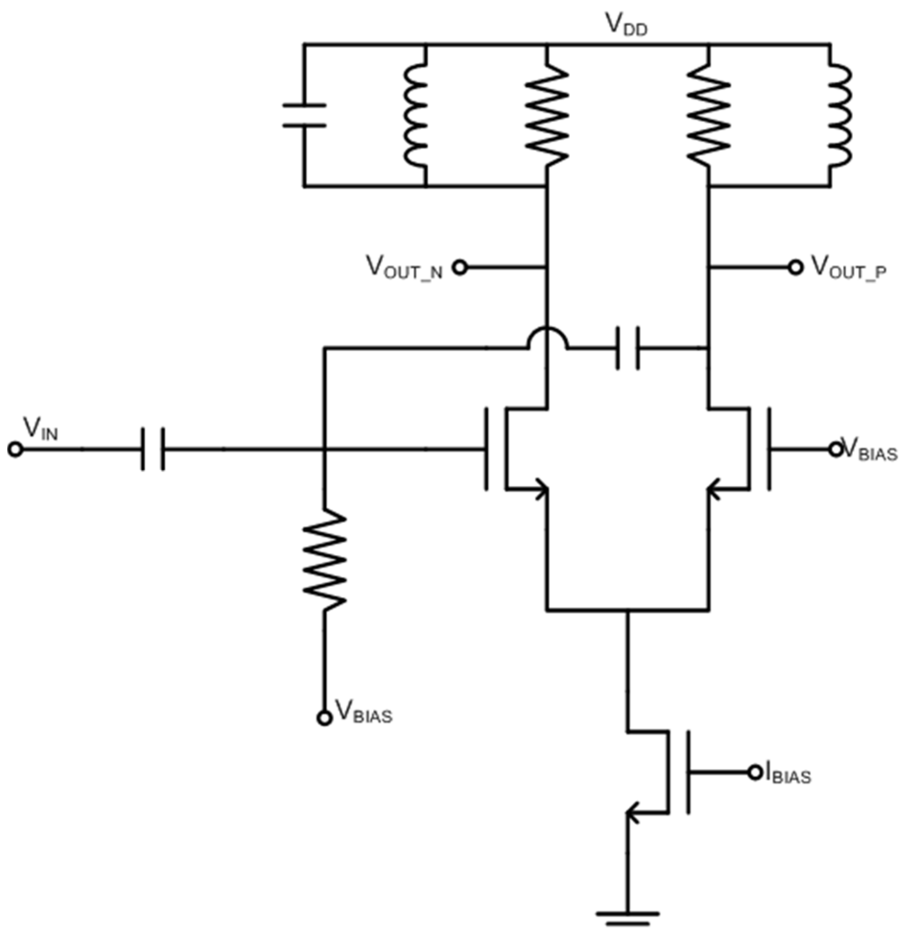


LNA Specifications

NF	2.3-2.4 dB
S11	< -10 dB
S21	21-22 dB
Gain	21-22 dB
P1dB	-26 dBm

Ranges Quoted for 2.4-2.5 GHz

Active Balun Design

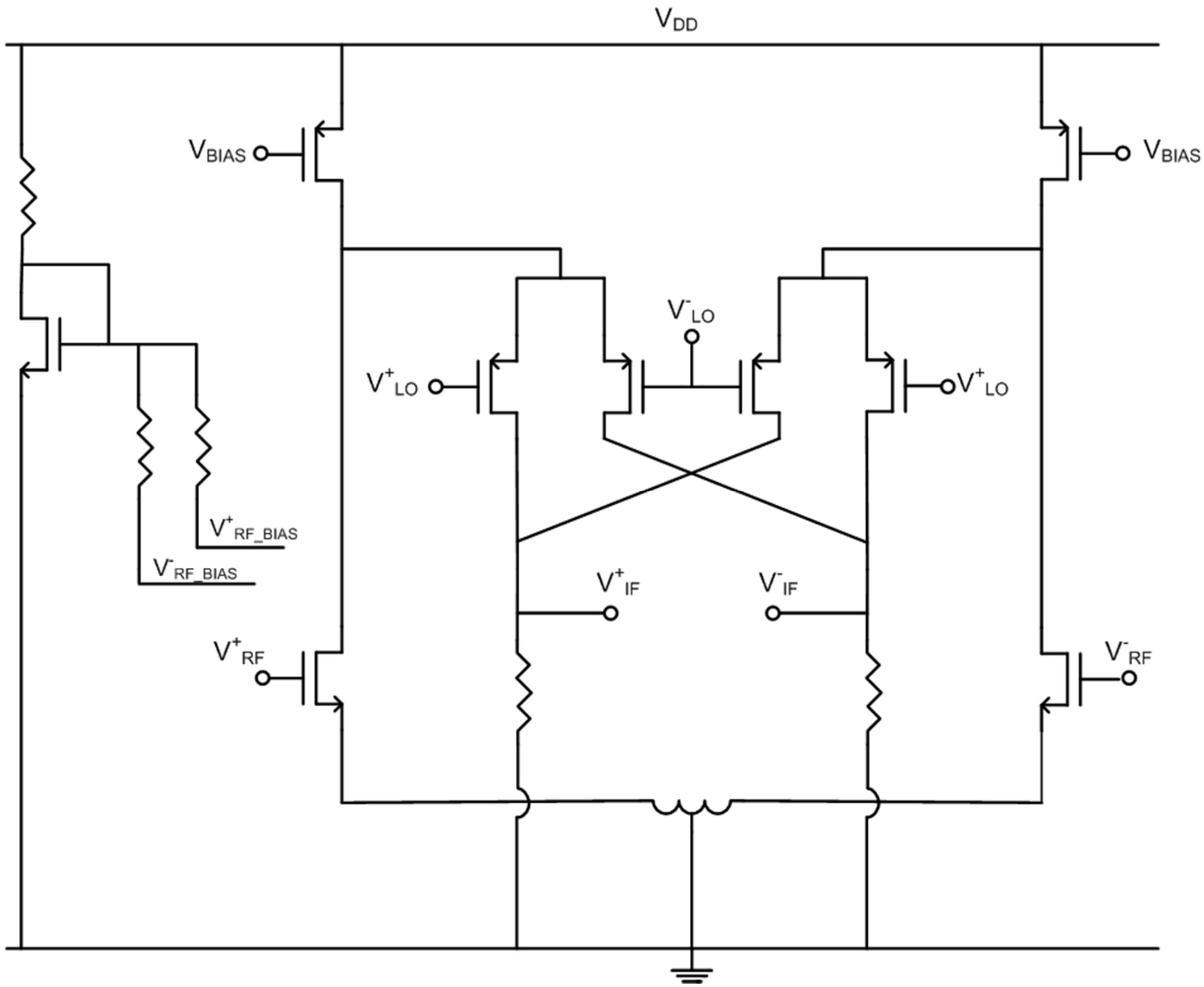


Balun Specifications

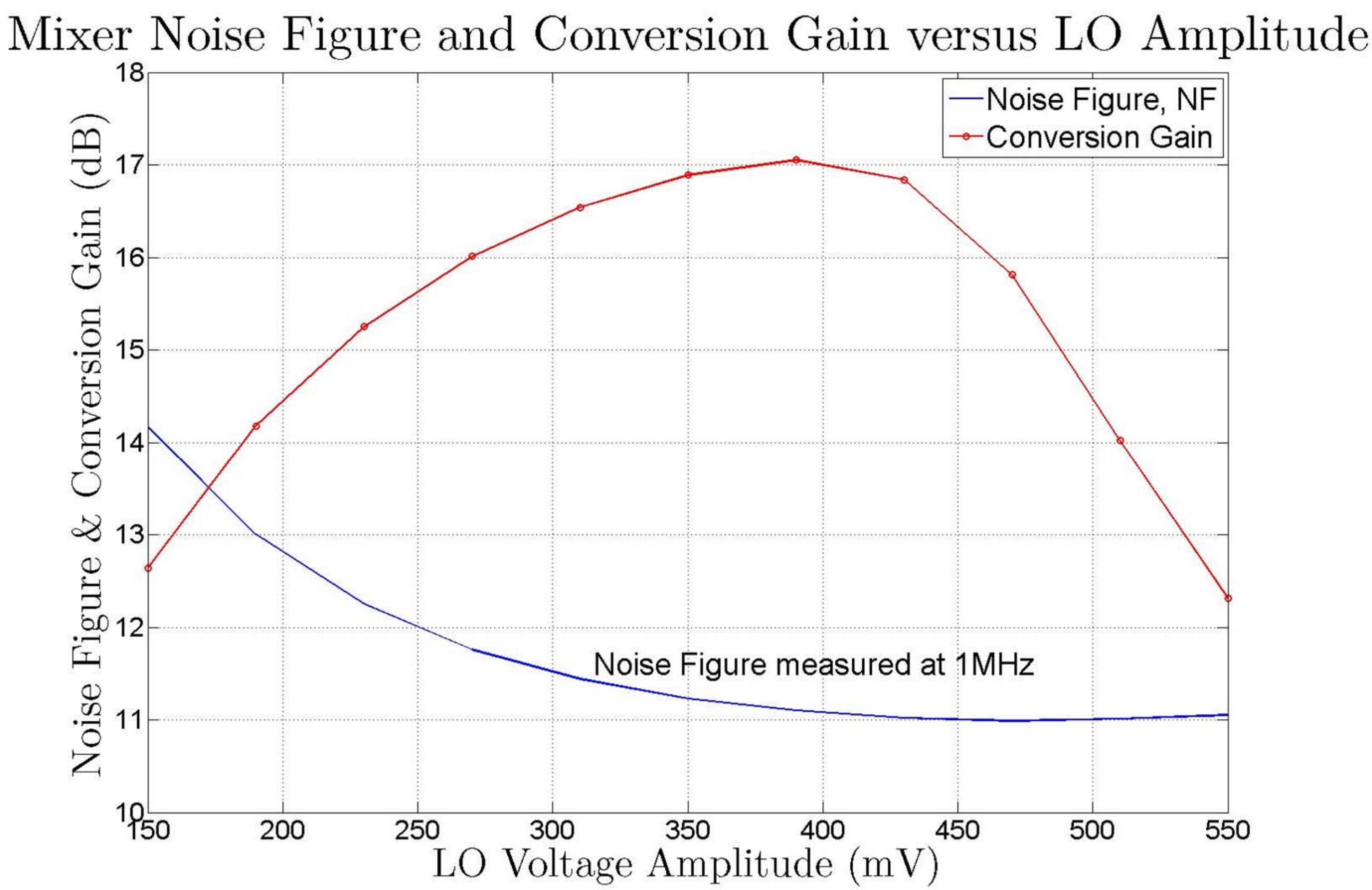
NF	7.4 dB
Max Phase Difference	4 degrees
Max Amplitude Difference	4%
Gain	12 dB

Ranges quoted for 2.4-2.5GHz and -10 dBm input

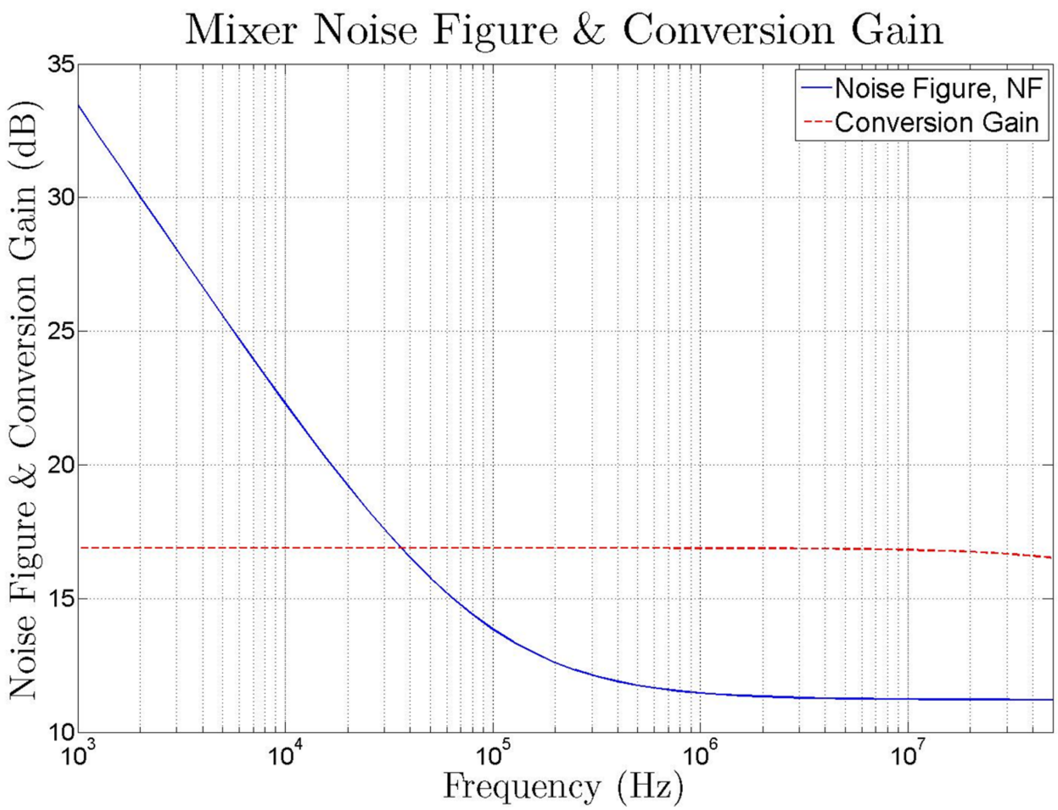
Mixer Design



Mixer Specifications



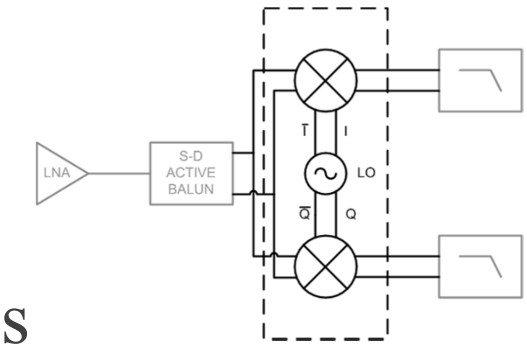
Mixer Specifications



Mixer Specifications

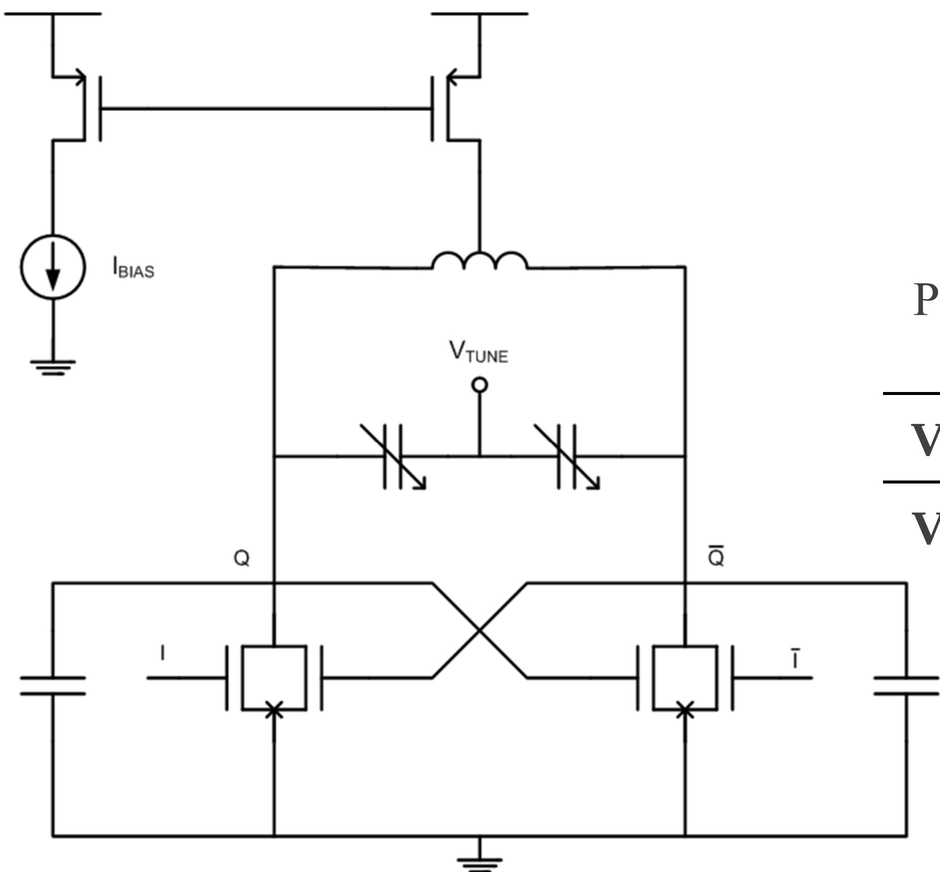
NF(dsb)	11.25 dB
Conversion Gain	16.9 dB
IIP3	-4.83 dBm
P1dB	-13.5 dBm
LO->RF Isolation	-97 dB
LO->IF Isolation	-80 dB

Local Oscillators for 802.11b



- DQPSK received signal
  - Requires both in-phase and quadrature (I/Q) LO signals
- LO must lock to 11 different frequencies
  - 1 center frequency per channel
- LO cannot drift much due to 5MHz channel separation
  - ➢ LO should be a Phase-Locked Loop (PLL)

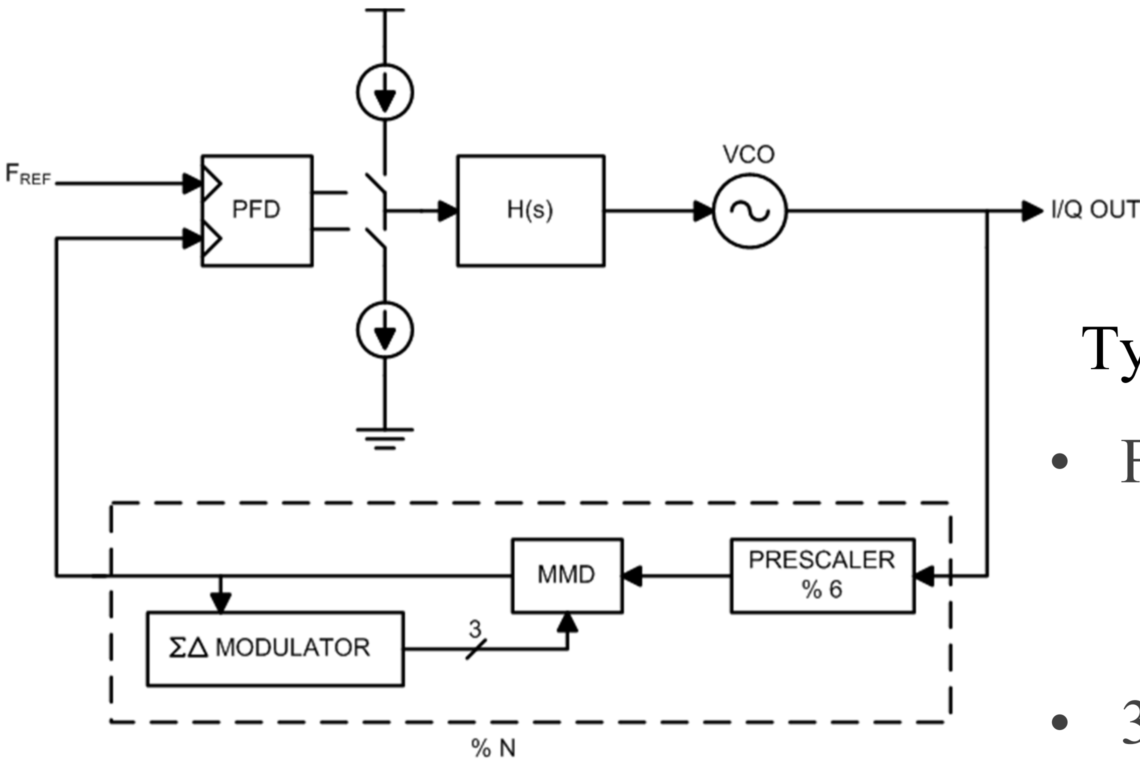
Quadrature Voltage-Controlled Oscillator (QVCO)



VCO Specifications

Phase Noise @ Δf = 1MHz	-118 $^{dBc}/_{Hz}$
VCO Gain, K_v	**220 $^{MV}/_{Hz}$**
Voltage Range	**550mV – 1.2V**

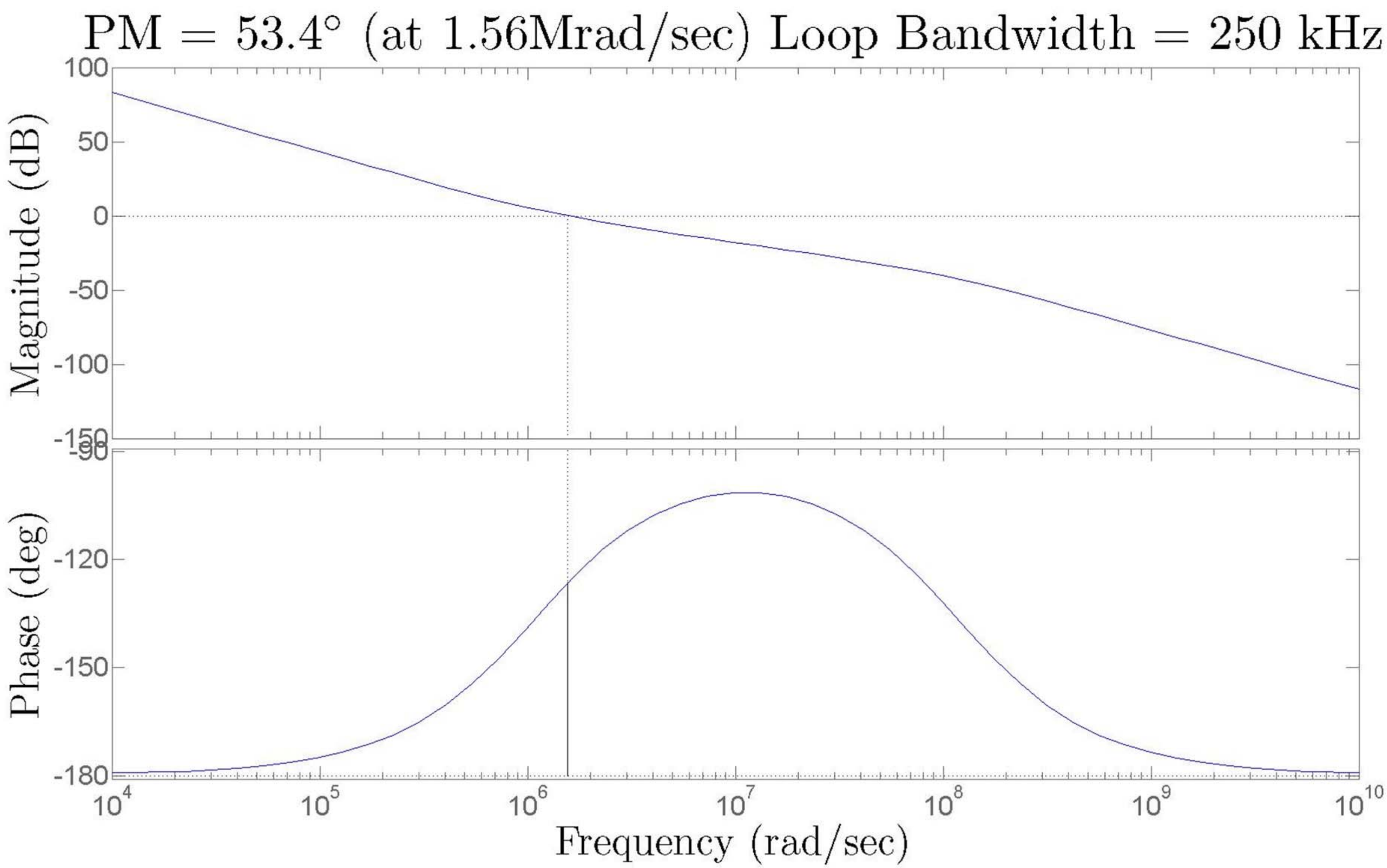
Phase-Locked Loop (PLL)



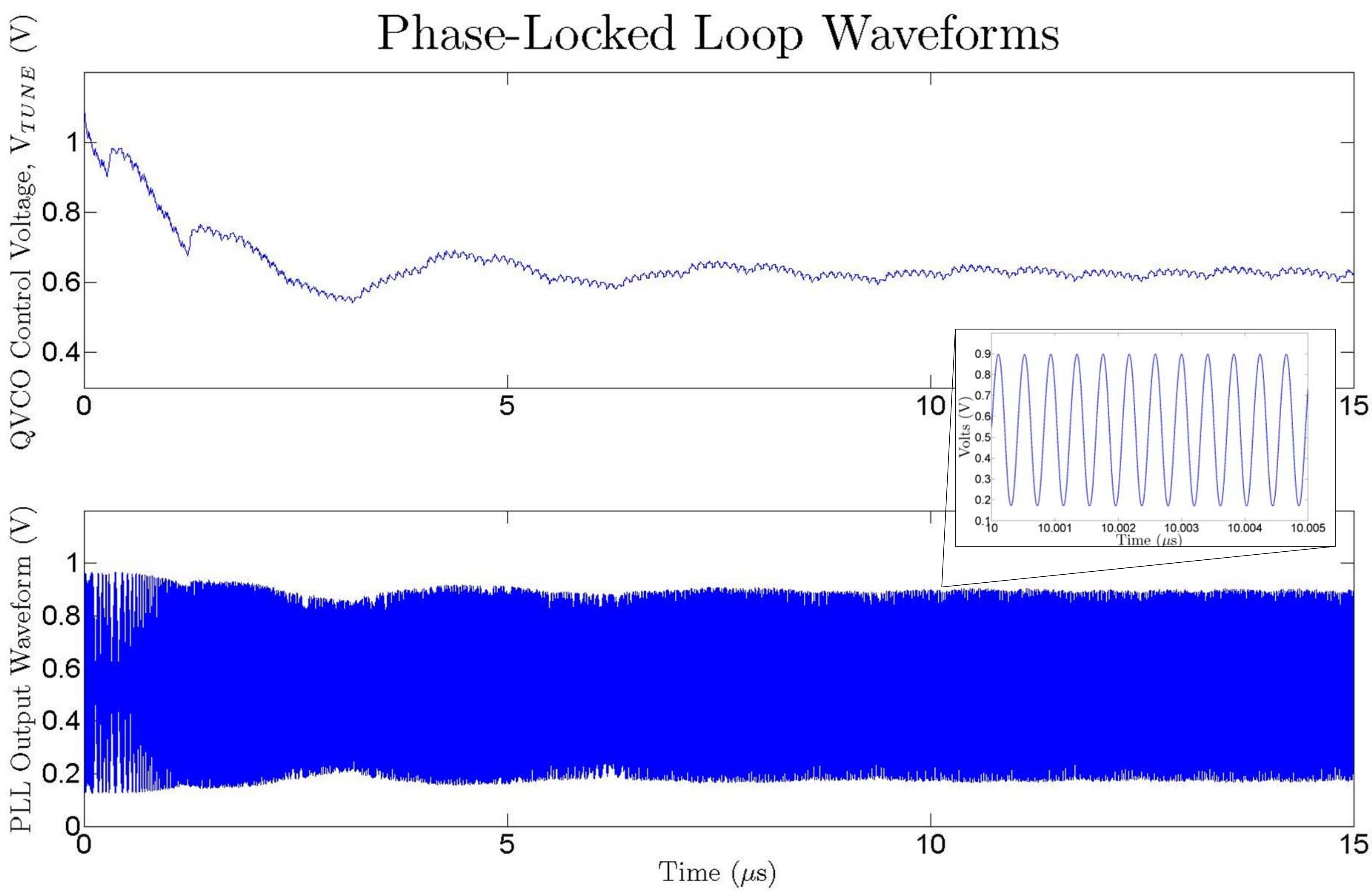
Type 2, 2nd order PLL

- Fractional-N Divider
  - Minimizes Noise
  - Allow higher F_{REF}
- 3rd order ΣΔ Modulator
  - Prevents spurs

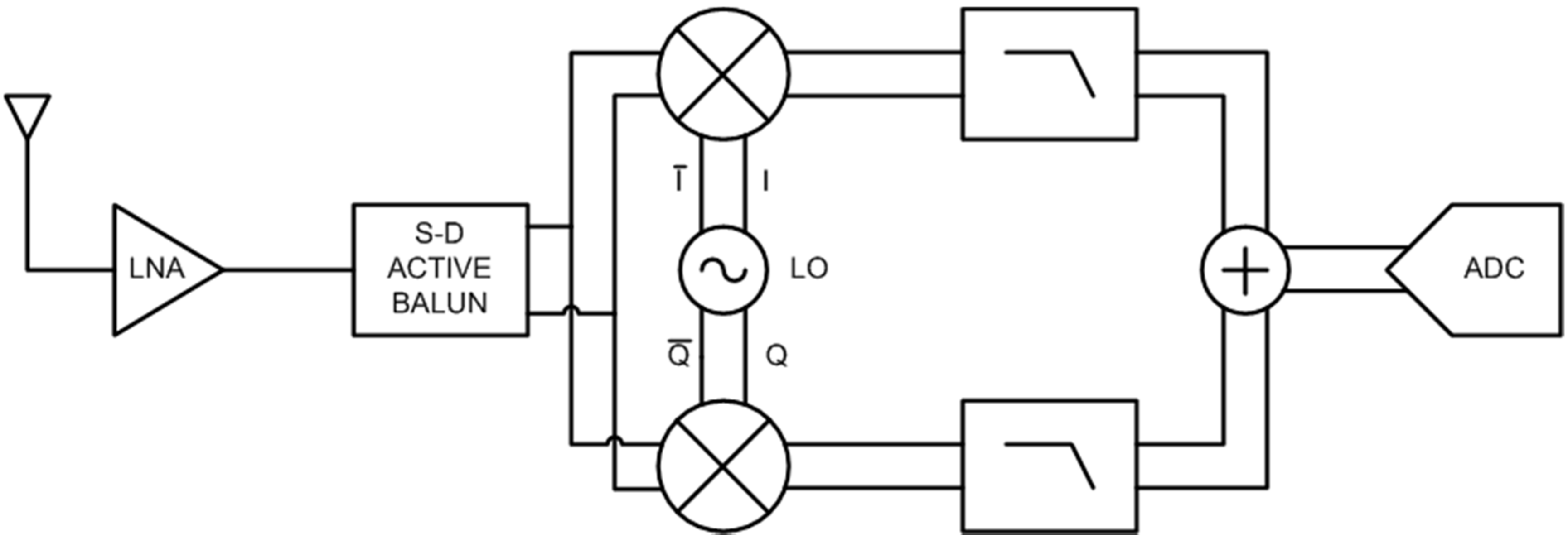
PLL Loop Transfer Function



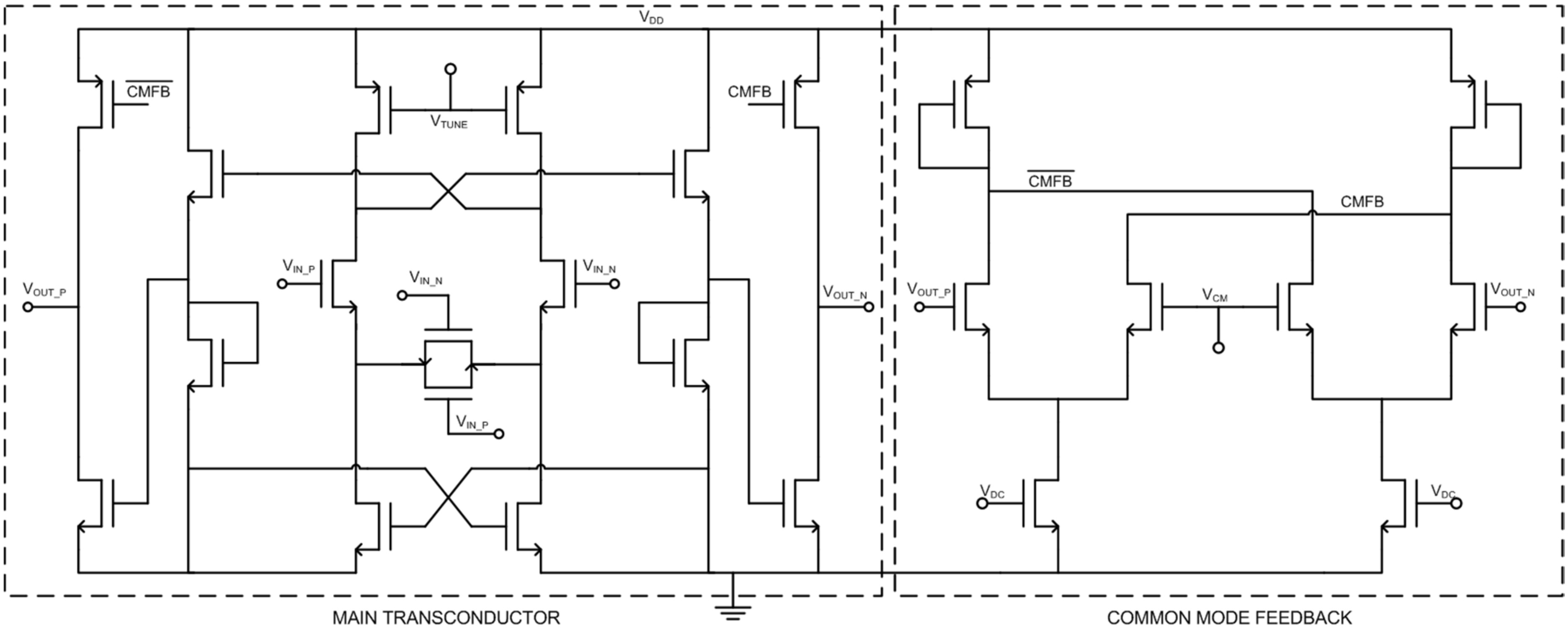
PLL Simulation Results



Our Receiver

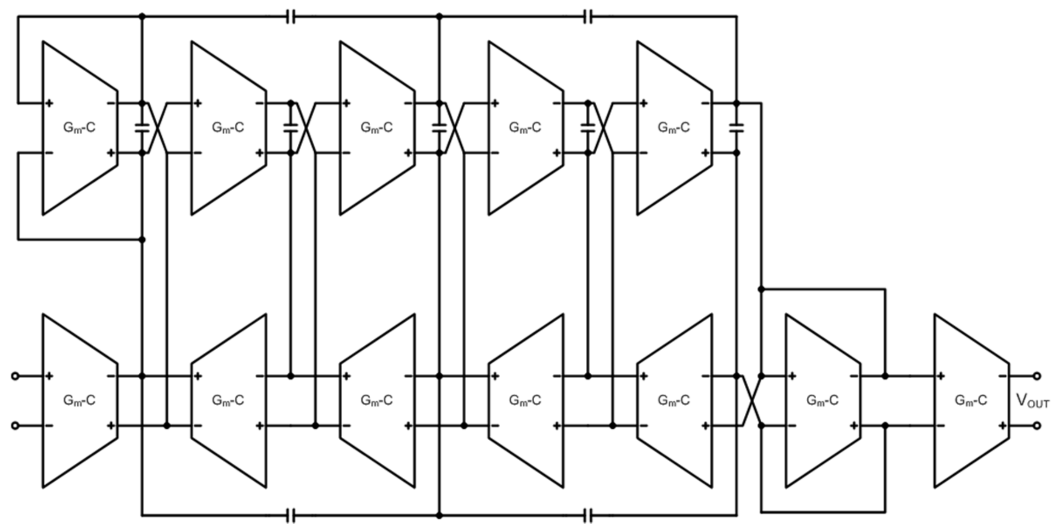


G_m-C Transconductance Cell

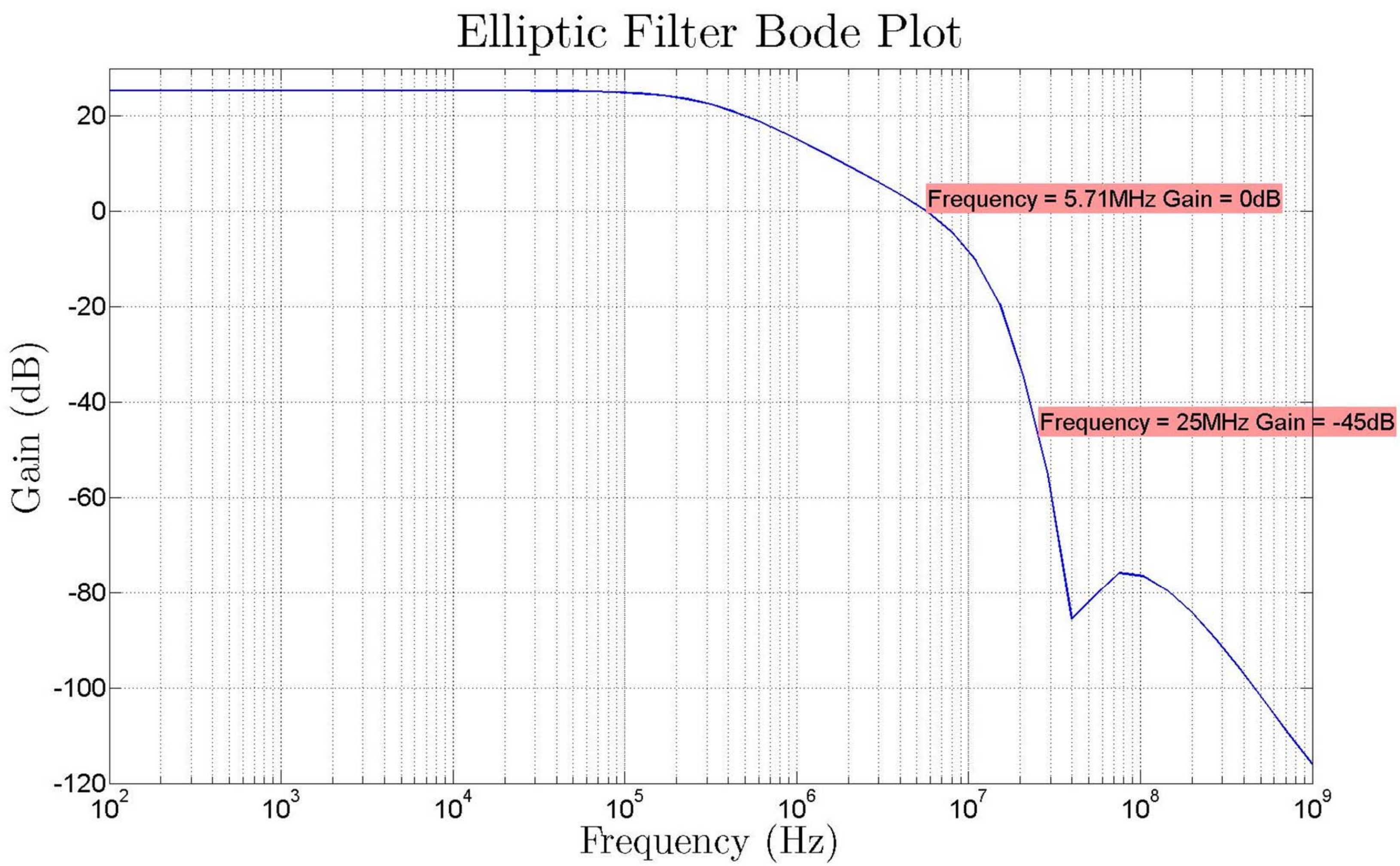


5^{th} Order Elliptic Filter

- Fully Differential Gm-C Filter
- Variable gain of from 0-25dB
- Roll-off ≈ -122dB/dec



Filter Bode Plot



DQPSK

- 2 Mbit/sec
  - Achieved using dibits, (d0,d1) representing in-phase (I) and quadrature (Q)

2 Mb/s DQPSK Encoding Table

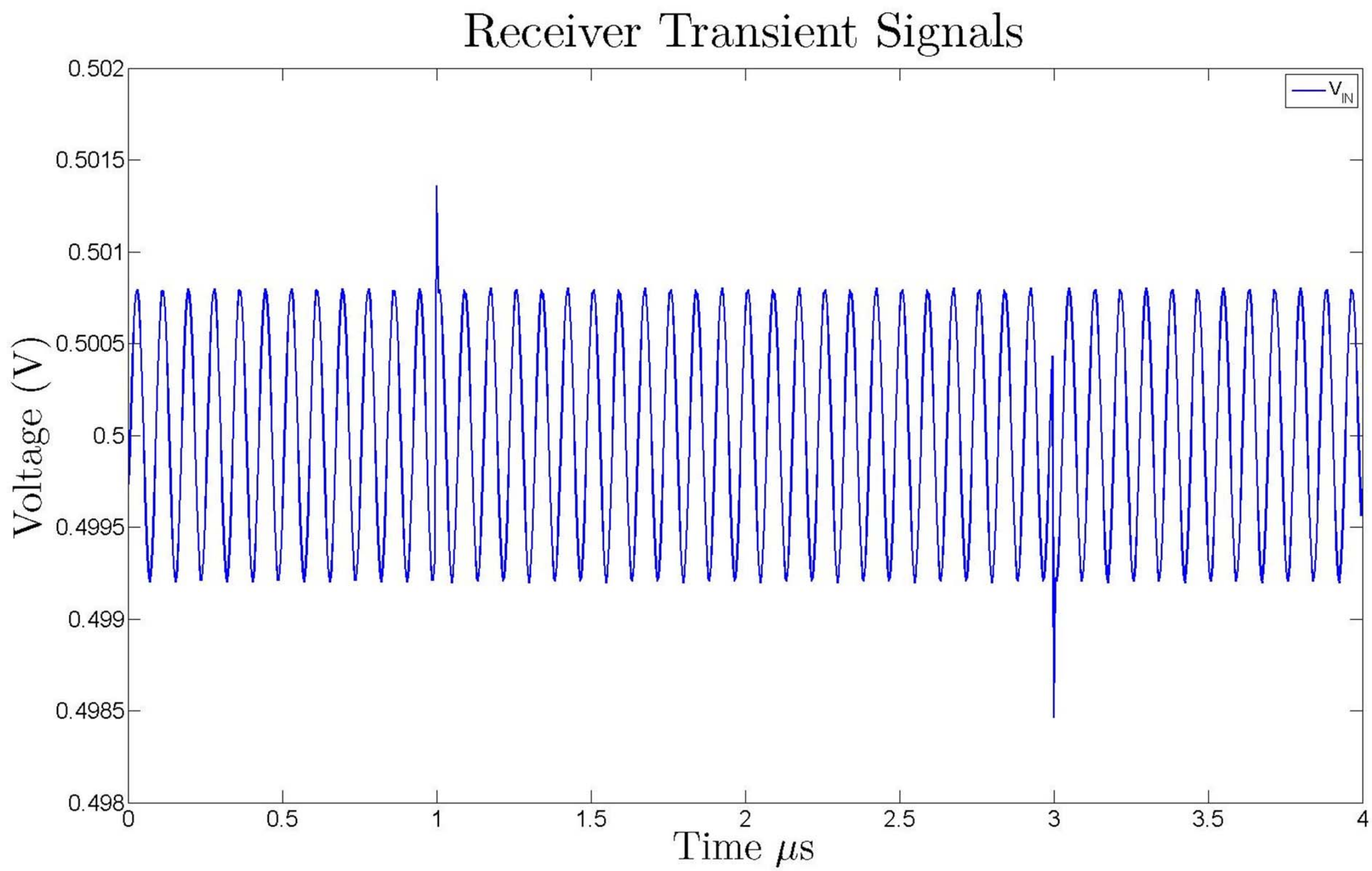
Dibit Pattern (d0,d1) (d0 is first in time)	Phase Change (+jw)
00	0
01	$\pi/2$
11	π
10	$-\pi/2$

CCK

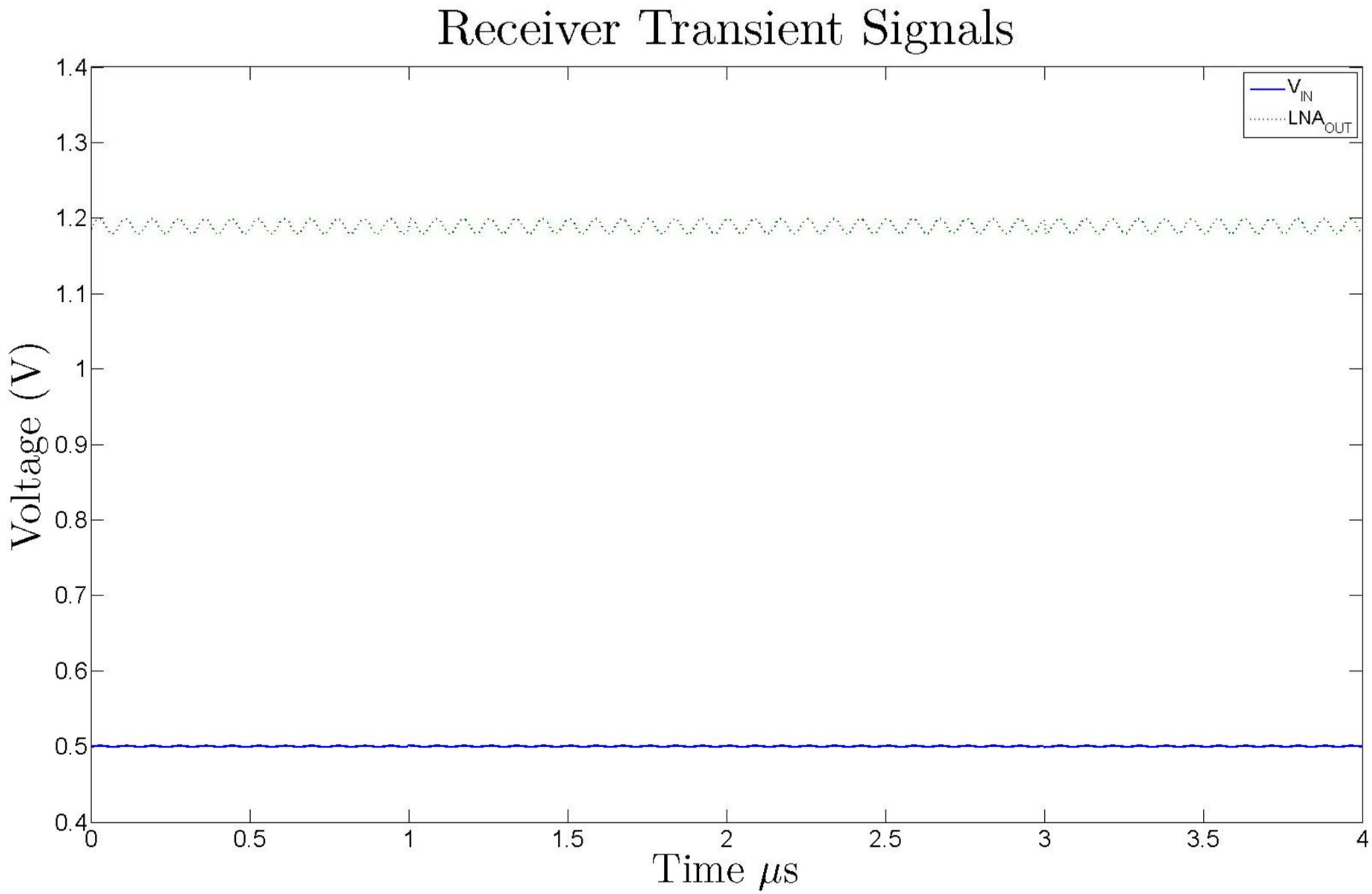
- Direct Extension of DQPSK
- Allows frequency spreading of data resulting in bandwidth of 5.5 and 11 Mb/s

$$c = \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j(\varphi_1)}\}$$

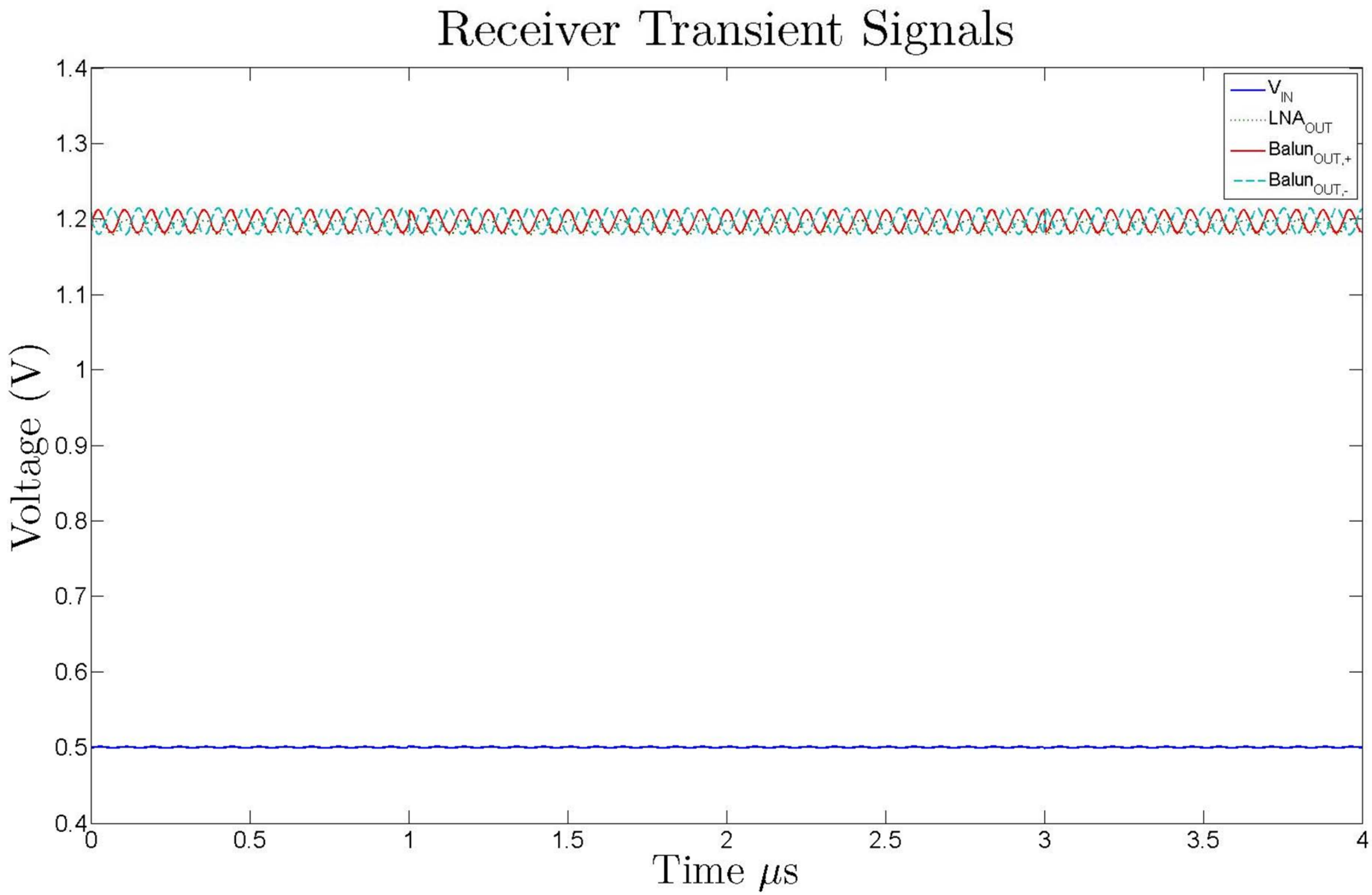
Symbol Transmission



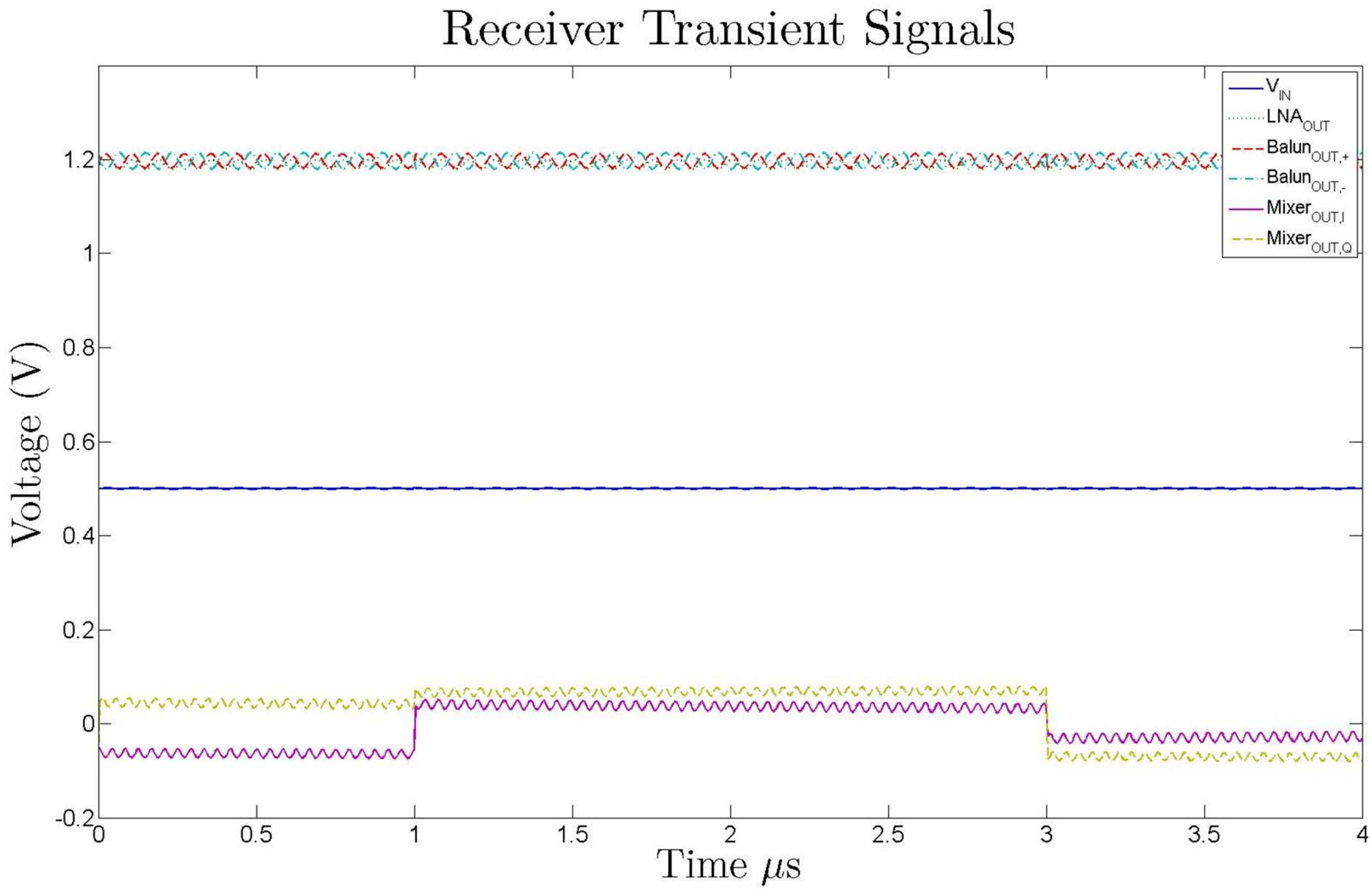
Symbol Transmission



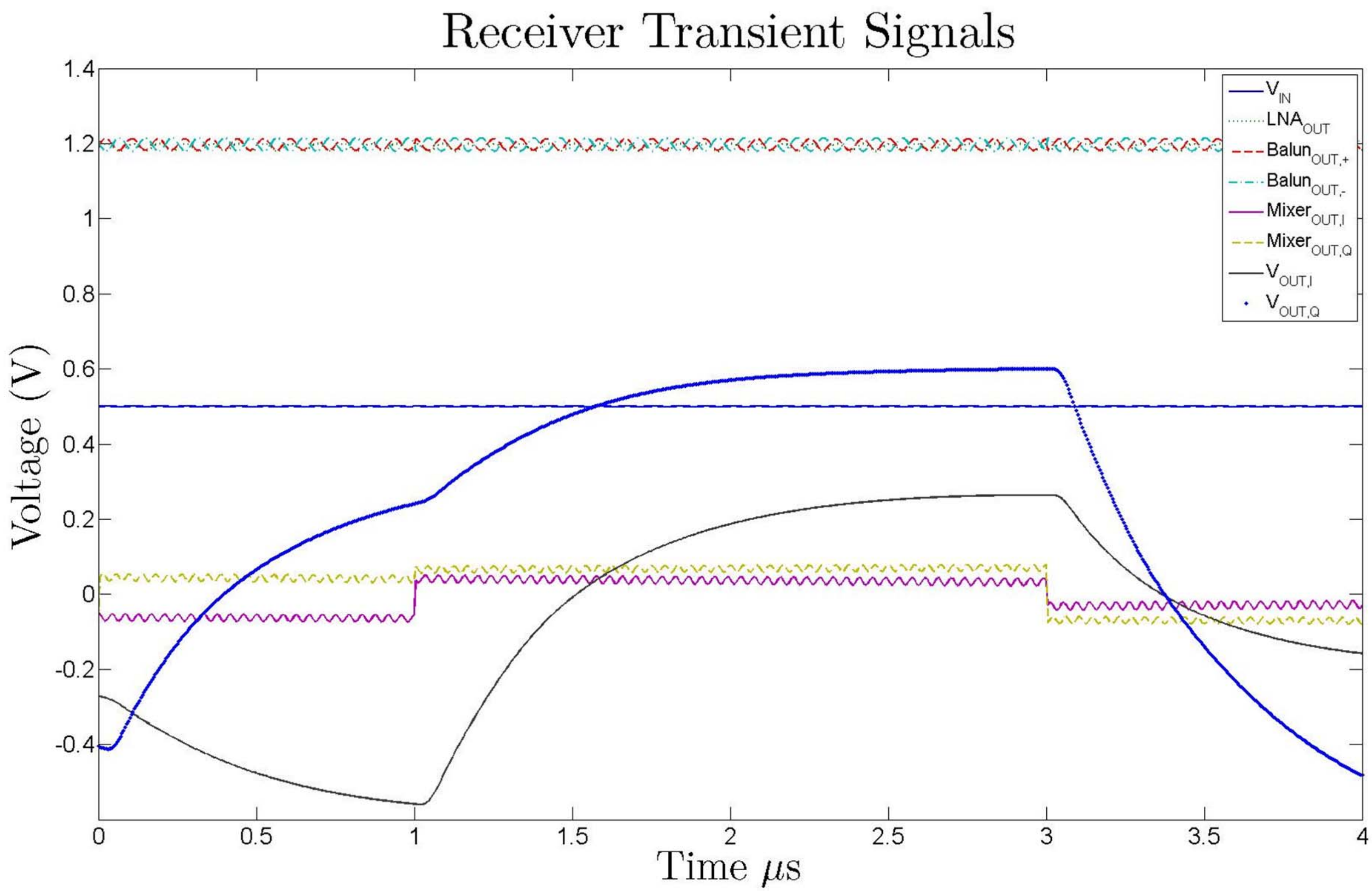
Symbol Transmission



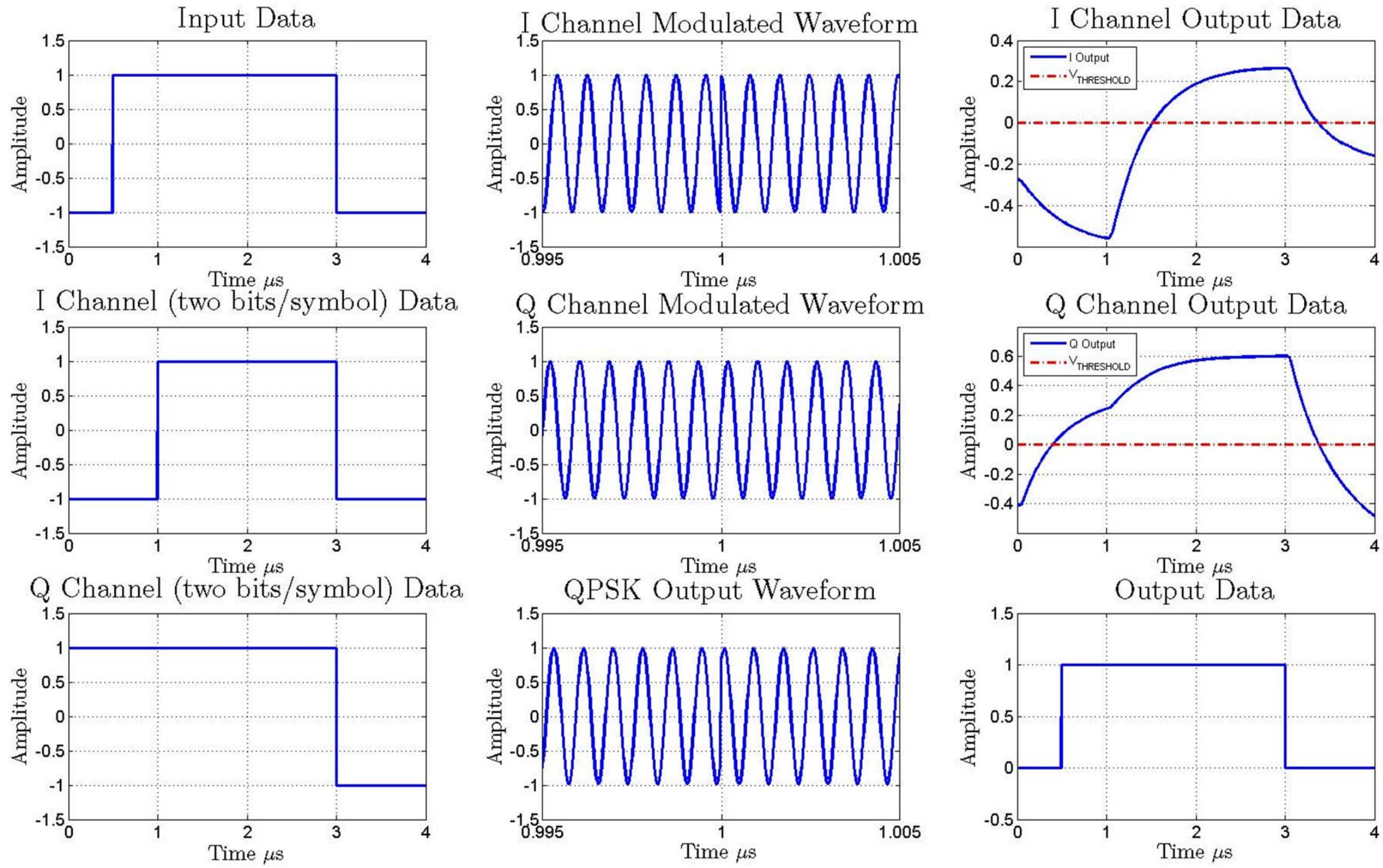
Symbol Transmission



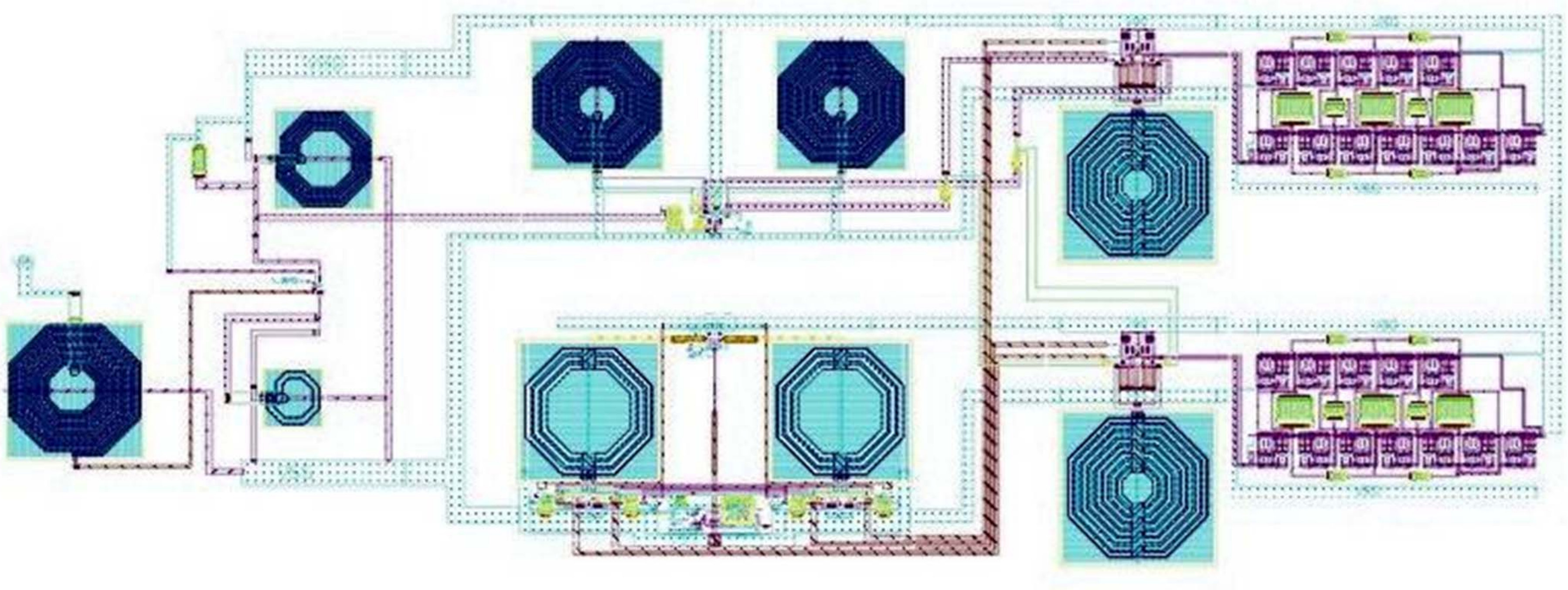
Symbol Transmission



Successful Data Recovery



Layout



Overall Results

Front End Comparison	This Work*	[40]	[41]
NFdsb	3.2 dB*	4.1 dB	5.2 dB
Gain	61 dB	25.1 dB	89 dB
Power	37 mW	22.7 mW	108 mW
Supply Voltage	1.2 V	1.8 V	1.8 V
Process	IBM .13 um CMOS	TSMC .18 um CMOS	IP6M .18 um CMOS

***Simulation results with ideal LO**

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