# Analog Front-End Direct Conversion Receiver for 802.11b Wi-Fi Applications

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*Abstract*—**This paper introduces the design of a Front-End Direct Conversion Receiver for 802.11b WiFi Applications. The chip was designed in .13 µm CMOS technology. Five main blocks are presented, the LNA, Active Balun, Mixer, QVCO with Frac-N PLL Stabilization and a Gm-C Channel Select Filter. The LNA block is a typical common source degenerated stage which has been cascoded. The mixer is a differential Gilbert cell which utilizes current bleeding and inductor degeneration for linearization. The QVCO is an LC-oscillator with PMOS tail current. It is controlled by a fractional-N type 2, 3rd order PLL. Lastly, a Gm-C filter will be constructed using multiple OTA cells organized to achieve a fifth-order Elliptic response.**

## I. INTRODUCTION

W IRELESS communications in today's society is in increasing demand. People are using multiple portable devices on a daily if not hourly basis. It has become rooted in our culture and as a result faster, smaller, higher quality RF components continue to be developed on all scales. The most possible wireless communications standard is that of wifi. Wireless hotspots are popping up all over today's cities, ranging from coffee shops, public parks, and university campuses. Coverage keeps getting broader and bandwidth demand keeps growing. As a result smarter more innovative designs are necessary.

## II. LNA

The purpose of the LNA in the receiver architecture is to reduce the noise figure of the entire system by having a large gain as can be seen from Frii's Equation. In receivers, it is more common to use a single-ended LNA because it consumes half the power while still giving the required results.

There are many topologies that can be considered to achieve this goal. A common source amplifier can provide enough gain so that the overall noise figure is minimized. However, resistors are noisy elements and would therefore be a source of noise in the circuit. To remedy this problem, the common source is inductively degenerated to provide the best noise performance because inductors are noiseless elements. The only issue with this is that inductors are very large devices and are difficult to place on-chip

The LNA above was designed using an inductively degenerated common source. The amplifiers are cascoded in order to prevent reflections from in the receiver. This is achieved because the gate of the cascoded transistor is AC grounded, decoupling the input from the output and effectively giving the reverse isolation.

Table 1: Simulation Results of LNA

| Ranges Quoted for 2.4-2.5 GHz | |
| --- | --- |
| NF (dB) | 2.3-2.4 |
| S11 (dB) | < -10 |
| S21 (dB) | 21-22 |
| Gain (dB) | 21-22 |
| P1dB (dBm) | -26 |

Narrow band operation around $\omega_o$ is achieved with the LC tank above the cascoded transistor. In addition to the inductive source degeneration the transistors have multiple fingers in order to further reduce the noise figure [14].

## III. BALUN

For single to differential conversion an active balun design was chosen in order to improve overall noise of the receiver front end. The active balun provides gain of around 12 dB with a noise figure of approximately 7 dB. Due to Friis equation this slackens the noise requirements of subsequent stages, most specifically the mixer as these components tend to be the noisiest. In accordance with 802.11b Wi-Fi standards the balun was designed to operate with RF signals as low as -50 dBm assuming an LNA gain of around 25 dB.
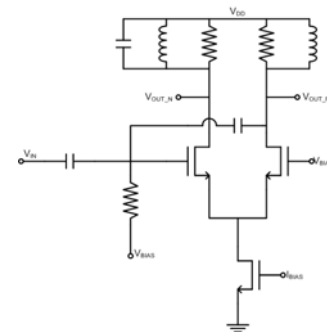


Figure 1: Balun Schematic

The topology used was chosen because of it's to ensure differential outputs. In a traditional topology there is a zero at the inverting output at a really low frequency compared to the non-inverting output [6]. This is the main contributor to the phase error at the output. Since 802.11b uses QPSK for its modulation technique phase errors can present a huge problem since we need both I and Q channels. To alleviate this problem a feed forward capacitor is added between the input and positive output. This effectively lowers the frequency of the zero at the non-inverting output to reduce the phase error in single to differential conversion. This introduces a small problem however. Now the capacitance looking into the

outputs is no longer equal. To compensate for this a balancing capacitor is added in parallel with the load inductor and resistor of the inverting output to ensure the capacitance at the outputs is equal [6].
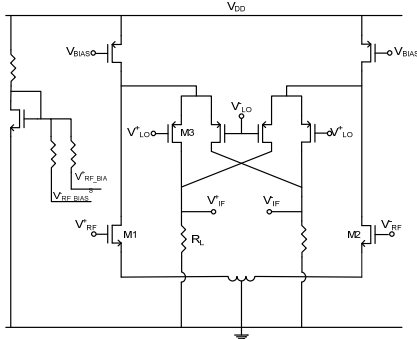
## IV. MIXER



Figure 2: Mixer Schematic

The design goals for the mixer were to achieve a high conversion gain, low noise figure, low flicker noise contribution, and a moderate to high linearity. A traditional Gilbert cell mixer was the topology of choice at first due to its gain and high port to port isolation. Such a topology lends itself well to heterodyne architectures where flicker noise is not a problem. In an attempt to degrade the effect of flicker noise, reduce the required headroom and maintain a high conversion gain a folded version of the Gilbert cell topology was chosen.

### A. Linearity

The majority of non-linearities occur from the transconductance stage of the mixer provided the current flowing through the commutating stage isn't so large as to degrade them too far from ideal switching [7]. Also, folded circuit topologies generally exhibit a lower linearity than there non-folded counterparts. As a result to increase the linearity a high bias current in the transconducting stage is used along with removing a tail current source. Removing the tail current source increases the linearity at the expense of common mode rejection. Linearity is further increased with a degeneration inductor which was center tapped to save on area.

### B. Gain

An advantageous aspect of the folded topologies is the fact that the bias currents of the commutating and transconducting stages can be chosen separately. A large bias current was then driven through the input transistors, increasing their gm values. Also since a smaller current now flows through the commutating stages a larger load resistance can be used due to fewer drops across it [8].

### C. Noise

The hardest challenge with the mixer was reducing overall noise figure and flicker noise especially due to the fact that the receiver is direct conversion. The folded topology helps with flicker noise due to the PMOS commutating pairs. Due to the higher isolation they are less susceptible to substrate noise. Also flicker noise is directly proportional to $g_{m3}$ which is reduced by decreasing bias current and since we can now drive a smaller current through the commutating pairs, it not only helps the linearity of those pairs but now is realizing the goal of lowering flicker noise contribution.

$$\bar{\iota}_{dn}^2 = 4kT\frac{\gamma}{\alpha}g_m\Delta f + \frac{K}{f}\frac{g_m^2}{WLC_{ox}^2}\Delta f$$

Also seen from the equation the flicker noise decreases with increased area. The commutating pairs were made slightly bigger but kept at minimum lengths to ensure proper switching. Flicker noise due to the transcondutance stage is irrelevant due to the fact that it will be unconverted far away from base band and can easily be filtered out. The overall noise figure away from DC was also improved due to the large power consumption and high gain of the input transconductance stage as well. The following are plots illustrating gain and noise figure of the Gilbert type mixer.

Table 2: Simulation Results of LNA

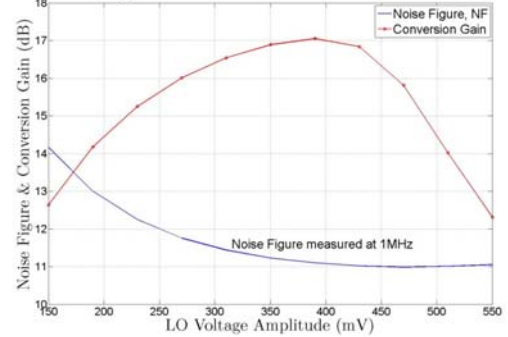| Reference | This Work | [8] |
|---|---|---|
| NF dsb (dB) | 11.25 | 7.146 (ssb) |
| Conversion Gain (dB) | 16.9 | 18.6 |
| IIP3 (dBm) | -4.83 | -8.77 |
| P1dB (dBm) | -13.5 | N/A |
| LO-RF Isolation (dB) | -97 | N/A |
| LO-IF Isolation (dB) | -80 | N/A |
| CMOS Process | .13μm | .18μm |
| Current (mA) | 7 | 5.78 |
| Voltage (V) | 1.2 | .9 |



Figure 3: Mixer Noise Figure and Conversion Gain versus LO Amplitude

## V. LOCAL OSCILLATOR

### A. Local Oscillator (LO) 802.11b Requirements

The 802.11b Standard transmits packets using the differential quadrature phase shift keying (DQPSK). Therefore, the receiver has to split the received signal into I & Q signals. The standard way to achieve this, is by using an LO that produces oscillating signals that have a 90° phase difference. Additionally, the Standard is made up of 11 different frequency channels spaced 5MHz apart. For direct conversion, this requires that the LO must lock into 11 different oscillation frequencies without drifting into neighbor channels. A Phase-Locked Loop (PLL) is implemented in order to satisfy these requirements.

## B. Overall PLL Structure

A Phase-Locked Loop utilizes feedback to stabilize the output frequency. This feedback is dynamic, allowing it to lock onto multiple output frequencies. The system can be seen in figure 4. It begins by taking the output of a voltage controlled oscillator (VCO) and divides the high frequency signal to much lower frequency signals. This divided signal is compared to a reference frequency, commonly produced from a crystal oscillator. The comparison is done using a phase-frequency detector (PFD) which outputs two digital signals, UP & DOWN. These digital signals control current that either inject or remove charge from a loop filter, H($s$). This loop filter effectively averages the two digital signals seen from the PFD resulting in a DC voltage, which controls the VCO.
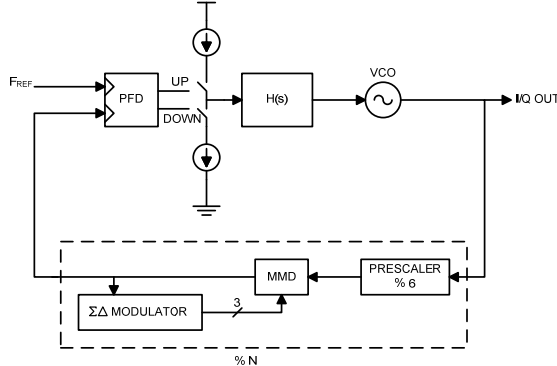


Figure 4: Phase-Locked Loop block diagram.

If the VCO output frequency is too high, the PFD will trigger a DOWN signal, which will then cause the charge pump to pull charge off the loop filter. This decrease in charge decreases VCO tune voltage that, in turn, decreases the oscillation frequency. This process is repeated until the divided down signal is in phase and the same frequency as the reference signal.
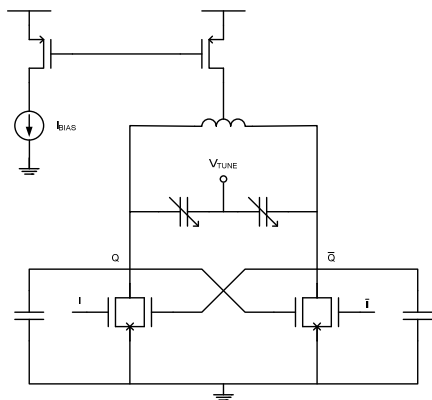
## C. Quadrature Voltage-Controlled Oscillator



Figure 5: Half of the Quadrature Voltage-Controlled Oscillator.

The VCO is shown in figure 5, where only one of the two VCOs is shown. A second VCO is attached to this where $Q$ & $\bar{Q}$ are replaced with $I$ & $\bar{I}$, and $I$ & $\bar{I}$ are replaced with $\bar{Q}$ & $Q$. In this cross-coupled configuration, the VCOs will be forced to stabilize with 90º phase differences resulting in the desired QVCO. A PMOS tail is favored, over NMOS, because with

NMOS, the output signal swings around the voltage rail. This requires the output to be AC coupled and DC biased before continuing to additional stages, furthering complexity and increasing power [35].

## D. Divider

The divider for this PLL is a fractional-N divider, which allows for the use of a higher reference frequency and lower PLL noise. With integer-N, the reference frequency must be the channel spacing frequency in order to lock into each channel, however, with a fractional-N divider, much higher reference frequencies can be used because the divider can lock into fractions of the reference. The noise from the charge pump, seen at the VCO output, is proportional to $N^2$, so with a higher reference frequency, the amount of division required decreases, lowering overall output noise. Fractional-N division is achieved by modulating between multiple division ratios. A division ratio of 60.5 could be a result of dividing by 60 or 61 every other cycle. This will average out to 60.5, however, this periodic switching will also propagate through the PLL resulting in spurious tones at the VCO output. In order to avoid this problem, a 3rd order MASH ΣΔ modulator is used to randomly switch between integer division values.

The divider components themselves, consist of a prescaler and an 8/15 multi-modulus divider (MMD). The prescaler divides the VCO output by 6 using current-mode logic, due to its ability to handle high frequencies [30]. This prescaler is needed to bring the oscillation frequency down to a manageable level for the MMD digital blocks. The MMD can be seen in figure 6, where the divide ratio is controlled by input bits R0-R2 which are randomly generated from the ΣΔ modulator [22]. It consists of three cascaded 2/3 cells which divide by 2 when R is low and 3 when high. The total divide ratio for this block is: [32]
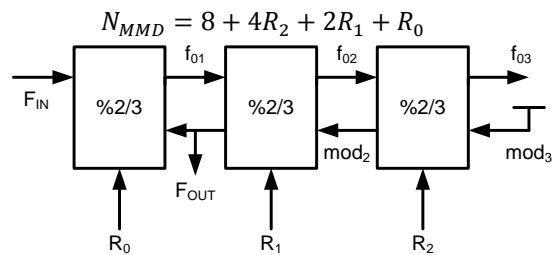
$$N_{MMD} = 8 + 4R_2 + 2R_1 + R_0$$



Figure 6: Multi-Modulus Divider.
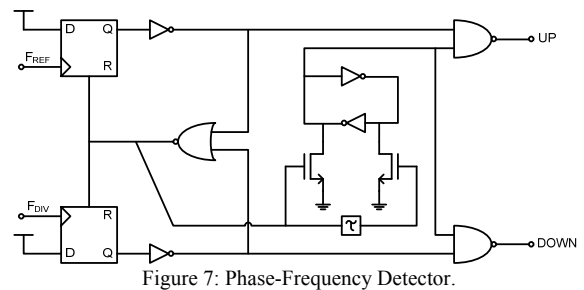
## E. Phase-Frequency Detector



Figure 7: Phase-Frequency Detector.

The PFD is similar to the traditional PFD with two D-Flip Flops with data tied high and a reset control. The differences are that instead of delaying the reset control to prevent a dead

zone, the DFFs are reset immediately and the delay occurs with the outputs of the PFD [15]. The delay is controlled by the τ block. This configuration still eliminates the dead zone problem, but now allows the next input transition to be sensed, even when the delay path is not ready.
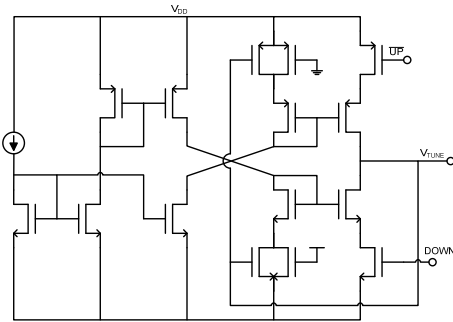
*F. Charge Pump*



Figure 8: Charge Pump.

The charge pump consists of current mirror stages to assure the up and down currents are equivalent. There are also two feedback transistors that help with output linearity. Near the rails, the output current speaks due to non-linearities, without feedback. In this voltage range, however, the feedback transistors go into the linear region causing the mirrored current to decrease resulting in increased linearity [16].

*G. Loop Transfer Function Stability*

The PLL feedback system must be stable to achieve locking. In order for this to occur, the loop bandwidth must have a phase margin (PM) greater than 0°. Conventionally, a PM of 50-55° is desirable for PLLs [32]. From figure 9, it can be seen that this PLL exhibits a PM of 53.4°. Additionally, a loop bandwidth of over a decade below the reference frequency is desired allowing the loop to average out drastic changes. For this we targeted a bandwidth of 1MHz, however settled with 250kHz due to unreasonable passive device sizes in the type 2, 2nd order passive loop filter.
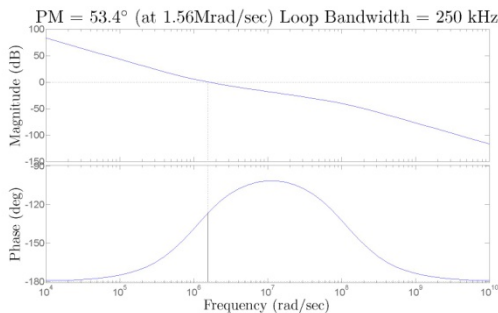


Figure 9: PLL Loop Transfer Function.

## VI. GM-C FILTER

In the design of the receiver front end, an efficient filter is needed to filter out unwanted signals and to keep the signal from overlapping into other channels. There are three main types of filters that are usually implemented: RC active filters, MOSFET-C filters and OTA-C (Gm-C) filters. The most

common type of filters used for this type of application is the Gm-C filter. The reason that these types of filters are used is because they can operate in a wide band of frequencies from several hundreds of kHz to more than 100 MHz. One of the main disadvantages of the Gm-C filter is the low linearity due to the fact that it relies on the linearity of the operational transconductance amplifier which is also low. This issue must be addressed in order to design a high linearity filter.

The transconductor was designed to have the highest linearity possible. Therefore, the transistors M1-M4 are kept in triode because triode devices are linear. To further improve linearity, the degeneration transistors M5 and M6 are also in triode region. The way that the degeneration transistors keep the circuit linear is by compensating for small changes in voltage in the V1 and V2 nodes. This compensation comes from the small signal resistance of the transistors. As the voltage changes, The resistance decreases which causes an increase in V1 and V2. Because there will be many of these OTA's cascaded, there is also common mode feedback to make sure that the DC voltage stays constant.
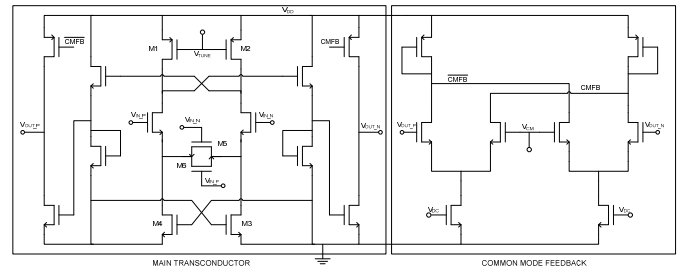


Figure 10: OTA Cell

For the receiver, a fifth order elliptic filter was implemented. An elliptic filter was chosen over Butterworth and Chebyshev because it gives the sharpest rolloff of the three. The disadvantage of the filter is that there is ripple in the pass and stop-band that can affect the signal. However, if the signal is attenuated enough, the ripple will be insignificant. From the plot we can see that the signal attenuates to -80 dB before the ripple which is more than adequate.
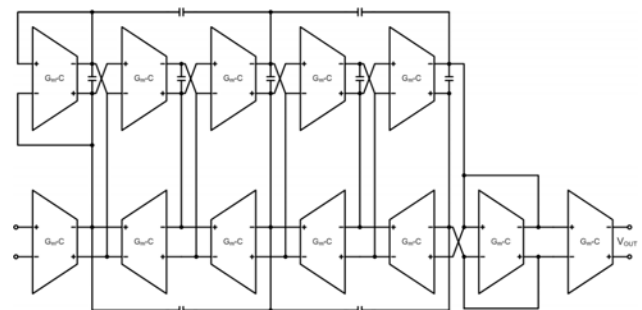


Figure 11: 5th Order Elliptic Filter

The plot below shows the response of the filter. The unity gain frequency, where attenuation begins, is at 5.71 MHz. Another important result was the attenuation at 25 MHz. The 802.11b standard requires that there be at least 27 dB attenuation in order to keep the signal from interfering with another channel. The 25 MHz comes from the fact that the spacing between channels is 22MHz. For this filter design, we

have achieved an attenuation of -45, which is well below the 27 dB needed. The filter also has a range of gain from 20-25 dB depending on the value of VTUNE [1],[12].
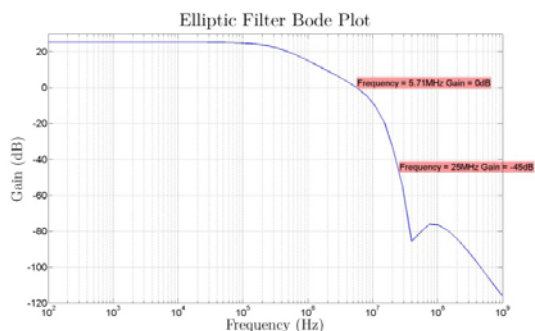


Figure 12: Elliptic Filter Response

## VII. OVERALL RESULTS

A results comparison can be seen in Table 3. This receiver achieves very good noise figure and gain while consuming a reasonable amount of power. Figure 7 shows data transmission and recovery through this receiver. An input stream is first split into I/Q data channels and then converted to transmitted waveforms. These waveforms propagate through the receiver and the output is shown on the top right graphs. A threshold voltage of 0V is used to define bit transitions. As can be seen in the final graph, the sent data is accurately recovered.

Table 3: Receiver Results

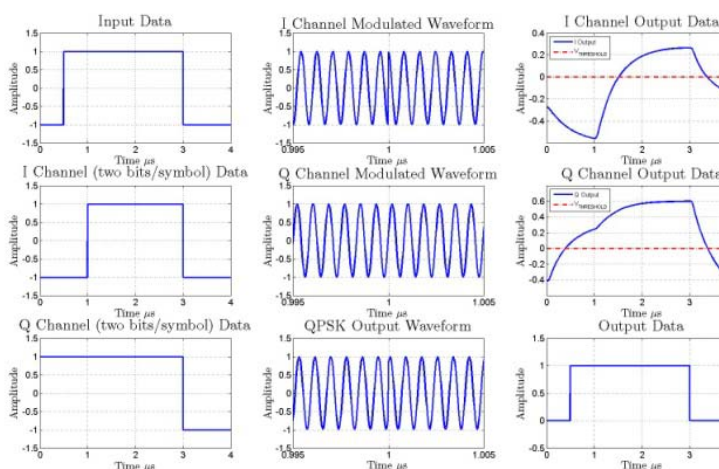| Front-End Comparison | This Work | [31] | [19] |
|---|---|---|---|
| NF dsb (dB) | 3.2 | 4.1 | 5.2 |
| Gain (dB) | 61 | 25.1 | 89 |
| Power (mW) | 37 | 22.7 | 108 |
| CMOS Process | .13μm | .18μm | .18μm |
| Supply Voltage (V) | 1.2 | 1.8 | 1.8 |



Figure 13: Successful Data Recovery

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