A Fully-Integrated Direct-Conversion RF Front-End for Wi-Fi

Zhengjia Lu, Jianmin Li, Zhicheng Wei

***Abstract* – A fully-integrated direct-conversion RF front-end for Wi-Fi application in the 2.4GHz band is presented in this paper. This RF front-end is designed and simulated with the 0.13µm cmrf8sf model in Cadence. The whole system simulation is performed and compared with proposed specifications. The receiver achieves a noise figure of 1.6dB and voltage gain of 50dB. The phase noise for the QVCO is -123dBc/Hz at an offset of 1MHz. The IIP3 for the whole system is -11dBm and P1dB point is -18.92dBm.**

***Index Terms*– Direct-conversion, RF CMOS, LNA, mixer, QVCO, low noise.**

I. Introduction

In recent years, the world of wireless communication system is rapidly growing. As a result, the fully integrated wireless connectivity devices become the mainstream of the market. As a critical part of the receiver, the performance of RF front-end plays a significantly role in the whole system.

The heterodyne architecture is widely used in the past for wireless receivers. One main drawback of this architecture is it needs an image-reject filter before the mixer to eliminate the image frequency. However, this image-reject filter is usually realized by passive external components and not preferable to the current trend to achieve a fully integration chip. As a result, direct-conversion receiver, also known zero-IF receiver, is prevalent in receiver designs for its high integration level and avoidance of the interference of the image frequency. In addition, it reduces the basic circuit complexity.

Wi-Fi is a wireless communication protocol within the frequency range from 2.4 GHz to 2.4835 GHz. Wi-Fi communication is commonly used for wireless networking.

II. WI-FI Standard and Applications

Wi-Fi, as quoted from Wi-Fi Alliance, is "A certification mark developed by the Wi-Fi Alliance to indicate that wireless local area network (WLAN) products are based on the Institute of Electrical and Electronics' (IEEE) 802.11 standards" [1].

Wi-Fi can be used as a tool to access the internet by personal computers, video game consoles, mobile phones, MP3 players or personal digital assistants within range of a wireless network connected to the Internet. Wi-Fi also allows communications between computers directly. This is called

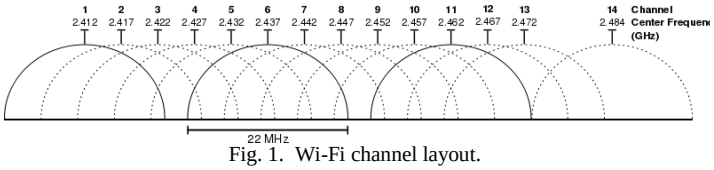

Fig. 1. Wi-Fi channel layout.

the ad-hoc mode of Wi-Fi transmission. For some reasons including security, this mode has rarely used for transfers from one computer to another directly. However, there is a new method named Wi-Fi Direct which is promising to improving the ad-hoc mode for quick file transfers and media sharing.

There are 14 overlapping channels within the Wi-Fi frequency range which have a 22MHz bandwidth each. The channel layout is shown in Fig.1. Channels 1, 6 and 11 are commonly used since there is no overlap between these channels. In this project, channel 1 (2.412GHz) is chosen as working channel for this receiver.

III. Circuit Operation and Analysis

A. Block Configuration of the System

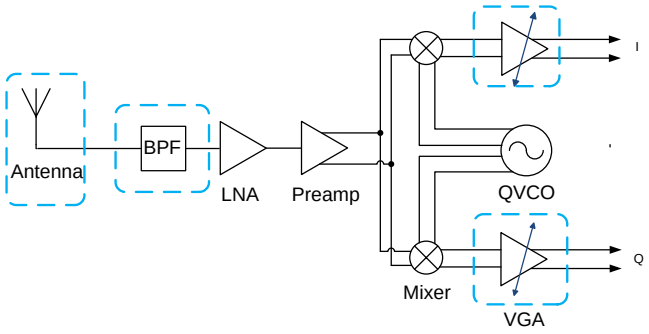

Fig.2 Receiver architecture

The overall receiver architecture is shown in Fig.2. The Wi-Fi signal is received by the antenna. A band-pass filter (BPF) following the antenna is used to filter out the undesired frequency elements. Surface acoustic wave (SAW) filter is commonly used as this BPF in industry due to its sharp roll-off property. Then the signal from the BPF is amplified by the low-noise amplifier (LNA). The objective of LNA is to achieve a low noise performance while maintaining a decent gain. To obtain a sufficient gain for the whole receiver, a pre-amplifier is utilized after LNA. At the same time, this pre-amplifier is used as the single-ended-to-differential converter to provided differential signals to the double-balanced mixer. In addition, by placing this pre-amplifier between the LNA and mixer, the LO leakage to the LNA can be significantly reduced [2] and dc-offset can be reduced as well. The

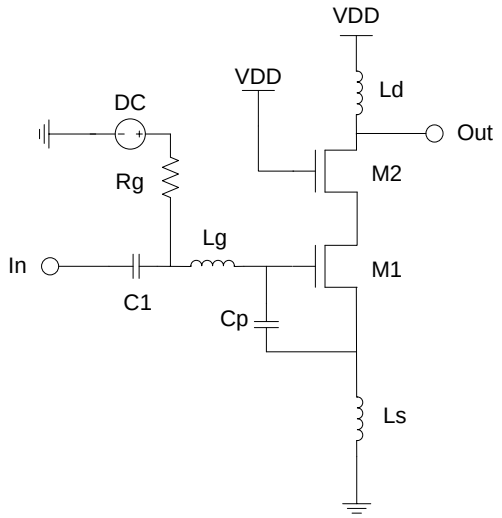

Fig.3 Schematic of the LNA

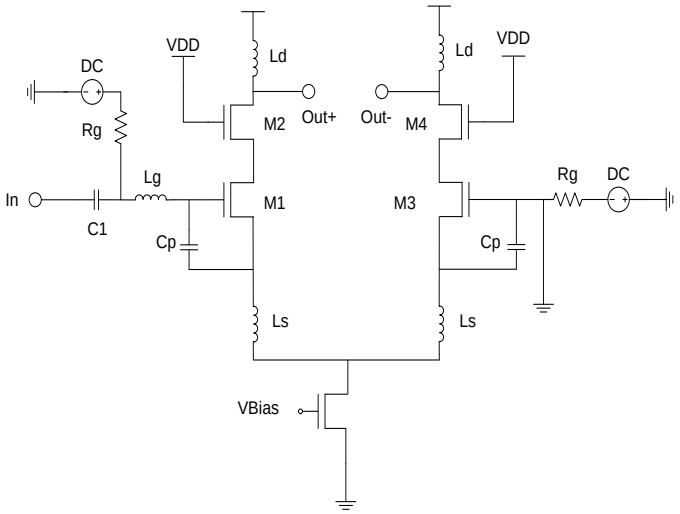

Fig.4 Schematic of the pre-amplifier

amplified RF signal is then down-converted to the baseband by double-balanced mixer. The quadrature VCO (QVCO) is used to generate quadrature signals for mixers.

B. LNA

The schematic of the LNA is shown in Fig.3. A single-stage cascode amplifier topology with inductive degeneration at the source is utilized. The single-stage is chosen to improve the 1dB compression point, increase the input referred third-order intercept point (IIP3) and minimizes the power consumption. The cascode topology is chosen to improve the isolation between the input and output nodes and it increases the output resistance to achieve a higher gain. In addition, the inductive degeneration is utilized here to achieve both the input impedance matching and noise matching. The frequency is set by Lg, Cp and Cgs at the same time. Because LNA is the first component after the BPF, the noise performance is critical for the whole receiver based on the Friss equation. As a result, the primary goal for the LNA is to achieve the low noise figure while maintaining a decent gain. The performance of LNA is shown is Table 1. As shown in Table 1, the noise figure is quite low (1.242dB) at working frequency, which is significant for the whole system to achieve a low noise figure.

C. Pre-Amplifier

The pre-amplifier is shown in Fig.4. A differential amplifier with one side at small signal ground is utilized to realize single-ended-to-differential conversion. Additional 17.98dB gain can be achieved by this amplifier. In addition, by placing this pre-amplifier between the LNA and mixer, the isolation between the LO and RF channel can be improved. Half circuit of the pre-amplifier use the similar topology as the LNA. The performance of this pre-amplifier is shown is Table 2.

TABLE 1
LNA PARAMETERS

Specification	Measurement Result
Gain(dB)	18.55
Noise figure(dB)	1.242
Return loss(dB)	-19.17
P1dB(dBm)	-9.3
IIP3(dBm)	-3.68

TABLE 2
PRE-AMPLIFIER PARAMETERS

Specification	Measurement Result
Gain(dB)	17.98
Noise figure(dB)	1.78
Return loss(dB)	-21
P1dB(dBm)	-11.7
IIP3(dBm)	-3.79

D. Mixer

Mixers are necessary components in almost all wireless communication systems, which can covert one frequency to another by working with the local oscillator. In general, mixers can be divided into two groups, passive mixers and active mixers. The popular passive mixers are passive diode mixers, which are easy to design. On the other hand, active

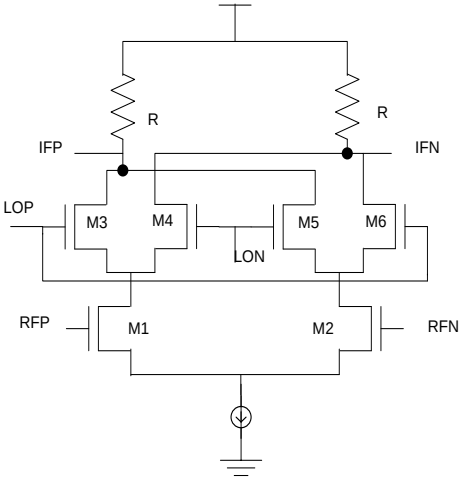

Fig.5 Schematic of the LNA

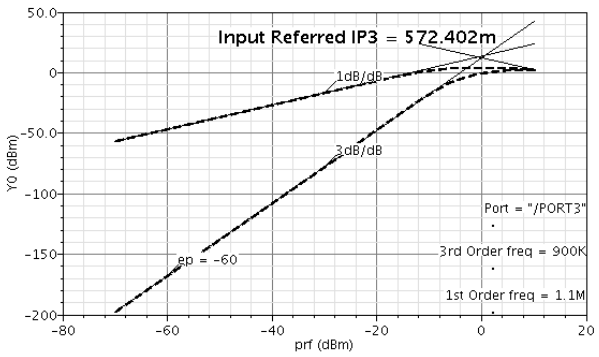

Fig.6 IIP3 Simulation Result of Mixer

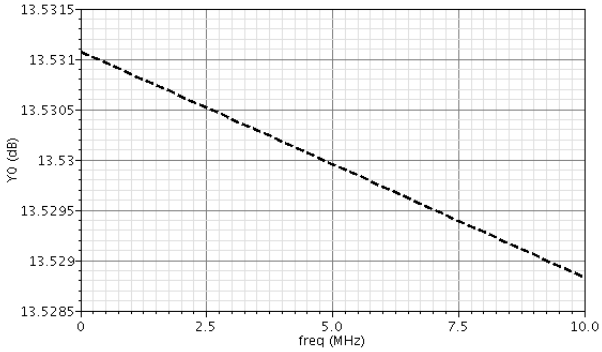

Fig.7 Conversion Gain Simulation Result of Mixer

mixers usually consist of transistors, which are known as transconductance mixers. The active mixers have advantages that they can provide an additional conversion gain. In addition, they have lower noise figure compared to the passive ones [3]. In our design, double-balanced Gilbert mixer is chosen using a differential pair to achieve the transconductor implementation. Gilbert mixer is the most commonly used active mixer. It has the most desirable characteristics in terms of isolation and harmonic suppression due to its balanced structure.

A double-balanced Gilbert cell mixer for this project is shown in Fig.5. The 1.5V voltage supply is applied. The RF signal is applied to the tail differential transistor pairs while LO signals commutating for the Gilbert cell.

Drains of transistor M1 and M2 are connected to the double-balanced Gilbert core with four transistors, which are driven by the differential signals from QVCO. When the LOP is high and LON is low, M3 and M5 turn on and M4 and M5 turn off. Then the mixer structure turns out into a typical differential amplifier structure. When the opposite scenario occurs, i.e. LOP is low and LON is high resulting in M3 and M6 turn off and M4 and M5 turn on, mixer turns out to be a symmetric differential amplifier. The different part for these two scenarios is that when one IF output is positive, the other one is negative. As a matter of fact, four transistors, M3 to M6, serve as a switch [4]. The conversion gain is expressed in the equation below:

$$A_{RFtoIF} = \frac{2}{\pi}(g_{m\_M1}R_L) \qquad (1)$$

TABLE 3
MIXER PARAMETERS

Specification	Measurement Result
Conversion Gain(dB)	13.53
Noise figure(dB@10MHz)	32
Power(mW)	4.95
P1dB(dBm)	-9.3
IIP3(dBm)	-0.57

A current source is added to force the output currents to be balanced at the bottom of the mixer. If the input voltage is perfectly balanced, the output current is also balanced. And another important aspect is that there are no degeneration inductors between the RF input FET and the current source. On the premise of meeting the specification, it needs less area in the layout. The conversion gain and the IIP3 are the key parameters for mixer design. IIP3 and conversion gain for this mixer design are shown in Fig.6 and Fig.7 respectively. As can be seen in these two figures, a relatively good gain is obtained and a nice input referred IP3 is achieved. Other simulation results of the mixer are summarized in Table 3.

E. QVCO

The availability of the quadrature signals is significantly important for the receiver with direct-conversion architecture. There are several methods to generate quadrature signals. Among these approaches, RC polyphase filter [5] can be utilized after the outputs of VCO to achieve such quadrature signals. However, this method introduces huge power consumption and poor phase noise. Another approach is to use a double frequency VCO with divider circuit. The drawback for this method is that it needs to work at higher frequency and additional divider circuitry is required. The third approach to obtain quadrature signals is to use two symmetric LC-tank VCOs coupling to each other, which exploits the good phase noise performance of LC oscillators. The first implementation of such principle is the quadrature VCO (QVCO) proposed by Rofougaran et al. [6]. The principle of this QVCO is shown in Fig.8. As shown in Fig.8, the combination of a direct connection and a cross connection make two VCOs oscillate in quadrature.

The MOS-coupled quadrature VCO for this project is shown in Fig.9. This QVCO consists of two cross coupled VCOs generating two pairs of differential signals with 90º phase shift. Low supply voltage (1.5V) is utilized for this QVCO. X-coupled oscillator structure is used to provide the negative resistance to make this oscillator start oscillating. The LC tank in the middle determines the oscillating frequency. Due to the process variation, oscillating frequency is often not accurate. As a result, voltage controlled structure is necessary

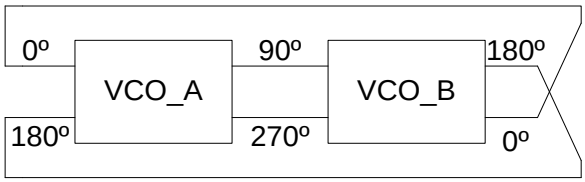

Fig.8 Block diagram and phase relations for a QVCO

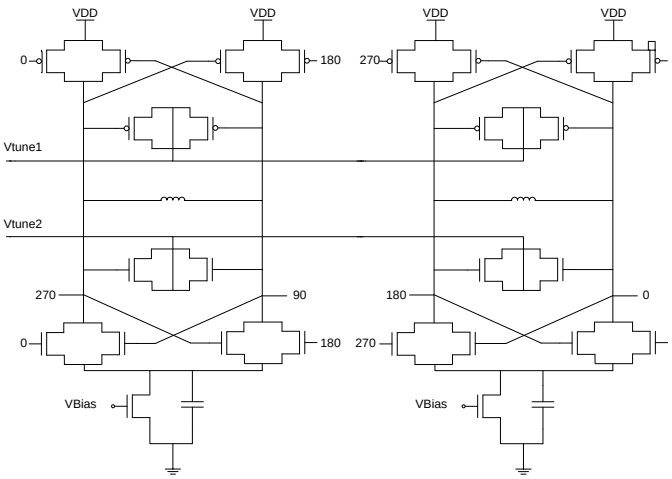

Fig.9 Architecture of QVCO

to obtain an accurate oscillating frequency. Two pairs of FET varactor are implemented with tuning voltage Vtune1 and Vtune2 to achieve a wider tuning range. In order to have a big capacitance, FETs for varactors have a relatively big width. However, compared to the capacitors, FETs still hold the advantage of smaller area. The FETs varactors and inductor in the middle constitute the LC tank. Tail current source is used to provide bias current. This bias current can be adjusted to achieve a rail-to-rail voltage swing for the LC tank. The tail capacitor is utilized here to reduce the drain current waveform in the duty cycle, leading to the reduction the drain noise of the differential NMOS and PMOS transistors. Therefore, this capacitor is helpful to reduce the total phase noise.

The most import characteristics of oscillators are frequency tuning range and phase noise. Tuning range is determined by the tuning voltage Vtune1 and Vtune2. Phase noise is the frequency domain representation of short-term, random fluctuations in the phase of a waveform. The relations between quadrature accuracy and phase noise in the typical MOS-coupled QVCO have been discussed [7]. The simulation result shows the some phase noise is contributed from low-frequency flicker noise from coupling MOS. Tank voltage amplitude also has an important effect on the phase noise of VCO[8]. The expression of phase is shown as an equation below [9].

$$L\{\Delta w\} = 10log_{10}\left(\frac{\overline{i_n^2}/\Delta f}{q_{max}^2}.\frac{\Gamma_{rms}^2}{2\Delta w^2}\right) \qquad (2)$$

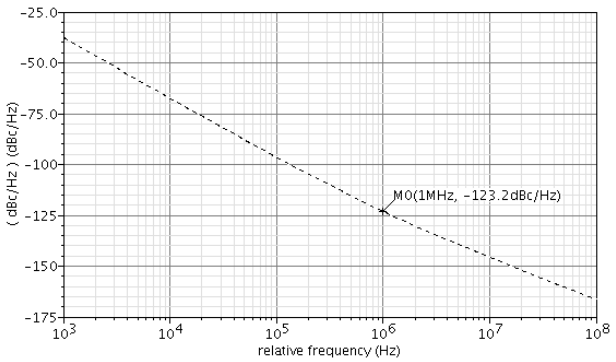

Fig.10 Plot of phase noise

Where $\overline{i_n^2}/\Delta f$ is the power spectral density of the parallel current noise, Γ_{rms}^2 is the rms value of the impulse sensitivity function (ISF), q_{max} is the maximum signal charge swing, and Δw is the offset frequency from the carrier. As equation (2) shown, phase noise is inversely proportional to the tank voltage amplitude. As a result, increasing the tail current will improve the phase noise due to the increase in the oscillation amplitude. The bias current should be adjusted to make oscillator work at the boundary between current-limit regime and voltage-limit regime. [8] In addition, the widths of the cross-coupled NMOS and PMOS transistors can be increased to achieve a lower Vdsat, which leads to an increase in the oscillation amplitude. Because another important noise source is transistors in VCO, bigger size of transistors is preferable to be used to achieve a low phase noise. For example, 20dBm improvement at 1MHz offset can be achieved after changing widths of transistors from 130nm to 500nm. As shown in Fig.10, the phase noise for the QVCO presented in this paper is -123.2dBc/Hz at 1MHz offset frequency.

IV. LAYOUT AND SIMULATION RESULT

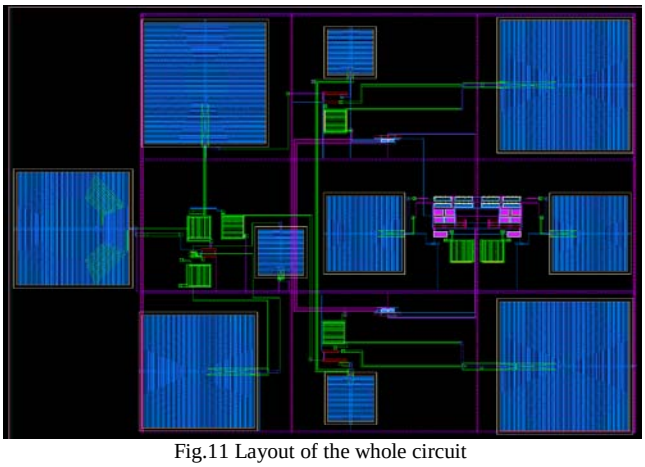

Fig.11 Layout of the whole circuit

The die photo of the layout is shown is Fig.11. RF layout is different from the analog layout. RF layout should be simple and less crowded. One important thing in drawing RF layout is that source to ground connections should be short and wide enough to avoid ground inductance which will kill the gain of the system. In addition, the RF signal path should be as straight as possible. On the whole, getting a relative symmetric distribution is a basic rule. According to this, the inductors are located symmetrically. The transistors and the resistors are located between inductors to reduce capacitive coupling. According to these rules, each layout block is drawn separately and then put them together. Antenna effect, more formally plasma induced gate oxide damage, is one problem we met during the layout process. For LNA and pre-amplifier, a big inductor needs to connect the gate of the nFET on the input path. The big metal area of inductor leads to the antenna effect. In order to solve this problem, two approached can be applied. First, a reverse connected diode can be applied before the gate to eliminate the excessive charges. Second, a different type of metal can be applied as a transition area before the gate. The final layout is fully DRC and LVS Clean.

TABLE 4
AREA FOR EACH COMPONENT

Components	Area
LNA	700 μm x 1001 μm
Pre-amplifier	2 x 820 μm x 346 μm
Mixer	67 μm x 24 μm
QVCO	2 x 366 μm x 316 μm
Whole	1486 μm x 1001 μm

The area of the entire Wi-Fi receiver is 1486 μm x 1001 μm which is dominated by inductors. The area for each block is shown in Table 4.

TABLE 5
RECEIVER REQUIREMENTS AND SIMULATED RESULTS

Specification	Targeted	Simulated	[2]	[3]	[4]
Process(um)	0.13	0.13	0.6	0.18	0.18
Noise Figure(dB)	<3	1.6	8.3	4.1	3.2
Gain(dB)	>25	50	34	25.1	34.5
Return Loss(dB)	-	-19	-	-24.5	-
P1dB(dBm)	> -20	-18.92	-21	-	-
IIP3(dBm)	> -25	-11	-9	-11.6	-15
Power(mW)	-	55	80	22.7	4.5
Phase Noise(dBc/Hz)	-	123@1MHz	-	-	-

The system level measurement results are shown in Table 5. As shown in Table 5, a good noise performance is achieved for our system. The noise figure is only 1.6dB for the whole receiver. The value of noise figure can be measured in cadence or calculated based on Friss equation. These two values fit very well. However, one limitation of our system is relatively high power consumption which sacrifices for the low noise performance.

V. CONCLUSION

A fully-integrated direct-conversion RF front-end for Wi-Fi application is presented in this paper. Individual components of receiver are designed and simulated with the 0.13μm cmrf8sf model in Cadence including LNA, pre-amplifier, mixer and QVCO. The whole system simulation is performed and compared with proposed specifications. The receiver achieves a low noise figure of 1.6dB and voltage gain of 50dB for the entire receiver. The phase noise for the QVCO is -123dBc/Hz at an offset of 1MHz. The IIP3 for the whole system is -11dBm and P1dB point is -18.92dBm. Overall, the results are satisfactory, except for relatively high power consumption. Trade-offs can be made among gain, noise figure, linearity and power consumption to balance its performance.

ACKNOWLEDGMENT

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