A 402/433 MHz Low Power, Direct Conversion Medical Implant Communication FSK Receiver Front End

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***Abstract*— Rapid advancements in RF technology allow the use of wireless implanted medical systems with the opportunity to improve the quality of life while reducing costs by employing preventive healthcare. The advancement of these systems is supported by the opening of a frequency band specifically for this purpose at 402-405 MHz, commonly referred to as Medical Implant Communication Service (MICS) band. This paper presents a RF-receiver front-end, designed to operate at this band consuming low power while exploiting low frequency and relaxed noise constraints. The front-end features a low noise amplifier (LNA) which feeds into I/Q mixers via a balun. Harmonic mixing with phase shifted signals created by a ring oscillator heavily reduces DC offset caused by LO leakage, while reusing bleed current lowers flicker noise and increases conversion gain. The harmonics along with the desired baseband signal are then separated by active filter stages whose gain can be adjusted using automatic gain control (AGC). The attained Voltage conversion gain is 76.45 dB and the noise figure is 9 dB, with phase sensitivity of -102 dB. This was achieved in a 0.13 µm CMOS process with 1 V power supply. The total power consumption is only 650.91 µW.**

Index Terms— ***MICS, gain, noise figure, power consumption, flicker noise, direct conversion, current bleeding , current reuse, harmonic mixer, self mixing.***

I. INTRODUCTION

With rapid progress in development and integration of radio frequency (RF) architecture on CMOS has opened plethora of options for medical industry. Rapid advancement in RF technology coupled with the opportunity to reduce healthcare cost while improving the quality of life of patients by employing preventive healthcare, has led to the opening of a frequency band at 402-405 MHz [1, 2]. This is commonly referred to as Medical Implant Communication Service (MICS) band. This band, approved by the FCC for use with medical devices, will be utilized by RF-front-ends to communicate short range (≈ 2 m) with medical implants through the human body [1, 2]. The industrial, scientific and medical (ISM) band at 433-434 MHz is more established yet shared with other applications. The need for embedding spurs the need for ultra-low power and small dimension transceivers for wireless communication. These systems should operate for sufficiently long battery lifetime with reduced power consumption, dimensions, low cost, and versatility. Their design highlights the tradeoff between performance, lifetime, cost, and power consumption. Ultra-low power receivers can be realized, provided that some specifications in speed and noise were relaxed. The two main receiver architectures that lend particularly well to themselves for low power applications are direct conversion and low-IF. The requirement of complex image reject filter and the need of port power matching when off chip filters are employed often leads to the decision to use direct conversion architecture for this application, also providing low-power and high-level integration advantages. But direct conversion is plagued by DC- offset and flicker noise. This paper presents a receiver design adjusted to be less affected by these issues, tailored to be operated within the MICS band at low power. Figure **1** illustrates architecture of the designed receiver. Due to use of harmonic mixing, the oscillator signals feeding into the in phase and quadrature (I/Q) mixers are 45° phase shifted instead of 90°.

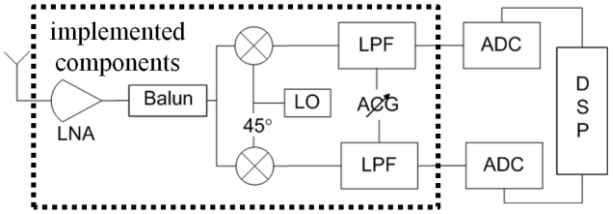

Figure 1 : Receiver architecture. The highlighted parts were implemented.

II. SPECIFICATIONS

The receiver sensitivity can be determined considering the minimum detectable signal level is -91dBm, free space loss in 2m is -30 dB, excess body loss is -10 dB and approximate antenna gain is -35dBi. With a 50-KHz noise bandwidth, for a 10-dB SNR value at the demodulator input, the noise figure requirement of the receiver is:

$$NF = 174 - 10\log BW - SNR + MDS \quad (1)$$
$$= 174 - 47 - 10 - 91 = 26\text{dB}.$$

This is a relaxed requirement and allows the design of a very low-power transceiver. The front-end components such as low-noise amplifier, mixers, and analog amplifiers can be designed to accommodate higher noise and therefore can be designed with less power [1]. The specifications for this receiver are listed in table 1.

Table 1: MICS Specifications [3]

Parameter	**Target Specifications**
Frequency of Operation	402-405/433-434 MHz
Data Rate	20 kbps
Modulation Scheme	Non – coherent FSK, m=0.25
Adjacent channel rejection	50dB
Sensitivity	-110 dBm @ 0.1% BER
Power Consumption	~1mW
Range	~ 2m
Minimum Detectable Signal	-91 dBm
Noise Figure (NF)	26 dB
Technology	0.13 um

III. CIRCUIT REALIZATIONS

For the sake of power savings, all components are designed to operate at a reduced supply voltage of 1V.

A. LNA

The schematic of the LNA is shown in Figure 2.

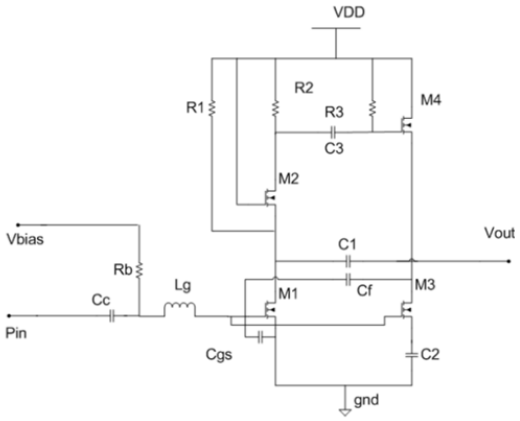

Figure 2: LNA schematic.

The common source topology is selected because it has the best reported noise figure. There is a tradeoff between bandwidth, noise figure, gain performance and power consumption in this topology. In order to improve the noise performance feed forward and thermal noise canceling techniques in LNA design is utilized, where thermal noise from the input stage is sensed and canceled by the noise from the feed-forward network. The LNA with a topology where both capacitive feedback and thermal noise canceling techniques are used is shown in figure 1. The first stage in the feed-forward path in the LNA is a cascode common source amplifier, which includes the common source transistor M1, the cascode transistor M2 and the load resistor R2. The cascode transistor is used to increase the output impedance and the reverse isolation. The second stage is a noise canceling stage. A capacitive feedback network (Cf in Figure 1) is used to control the bandwidth. Capacitor C3 compensates for the parasitic capacitance (at the drain node of M2 and the gate node of M4) and also widens the bandwidth. Resistors R1 and R3 provide DC bias [4]. The input impedance at moderate frequencies is set as

$$Z_{in} = R_f/1 + Av \approx R_f/A_v \qquad (2)$$

Figure 2 explains the mechanism of noise canceling in the circuit. The noise signal due to transistor M1 at node A flows out of the node A through feedback path (where Cf is omitted for simplicity) and common source transistor M3, leading to two opposite-signed noise voltages at the output node B. These two noise signals cancel each other. By carefully designing the circuit parameters, the total output noise is reduced. The cancellation condition is

$$Av_2 = 1 \qquad (3)$$

where, *Av,2* is the gain of the second stage [5].

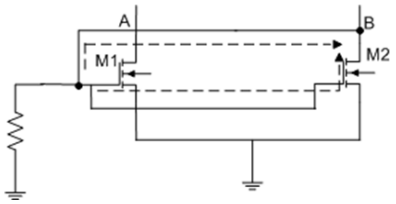

Figure 3 : Noise cancelling mechanism.

B. MIXER

I/Q channels are employed to allow for local oscillator (LO) and RF-input being non-coherent. The mixer operates after the principle of a commutating double balanced Gilbert cell. To allow operation under decreased supply voltage, an active load has been chosen. The load is connected to suppress common mode signals [6]. Direct conversion suffers dc-offset, flicker noise and I/Q mismatch. A dc-offset at the output of typical mixers employed in direct conversion is partially caused by self-mixing. Self-mixing occurs when the local oscillator leaks into the input. It is then mixed with itself and the down converted signal falls into the baseband together with the signal of interest. The offset comprises static and dynamic components, the latter ones are directly affected by the environment and are thus hard to predict and troublesome to cancel. Un-cancelled offsets can saturate following high gain stages [7]. In this design, the commutating frequency is tuned differently to that of the LO, while a higher harmonic of it is created within the mixer. This basically eliminates self-mixing by the root and can be achieved using switches in parallel configuration that are controlled by 180° phase shifted signals, as illustrated in Figure 4. These can be easily created with a ring oscillator. Referring to the frequency of the LO, the phase difference between I and Q channel will then be 45° instead of 90°. Figure 5 shows switch timing for I/Q mixers which holds when the switches are between input and output node. (In an alternative design, switches can be positioned as tail current source. Then other timings have to be chosen).

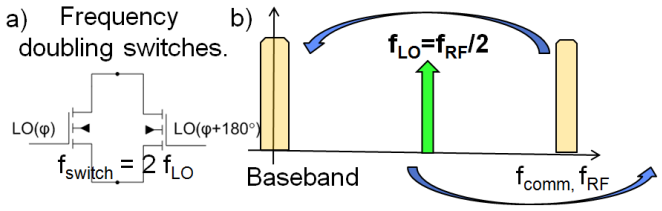

Figure 4 : a) Example of a frequency doubling switch. b) The commutating frequency and the LO frequency differ. Self mixed signals are up-converted and do not fall into the baseband.

Flicker noise dominates at low frequencies; it is desirable to employ designs that are less susceptible to it. Flicker noise generated at the gm stage is up-converted to the commutating frequency and does not appear in the signal band [8]. The load can be either passive or properly sized active. By elimination principle the main contributors of flicker noise are the switches. Two coupled parameters in trade off forbid a straight forward lowering of the noise contribution of the switches as it can be done with the load.

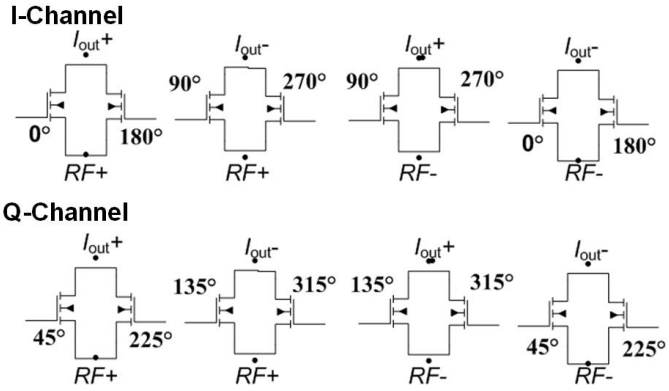

Figure 5 : Switch phase of I and Q channels.

Following equation describes the part of the flicker noise current that is created inside the switches and directly flowing towards the output (4):

$$i_n = \alpha I_S \sqrt{\frac{2 K_f}{A C_{OX} f_{RF}}} \qquad (4)$$

α is a factor taking switching time into account, I_s is the DC bias current, K_f is a process parameter, A is the effective area of the device, C_{OX} is the oxide capacitance density and f_{RF} is the frequency of the input signal. The area of the switches cannot be increased arbitrarily to prevent loading of the LO, and to maintain fast devices. The bias current cannot be decreased arbitrarily when it is shared with the gm stage. Therefore a bleeding transistor shunts off current, allowing to independently control switch and gm stage bias current. Thanks to operation at relatively low frequencies, the current through the load of the mixer can be decreased significantly. When the gate of the bleeding transistor is modulated with the RF input, this current can be reused so that the effective gm is increased significantly. Care has to be taken that a low bias current increases the small signal resistance of the switches seen from the input stage. This can lead to increasing parts of the generated small signal current not flowing to the switching stage [9].

Mismatches between the I and Q channel corrupting phase or amplitude degrade the bit error rate; it is desirable to match those as closely as possible. The transconductors of both channels can be combined. Then they will share process variations and consumed power, Figure 6, [6].

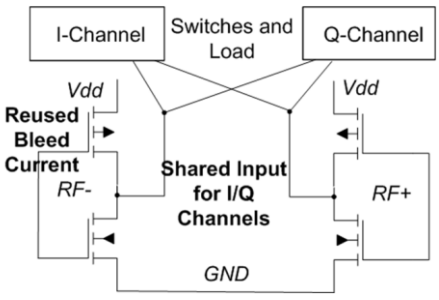

Figure 6 : Current bleeding reduces flicker noise while leaving the gm of the input stage untouched. The current is reused to employ the gm of the bleeding PMOS. I and Q channel share the same input stage.

C. Voltage Controlled Oscillator

The major requirement of our receiver is low power consumption. There are two basic choices available for implementing a VCO- a ring oscillator or an LC oscillator. While an LC oscillator will give a better phase noise performance than a ring oscillator, it has higher power consumption especially with on chip inductors and capacitors. A ring oscillator on the other hand has higher phase noise, however much lower power consumption. Since the noise requirement for our device is relaxed while power requirement is of paramount importance, the ring oscillator topology was chosen.

The delay element for our ring oscillator is based on [10]. They are basically two inverters with latch connected at their outputs. When the input changes state, so does the output after some delay. The outputs of the last delay element are connected to the first delay element. The basic delay element is shown in the figure.

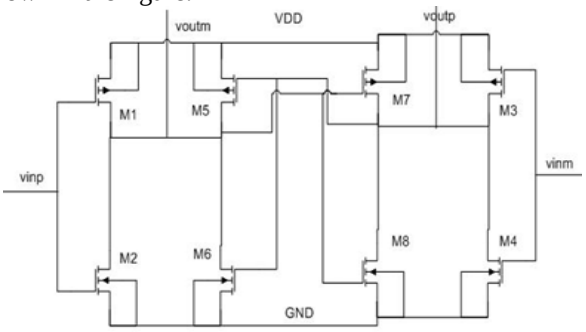

Figure 7 : Differential voltage control oscillator element

Transistors M1, M2 and M3, M4 form the two input inverters that invert the input to the delay cell. M5, M6 and M7, M8 form the latch that is connected across the outputs of the previous inverters. These four inverters combine to provide the necessary delay. Eight of these delay cells are connected back to back with the outputs of the last delay cell inverted over and connected back to the input of the first cell. This gives 180° phase change while the delay elements provide the remaining 180° of phase change, satisfying the oscillation criteria.

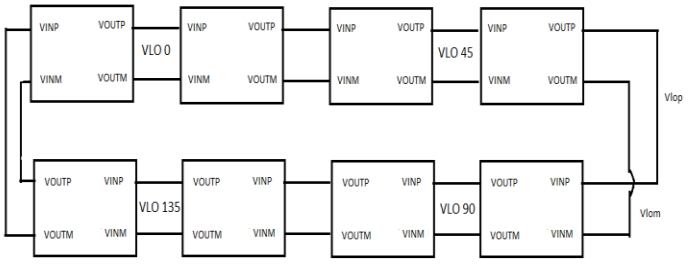

Figure 8 : Schematic of ring oscillator.

D. Low pass filter

The low pass filter is the final stage in our front end design. It is designed to have a passband of around 200 kHz. It is a simple differential input, single ended output amplifier, cascaded with a common source amplifier with diode connected load. A capacitor is connected across the output of each stage providing 40 dB/decade roll off.

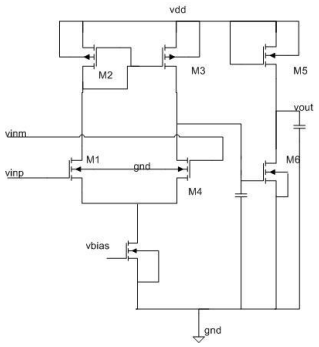

Figure 10: Schematic of differential CS amplifier with diode load.

The power consumption of this stage is around 18µW, I and Q stages for the receiver are needed. The gain is tunable from 0 to 40 dB by changing voltage bias. This allows use in conjunction with an automatic gain control.

V. SIMULATION RESULTS

LNA and balun were simulated connected, all other components were simulated assuming matched conditions, no load and using ideal sources.

A. Simulated Behavior

Figure 9 shows NF, S11 and S21 of the LNA. All parameters are tuned to operate across the designated band.

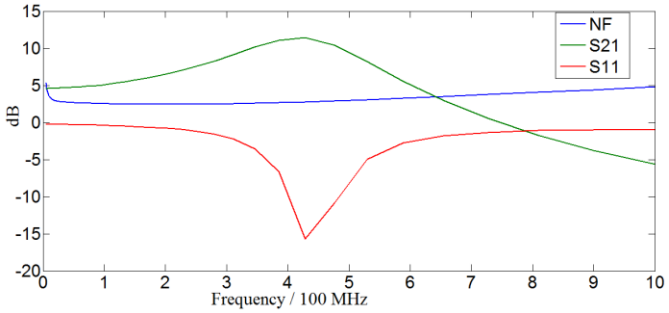

Figure 9: S11, S21 and NF of LNA.

Figure 10 shows that conversion gain is stable over the frequency band of interest. The noise figure at 1 MHz is 17.5 dB.

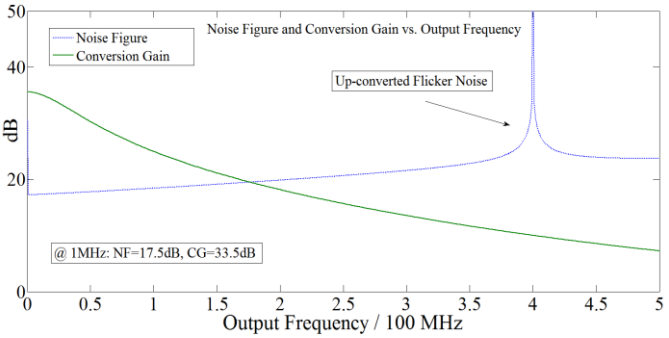

Figure 10: Conversion gain and noise figure of the mixer over 500 MHz frequency range.

Figure 11 illustrates the effect of the bleeding current on noise figure. Flicker noise is effectively lowered by shunting off current after the gain stage before reaching the switches. Even small variations in the current change the corner frequency significantly.

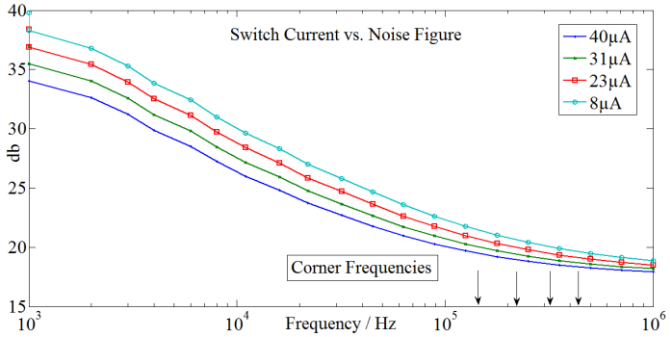

Figure 11 : Noise figure of the mixer with variation in current through the switches, controlled by bleed current.

Figure 12 shows how power can be traded in for noise performance (evaluated at 1 MHz) and gain. The mixer can operate below 50 µW.

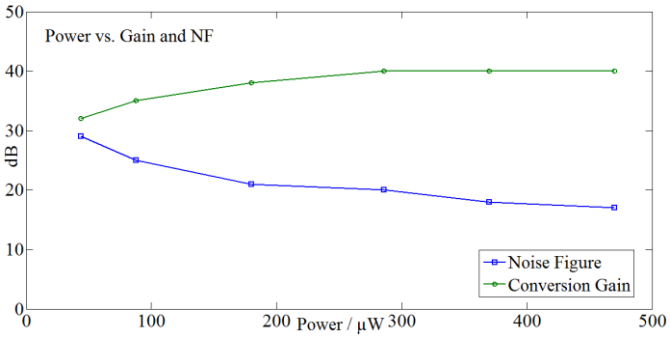

Figure 12 : Trade-off between power, gain and noise figure of the mixer.

The designed VCO has a phase noise of -102 dBc/Hz at 1MHz and a power consumption of 20 µW.

Figure 13 shows high gain of 40 dB, roll off with 40 dB/decade and 200 kHz bandwidth of the filter.

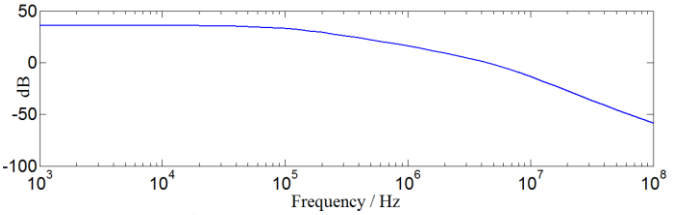

Figure 13 : Low pass filter characteristic

B. *Performance Metrics*

Table 2: Summary of Results

Parameter	Simulated Results
LNA with Balun	
S11 (LNA only)	-10.28 dB
S11	-9.65 dB
S21 (LNA only)	11.22 dB
S21	16.45 dB
NF (LNA only)	2.71 dB
NF	8.03 dB
1 dB Compression Point	-4.829 dB
IIP3	-7.281 dB
Power consumption (LNA)	9.87 µW
Power consumption	44.91 µW

Mixer	
Conversion Gain	23 dB
NF	17.5 dB
Corner frequency	20 KHz
Power consumption (I and Q)	550 µW
VCO	
Phase Noise	-102 dBc/Hz
Power consumption	20 µW
Filter	
Gain	0-40 dB
3db Bandwidth	200 KHz
Power consumption	36 µW

Table 3: Comparison with receiver [10]

Parameter	[10]	This work
Technology	0.18 µm	0.13 µm
Supply	0.7 V	1V
Modulation	FSK	Non – coherent FSK
Image Rejection	>30 dB	NA
Sensitivity	-118 dBc/Hz	-102 dBc/Hz
Data Rate	250 kbps	20-25 kbps
Area	1 mm^2 (Transceiver)	0.987996 mm^2

Table 4: Power consumption comparison with receiver [11]

Component	[11]	This work
LNA	140 µW	44.91 µW (with Balun)
Mixer	49 µW	550 µW
IF Amplifier	70 µW	NA
Demodulator	21 µW	NA
Filter	NA	36 µW
Oscillator	210 µW (LC DCO)	20 µW (ring)
Total	490 µW	650.91 µW

VI. LAYOUT

The full layout is shown in Figure 12. The total area is 0.987996 mm^2.

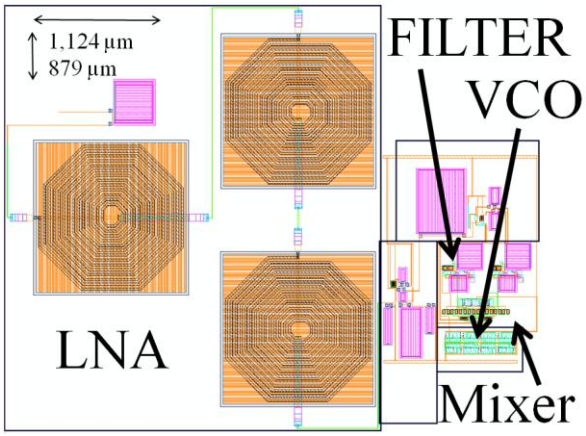

Figure 14 : Layout of the RF front-end.

VII. CONCLUSION

A receiver architecture targeting the MICS band at 402-405 MHz and ISM band at 433-434 MHz has been described. System and circuit level trade-offs, some of which have been discussed, were carefully studied to achieve a fully-integrated, low-power implantable receiver operating at these bands. The circuit blocks of the direct conversion FSK receiver described in this paper being implemented: the proposed ultra-low power LNA, a current bleeding, current reuse I/Q mixer with DC-offset suppression, ring VCO and a low pass filter have been designed and simulated for performance for use in a direct receiver. A voltage conversion gain of 76.45 dB and 9dB noise figure with phase sensitivity of -102dB were attained. This was all achieved in 0.13 µm CMOS with a 1 V power supply while consuming only 650.91 µW power. Further finer optimization would likely lead to some improvements in the results. In continuing this work, the authors would like to investigate expanding the circuit to include transmitter and antenna section in order to develop a complete transceiver.

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