



A 5.2 GHz RF-Front end

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OUTLINE

- *Motivation*
- *IEEE 802.11a Specs*
- *Receiver Architecture*
- *Receiver Design*
- *Overall performance*
- *References*

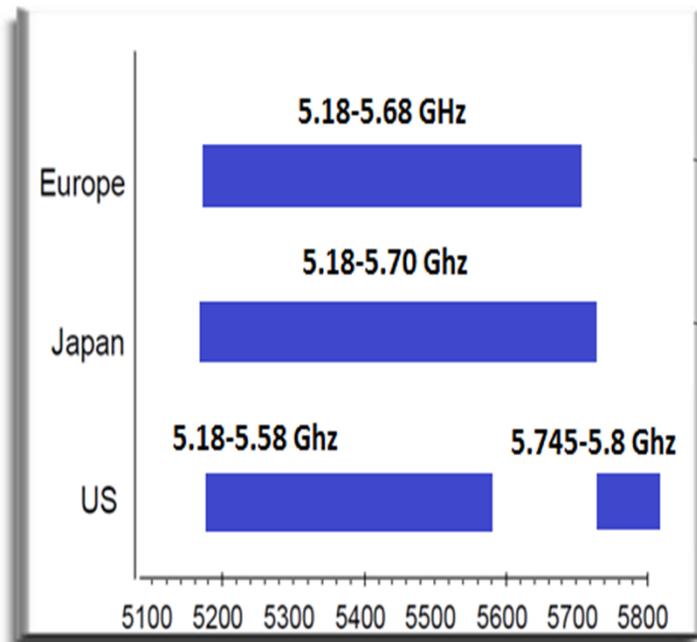
MOTIVATION

- Why the 5-GHz band?
 - ✓ 100s of MHz of unlicensed spectrum available
 - ✓ free from microwave oven radiations
- Application
 - ✓ IEEE 802.11a standard for WLAN
 - ✓ High Performance Radio Local Area Network (HIPERLAN)
 - ✓ For high data rate (upto 54 Mbps), data intensive applications.

IEEE 802.11 A, HIPERLAN

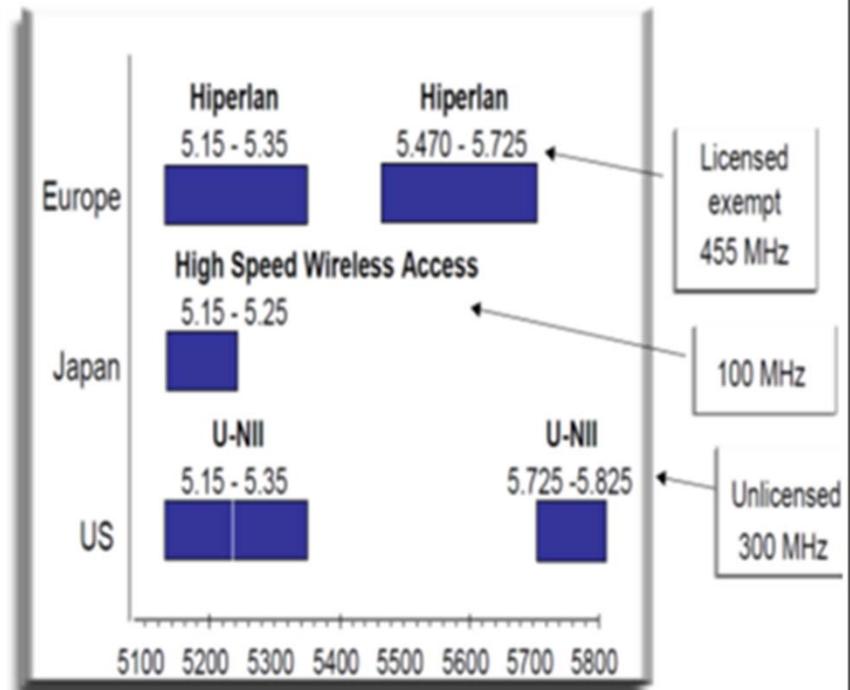
IEEE 802.11a

Spectrum Allocation at 5 GHz

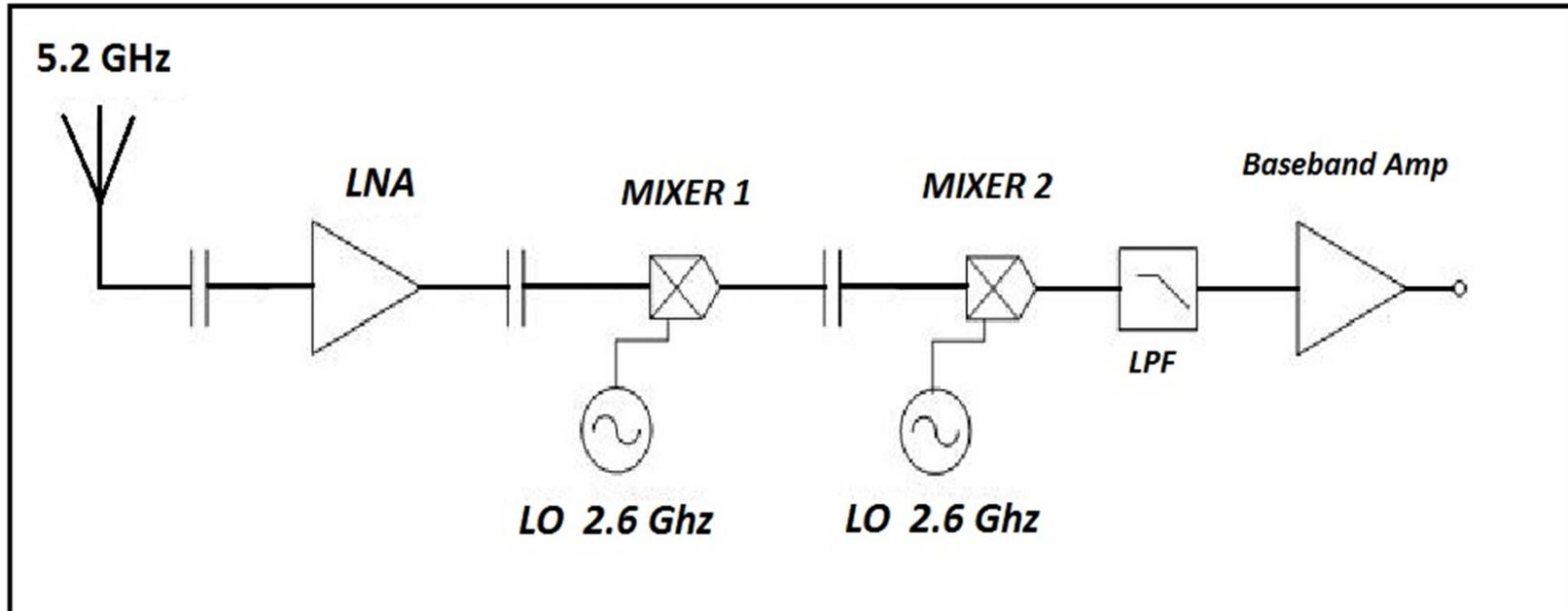


HIPERLAN

Spectrum Allocation at 5 GHz



RECEIVER ARCHITECTURE



- RF 5.2 GHz \rightarrow IF 2.6 GHz \rightarrow Baseband
- A dual conversion heterodyne architecture

RECEIVER ARCHITECTURE

- + Frequency synthesizer (not designed) operates at half the i/p frequency => more accurate phase
- + Image band centered at Zero => high image rejection achieved. No explicit Image reject Filter required
- + In contrast to direct conversion receiver, low LO leakage to antenna
- Flicker noise up converted to the first IF
- LO-IF feedthrough of first mixer may desensitize second mixer
- No channel select filtering between two mixers => high linearity requirement for IF mixer

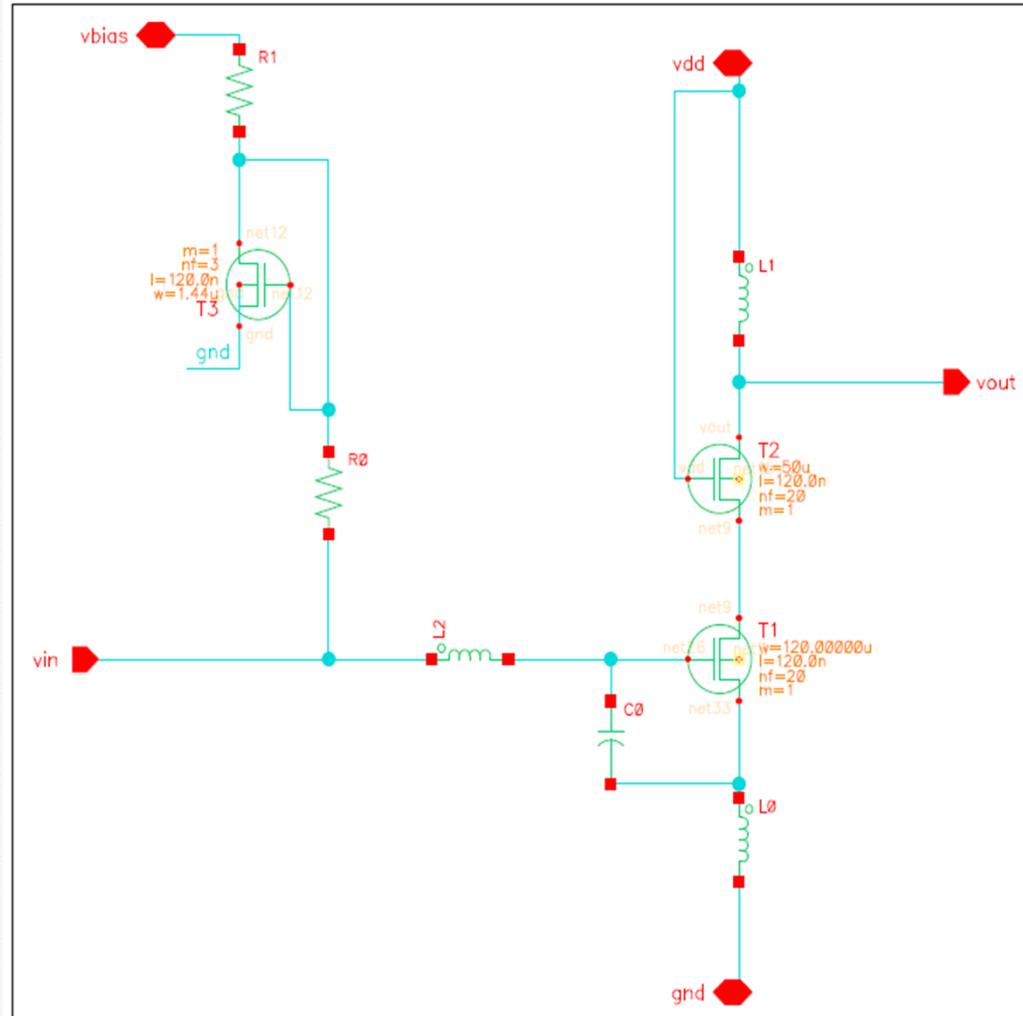
[5]

DESIGN CONSIDERATIONS

- *LNA* : Low Noise Figure(NF), High Gain
- *RF Mixer (Mixer 1)*: Low NF, Low LO-IF feedthrough, High Gain
- *IF Mixer (Mixer 2)*: High linearity, Low NF, Reasonable Gain
- *Base-band Section*: High linearity, Low NF

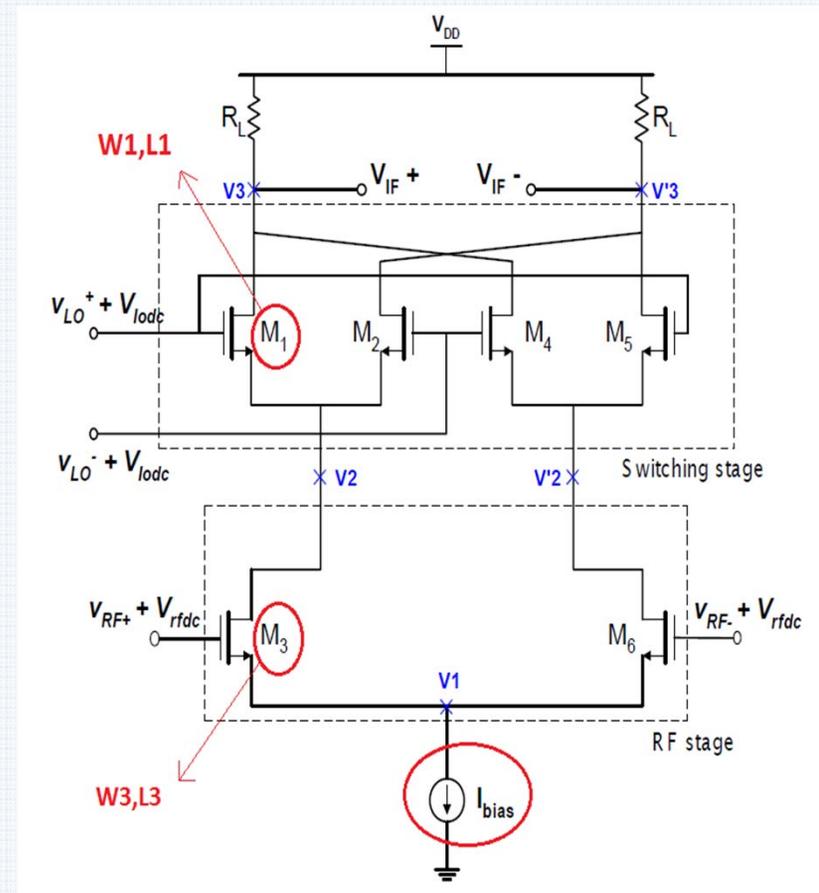
5.2 GHz Cascoded LNA -

LNA Performance	
Gain	29.82 dB
NF	1.58 dB
Power	7.61 mW



RF MIXER DESIGN

- Topology: Double Balanced Gilbert Cell
- Design Variables:
 - *Switching, RF Transistor W, L_s*
 - I_{bias}, R_L
- Initial MATLAB analysis for:
 - *NF, Conversion gain*
 - To choose parameters for optimum performance



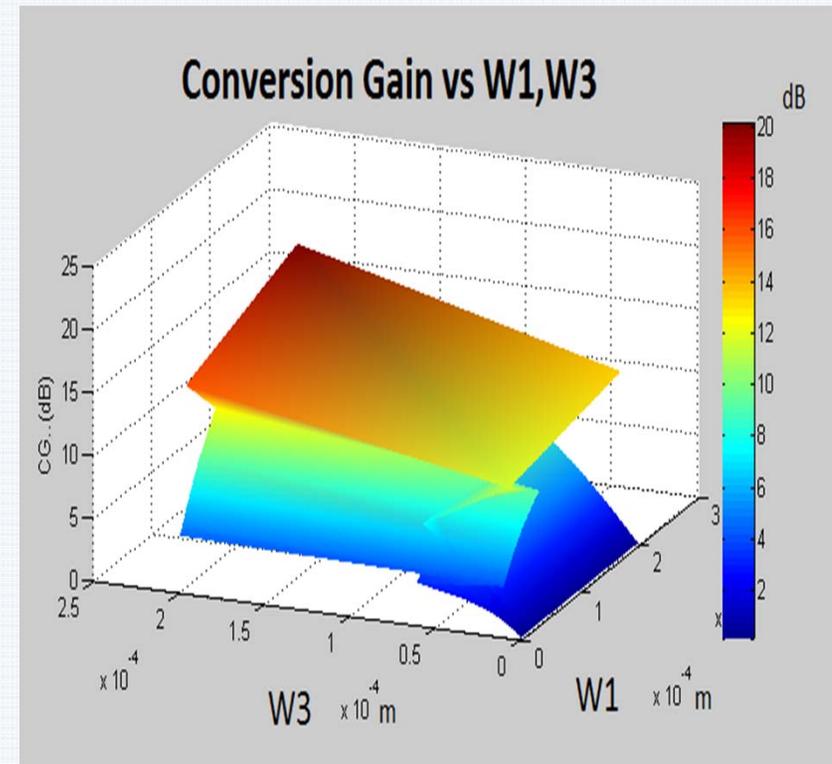
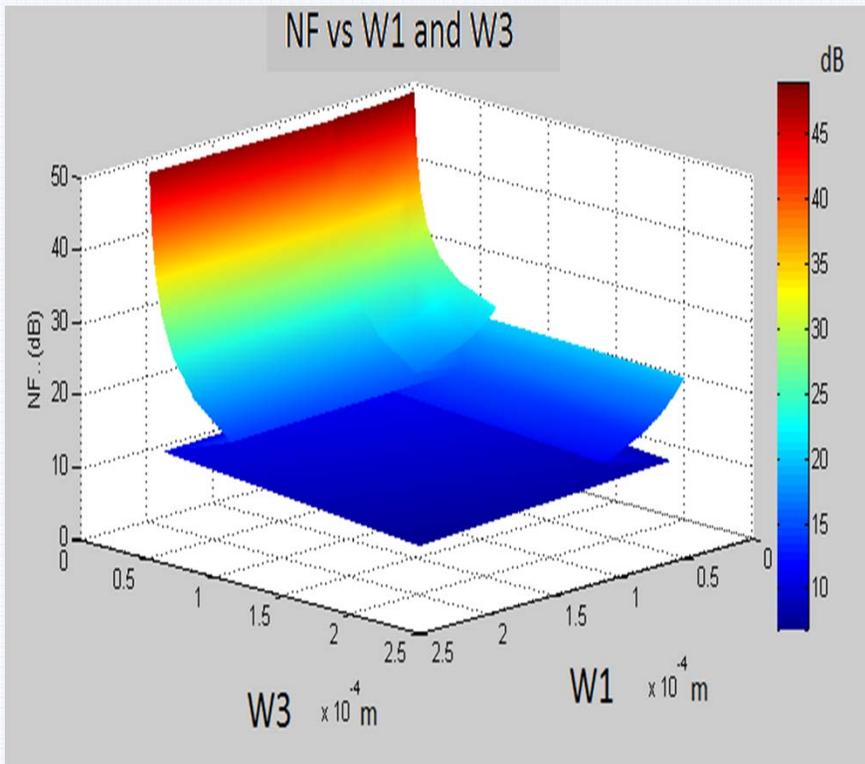
Sample topology

RF MIXER DESIGN : MATLAB

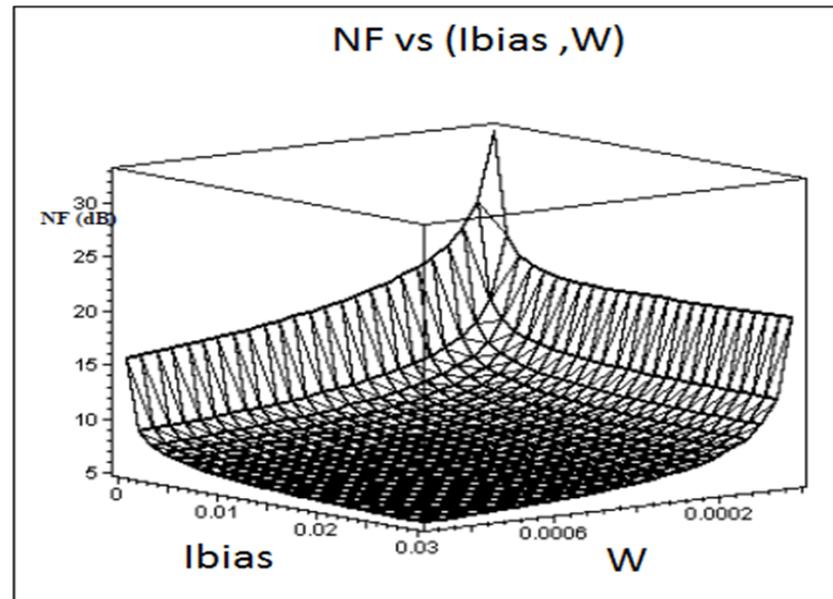
$$NF_{(SSB)} = 10 \cdot \text{LOG} \left[\frac{\alpha}{c^2} + \frac{2(\gamma_3 + r_{g3} \cdot g_{m3}) \alpha \cdot g_{m3} + \gamma_1 \bar{G} + (4r_{g1}) \bar{G}^2 + \left(\frac{1}{R_L}\right)}{R_S \cdot c^2 (g_{m3})^2} \right]$$

$$CG = A_{VRF} \times A_{switch} = -\frac{2}{\pi} g_{m3} \cdot (r_{ds1} // R_L)$$

[6]

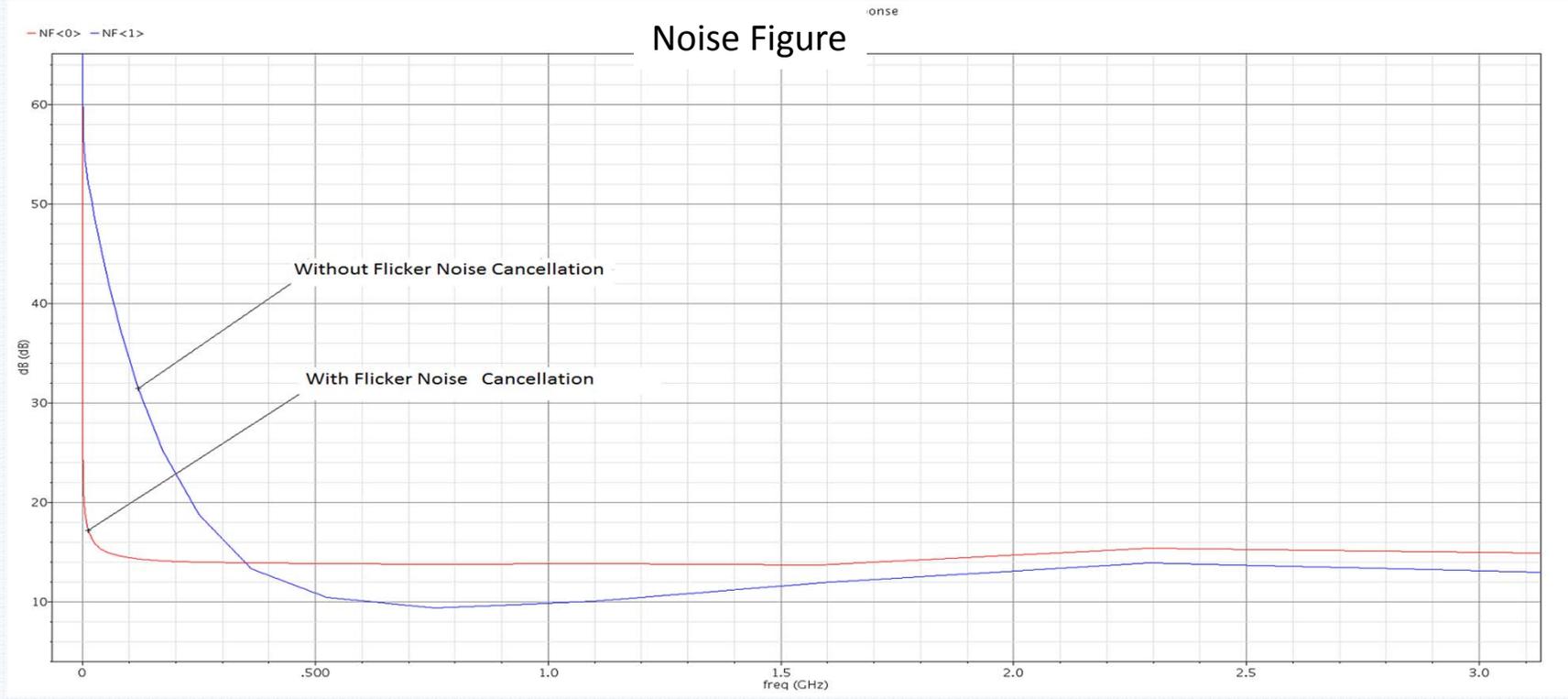
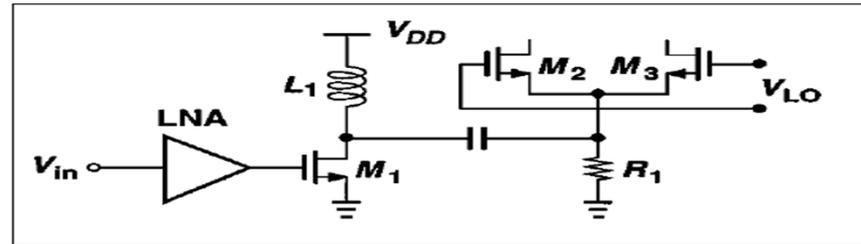


Variation of NF with
Ibias and W:



Ref- S. Douss, F. Touati and M. Loulou," Design Optimization Methodology of CMOS Active Mixers for Multi-Standard Receivers", International Journal of Electrical and Computer Engineering 2:9 2007

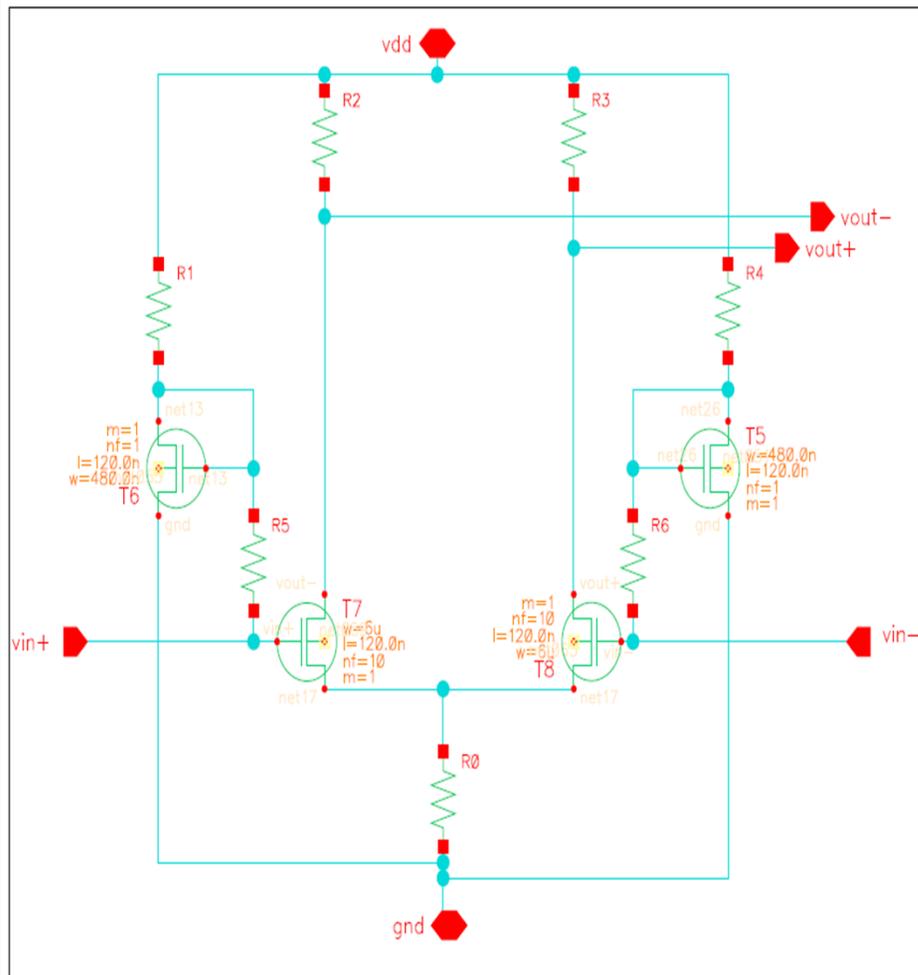
Alternate Topology



IF Mixer Performance and Benchmarking

Parameter	[2]	[3]	[4]	Our Work
Technology (μm)	0.18	0.5	0.25	0.13
Supply Voltage	1.5	2.5	1.8	1.2
Conversion Gain (dB)	3.3	3.35	-2.688	6
P1 dB (dBm)	-8.98	-8.2	5.075	-2.9
IIP3 (dBm)	5.46	2.17	12.81	5.57
Noise Figure(dB)	14.87	9.04	13.678	13.2
Power consumption(mW)	5.6	10	13.3	5.04

BASEBAND SECTION



Topology:
Fully differential amplifier

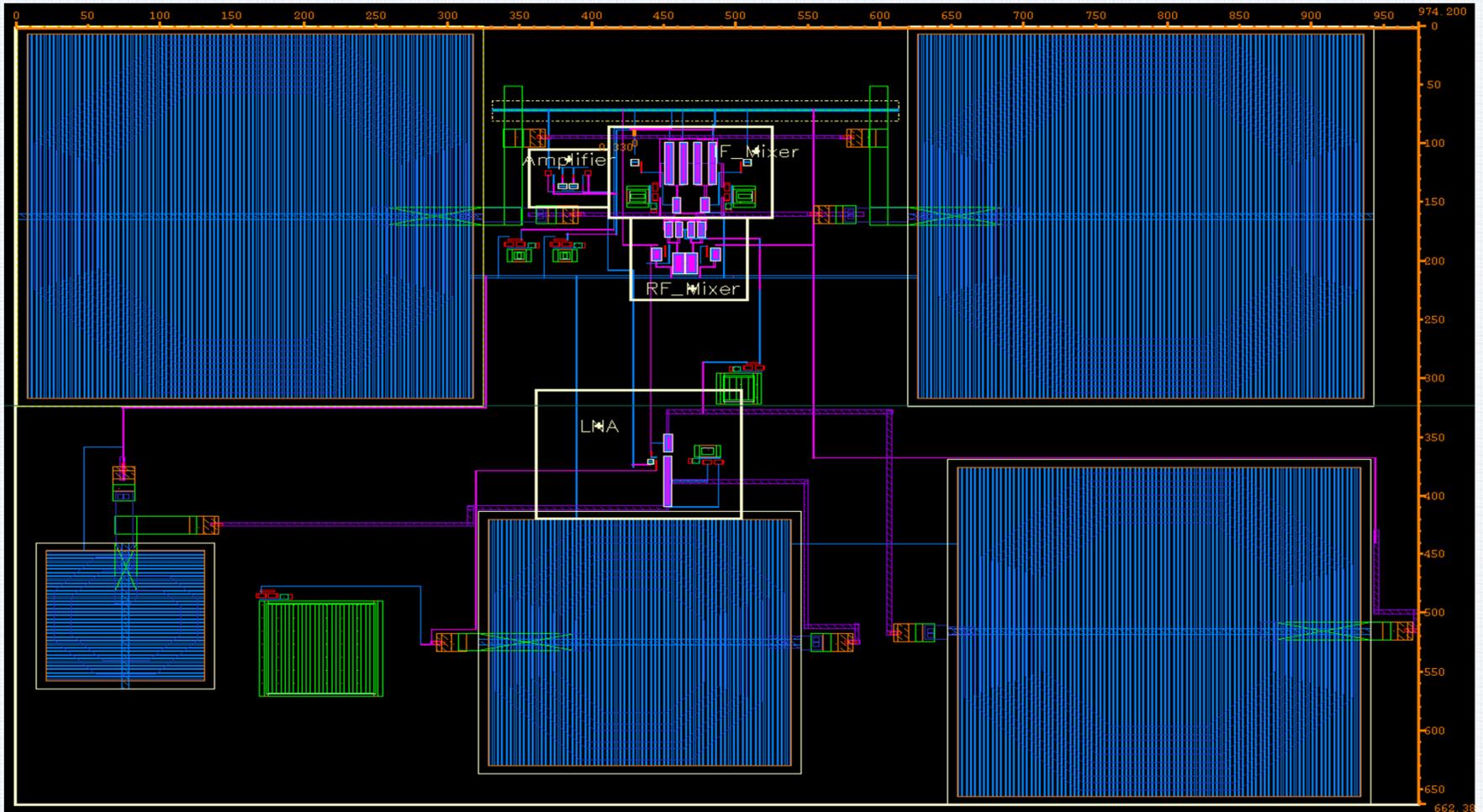
Design Requirements:

- High linearity
- $g_m = 2I_D / (V_{GS} - V_{TH})$
=> tradeoff with gain

Performance	
Gain	3.2 dB
NF	9.2 dB
P1dB	7.54 dBm
Power	0.57 mW

LAYOUT

Area = $0.974 \mu\text{m} \times 0.662 \mu\text{m}$



OVERALL PERFORMANCE

Parameter	[1] Razavi, B.	Our Work
Technology	0.25 μM CMOS	0.13 μM CMOS
Supply Voltage	2.5 V	1.2 V
Center Frequency	5.2 GHz	5.2 GHz
Noise Figure	6.4 dB	9.83 dB
1- dB Compression	-26.5 dBm	-36.5 dBm
Image Rejection	62 dB	57.1 dB
Voltage Gain	43 dB	35.28 dB
Power dissipation		
LNA	8.75 mW	7.61 mW
RF Mixer	5 mW	7.4 mW
IF Mixer	5 mW	5.04 mW
Baseband Section	5.25 mW	570 μW
Total	29 mW	20.62 mW

REFERENCES

- [1] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection", IEEE Journal of Solid-State Circuits, vol. 36, no. 5, pp. 810-815, May 2001
- [2] Hung-Che Wei, Ro-Min Weng, Chih-Lung Hsiao and Kun-Yi Lin, " A 1.5V,2.4Ghz CMOS Mixer With High Linearity", The 2004 IEEE Asia-Pacific Conference Circuit and Systems , Dec 6-9, 2004
- [3] H.Kilicaslan, H.S Kim, and M.Ismail , "A 1.9Ghz CMOS down-conversion mixer ",Proc. 40th Midwest Symp. Circuit System, vol2 pp.1172-1174, 1998
- [4]Kumar Munusamy and Zubaida Yusoff , " A Highly Linear CMOS Down Conversion Double Balanced Mixer", ICSE2006 Proc. 2006, Kuala Lumpur, Malaysia
- [5] B. Razavi, " Design Considerations for Direct-Conversion Receivers IEEE Transactions On Circuits and Systems—II: Analog And Digital Signal Processing, vol. 44, no.6, June 1997
- [6] S. Douss, F. Touati and M. Loulou," Design Optimization Methodology of CMOS Active Mixers for Multi-Standard Receivers", International Journal of Electrical and Computer Engineering 2:9 2007



**THANKS TO PROF. MICHAEL P. FLYNN AND
PROF. DAVID WENTZLOFF**

QUESTIONS?