

A Current Re-use Quadrature Front End Receiver for ISM Band

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Abstract — This paper presents a current re-use quadrature front end receiver architecture for ISM Band. The proposed architecture is a stacked QLMV cell which consists of a low-noise amplifier (LNA), mixer and voltage-controlled oscillator (VCO), which feeds into the intermediate frequency (IF) load. The LNA is a common source amplifier with L_s source degeneration, a double-balanced Gilbert cell mixer and a parallel VCO. Two IF load architectures are presented in this paper, IF_1 and IF_2. IF_1 is a basic transimpedance amplifier and IF_2 is a complex transimpedance amplifier with output buffering. This design was implemented in 0.13 μ m CMOS technology and the results obtained show a S_{11} of -18.51 dB, P_{1dB} of -41.5 dBm, VCO phase noise of -116 dBc/Hz @ 1MHz and a noise figure of 12 dB with the differential amplifier based TIA (IF_2) and 9.8 dB with the output buffered differential amplifier IF load (IF_1) and has an overall power dissipation of 2.16mW.

Index Terms— LNA, mixer, VCO, noise figure, IF, amplifier, RF, Transimpedance Amplifier (TIA).

I. INTRODUCTION

THIS paper presents a current re-use architecture for a radio-frequency (RF) front-end receiver for ISM band. There is a steadily growing demand for ISM band based applications. Although the ISM band has not been relatively utilized compared to GSM or Wi-Fi in mainstream commercial applications, it is however growing due to emergence of wireless sensor networks, ZigBee devices and cordless phones. The FCC made unlicensed spread spectrum in ISM bands available on May 1985 and all devices using this band must pass the interference limits allowed by the FCC. The ISM band employs binary phase shift keying (BPSK) mechanism for signal transmission and reception.

Recently, there has been a great deal of interest for low power and low cost integrated receivers and as technology scales, more emphasis is placed towards minimizing the use of external components. Current devices typically have high energy consumption and this limits the battery life of these devices and for applications such as wireless sensor nodes especially in environmental monitoring situations require long battery life and thus need to have low power consumption and an optimized link budget for communication purposes. This has led to the development of stacked current re-use architecture which has multiple RF circuits sharing the same DC bias current, laid on top of each other as shown in Fig. 1.

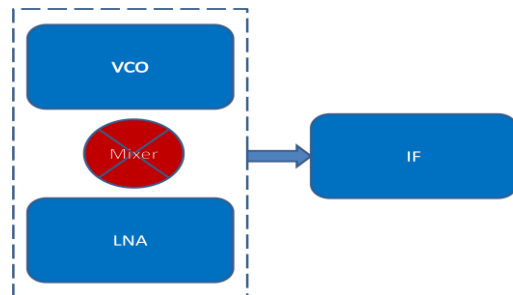


Fig. 1. Stacked Quadrature LNA, mixer, VCO Cell

The conventional receiver front end architecture consists of a cascaded structure of the low-noise amplifier (LNA), mixer and the voltage-controlled oscillator (VCO). Input signal from the antenna is fed directly into the LNA, and if the LNA is a differential structure, a balun is used to convert the single-ended input to a differential ended input. The output of the LNA is fed into the mixer and two mixers are used to perform in-phase (I) and quadrature phase (Q) signal demodulation with an output local oscillator (LO) frequency of the VCO. The output of the demodulation is then supplied to the IF load for bandpass modulation and then the back end chain consisting of an analog to digital converter (ADC) followed by digital baseband processing. The conventional front-end is shown in the Fig. 2.

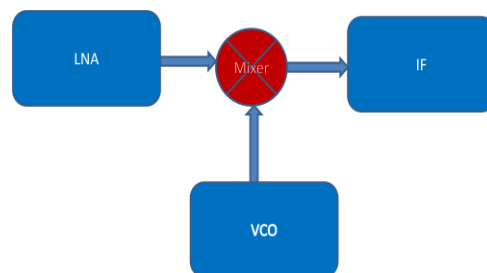


Fig. 2. Conventional RF Front-End Architecture

Section II discusses the proposed current re-use architecture delving into LNA, mixer, VCO and IF loads in detail. Section III discusses the simulation results for two types of IF loads, IF_1 (basic transimpedance load) and IF_2 (output-buffered transimpedance differential amplifier load). Section IV shows the layout, Section V discusses future work and Section VI summarizes our work.

II. ARCHITECTURE

The transistor level low power, vertically stacked Quadrature LNA, mixer, VCO (QLMV) cell is shown in Fig. 3. Instead of the gate-modulated QVCO proposed by [1], a parallel QVCO is used for this particular application due to the increased phase noise and less frequency pulling of the gate-modulated QVCO. This will be discussed in the section below in more detail.

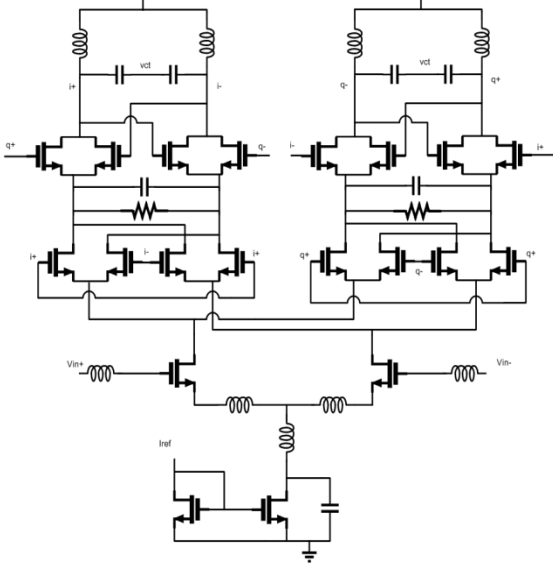


Fig. 3. Transistor-Level Stacked QLMV Cell

A. Low Noise Amplifier (LNA)

The LNA used in the QLMV cell is a common-source inductor degeneration topology. The circuit level implementation is given below in Fig 4 below:

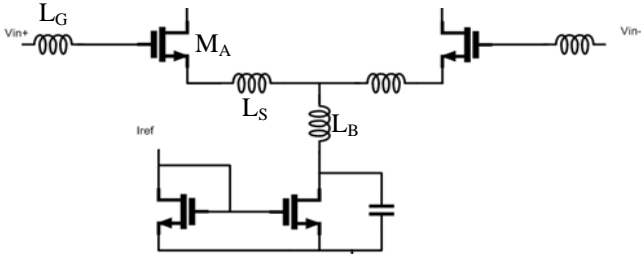


Fig. 4. Common-Source Degenerated LNA

The input impedance, Z_{in} of the matching network seen by the RF input signal can be derived as in (1).

$$Z_{IN} = \frac{g_{mA}L_S}{C_{gsA}} + j(\omega(L_G + L_S) - \frac{1}{\omega C_{gsA}}) \quad (1)$$

The L_B inductor is used decouple the QLMV, making it an open circuit at high frequencies. The tail current for the QLMV cell is generated by using current mirrors based on an I_{REF} of 1.8mA. The LNA, when individually characterized has a noise figure of 2.1dB. The S_{11} , which represents the effective of input matching, is -18.51dB @ 900MHz, which meets the specifications. The quality factor of input impedance network is derived as in (2).

$$Q_{IN} = \frac{\omega_0(L_G + L_S)}{2R_S}, \quad \omega_0 = \frac{1}{\sqrt{(L_G + L_S)C_{gsA}}} \quad (2)$$

Whereby C_{gsA} and g_{mA} are the parasitic gate to source capacitance and transconductance of the nfet of LNA, M_A . The effective transconductance of the LNA stage for the gain can be derived as follows

$$G_{m,LNA} = \frac{\omega_T}{2\omega_0 R_S}, \quad (3)$$

where ω_T is the cut-off frequency and R_S for the design is 50Ω. Simulation results for S_{11} and noise figure are discussed more in detail in Section III.

B. Voltage Controlled Oscillator (VCO)

Good phase noise, frequency tuning, low power and good amplitude swing are some desired features for a VCO for RF front-end applications. For sinusoidal waveforms, LC oscillators are the preferred topology. A PLL control is usually given for precise frequency tracking using a good frequency reference.

Quadrature demodulation is used mainly for image rejection. LC oscillator based quadrature demodulation was first suggested in [8]. It was based on anti-phase injection of phase from two LC based oscillators into each other, so that at steady conditions, there will be a stable state of operation when they are 90° phase shifted. Various topologies have emerged presenting trade-offs between them [8].

The originally proposed scheme in [8] is known as Parallel QVCO (P-QVCO) since the phase injection transistors appear in parallel with the main negative impedance transistors. The variants that emerged later-on were Series QVCO (S-QVCO) and Gate-modulated QVCO (GM-QVCO) shown in Fig. 5. The S-QVCO had good phase noise characteristics [9] but was not desirable for use in the current re-use architecture for the lack of headroom. The current re-use architecture used in [1] had claimed a better phase noise characteristic over the S-QVCO and P-QVCO topologies [1]. So both P-QVCO and GM-QVCO structures were tested for this work.

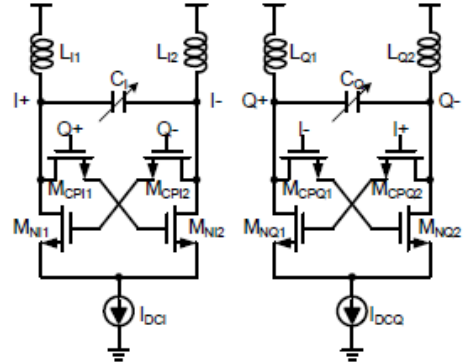


Fig. 5. Gate modulated QVCO proposed by [1]

For proper anti-phase injection mechanism to work, the gate-modulated injection transistors have to be sized big. This added a lot of parasitic capacitance at the VCO output node. This parasitic capacitance caused a lot of frequency pulling

and is not desirable. In P-QVCO, this concern is not seen. A sizing ratio of $\alpha = W_{inj}/W_{gm} = 0.2$ to 0.5 was found to give sufficient phase injection and less phase noise (W_{inj} - width of injection nfet and W_{gm} - width of gm stage. A value of $\alpha = 1/3$ was chosen here which gave a good balance between phase noise (VCO alone -120dBc/Hz @ 1MHz) and noise figure for the entire circuit. The final phase noise after integration in the current-reuse stack was seen to degrade a little bit to -116dBc/Hz @ 1MHz offset. This figure is seen to be better than the GM-QVCO implemented in [1] which had a figure of -110dBc/Hz @ 1MHz offset.

The ISM band sits at 915 MHz and the entire frequency spectrum ranges from $902\text{ MHz} - 926\text{ MHz}$. Since the Intermediate frequency is 10MHz , the VCO is centered at 925MHz . The varactor voltage control (vct) as shown in Fig. 6, steers the frequency from $912\text{ MHz} - 935\text{ MHz}$.

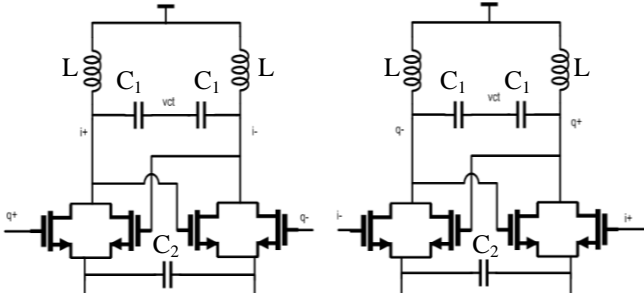


Fig. 6. Parallel QVCO

A capacitance is put across the VCO output as in Fig. 6. It improves the Q-factor of the LC tank without the need for increasing current or reducing the series loss of the inductor. This capacitor also increases the voltage swing at the VCO output. If this capacitor is kept sufficiently high ($\sim 2\text{pF}$), it helps to bypass the VCO output from going to the Intermediate Frequency (IF) stage. The amplitude at the VCO output was measured as $\pm 270\text{mV}$ centered at the VDD voltage. Since the varactors used in the circuit could not be easily characterized, measurements were done on circuit to get an exact match for the desired frequency by varying the vct voltage. The VCO frequency is given by (4).

$$f_{vco} = \frac{1}{2\pi\sqrt{L(C_1 - 2C_2)}} \quad (4)$$

C. Mixer

The VCO output and the amplified RF output from the LNA should be mathematically multiplied to get the sum and difference frequencies. For IF based down-conversion, the RF and VCO frequency are exactly IF frequency apart so that the down conversion will produce the difference frequency at the IF frequency (here 10 MHz). For direct down conversion to base band, the VCO frequency is kept exactly the same as the RF. The multiplication output will should be band pass or low pass filtered to reject the higher frequencies. Usually the IF and VCO frequencies are kept at least 2 decades apart in the frequency spectrum. This reduces the burden on the further filtering stages. A low power and lower order filter can do the

job.

The most popular mixing scheme for RF front end applications is the Gilbert Cell mixer. For the current re-use architecture used here, a doubly balanced mixer is used [1]. The doubly balanced architecture has the advantage of removing the DC bias current from the differential output as shown in Fig. 7. The conversion gain on the differential output of the mixer is $4/\pi$ and the 2^{nd} harmonics are removed.

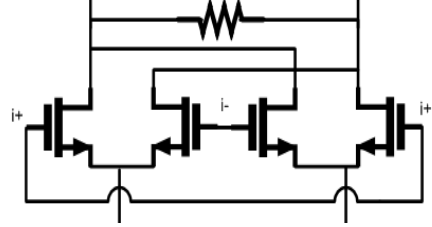


Fig. 7. Double-balanced Gilbert Cell Mixer

The transistors in the mixer were biased in triode mode. The VCO output has a DC bias of VDD and extra circuitry will be needed to bias these transistors in saturation mode. Extra transistors add noise in the circuit which is not desirable. The mixer being a non-linear device does not stay in saturation mode while is operation. So leaving them at triode region is tolerable.

D. IF Amplifier

Fig. 8 shows the IF amplifier which was designed to provide low input impedance to the RF front end. Such that majority of the IF current after mixing passes through the IF stage rather than the cross coupled LC VCO as represented in (5).

$$I_{IF} = I_{MIX} \frac{g_{mIF}}{g_{mVCO} + g_{mIF}} \quad (5)$$

Hence, the transconductance of the IF amplifier (g_{mIF}) should be high. Another key point to understand is that the I_{out+} and I_{out-} node are near VDD (approx. $VDD - VGS$). Hence this makes IF amplifier difficult to design. To address that in this paper, common drain amplifier has been designed to level shift the DC voltage, which is then fed to PMOS differential amplifier with resistor as load that provides the gain A. Followed by source follower to provide feedback to the input. This entire loop provides gain of total effective transconductance (G_m).

$$G_{mIF} = g_{mIF} (1 + A) \quad (6)$$

$$A = g_m R \quad (7)$$

Voltage gain can be obtained as follows:

$$V_{out} = I_{IF} \times (r_o // g_m r_{o2}) \quad (8)$$

An advantage of this IF amplifier is that there is flexibility to provide 2 poles before LO frequency. One at output node (9) and other one at differential amplifier's output (10). At the same time the feedback can remain stable. As differential amplifier output forms a major pole for the system in feedback whereas source amplifier compensates itself with pole and zero cancellation.

$$f_1 = \frac{1}{2\pi C_{out} (r_o \parallel g_{m_{r_{o2}}})} \quad (9)$$

$$f_2 = \frac{1}{2\pi C_{diff} R} \quad (10)$$

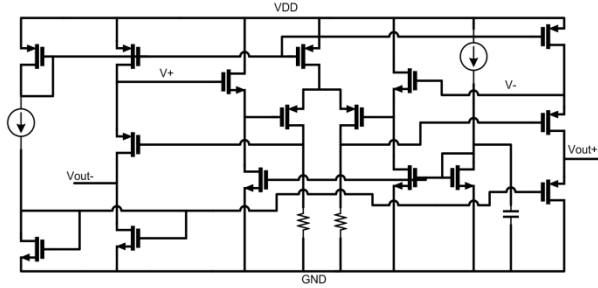


Fig. 8. IF_2, Novel transimpedance amplifier based IF load

The novel transimpedance amplifier is shown above in Fig. 8. This circuit introduces a lot of thermal noise and consumes considerable power. Hence a basic transimpedance amplifier is used as shown in Fig. 9. Its input impedance is given by (11).

$$R_{in} = \frac{R}{1+A} \quad (11)$$

$$A = g_m \left(\frac{r_o}{2} \right) \quad (12)$$

The total gain of this TIA is given by A_v in (13). This architecture is relatively simple to design but has 1 dominant pole. Hence, this can give a maximum 20 dB/dec roll off after the IF frequency. The advantage of this amplifier is that it has lesser number of transistors and thus contributes less noise.

$$A_v = I_{in} R \quad (13)$$

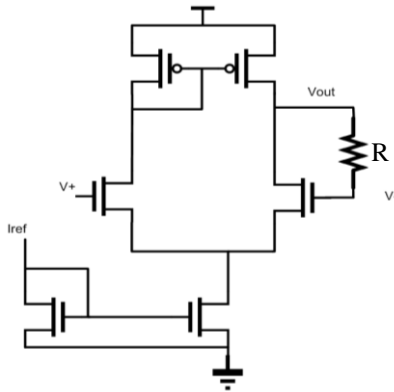


Fig. 9. IF_1, Basic transimpedance amplifier with resistive feedback

III. MEASUREMENT RESULTS

Some important parameters of the RF receiver are detailed below. Others are directly compared with the reference works.

A. S_{11} parameter

The S_{11} of the LNA was measured to be less than -10dB for input RF frequency of 830-990MHz. Fig. 10 shows the S_{11} plot

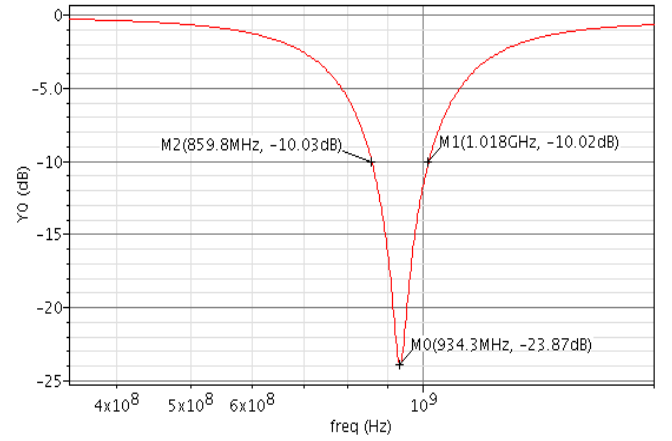


Fig. 10: S_{11} Plot

B. VCO Phase Noise

The VCO by itself gave a phase noise of -120dBc/Hz @ 1MHz as shown in Fig. 11. With the QLMV cell the phase noise reduced to -116dBc/Hz. This figure is better than -110dBc/Hz obtained in [1] even though it used the GM-QVCO which was proposed to give better phase noise.

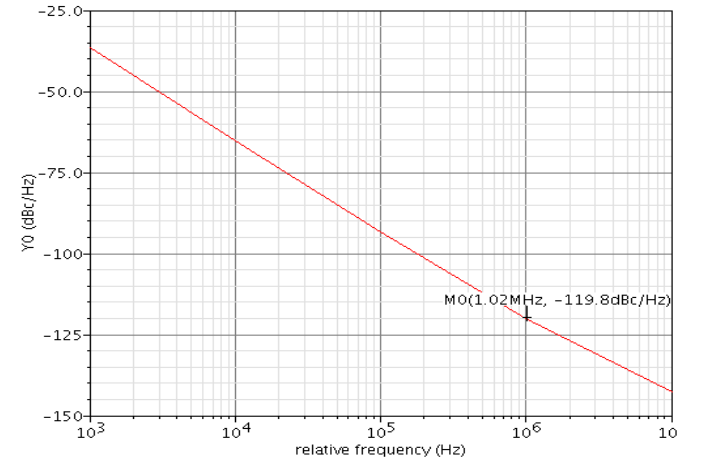


Fig. 11: VCO Phase Noise

C. VCO Frequency Tuning

The VCO frequency was also plotted against the control voltage. As can be seen from Fig. 12, the variation in frequency covers the entire ISM band with some additional swing provided to account for the process and temperature variations.

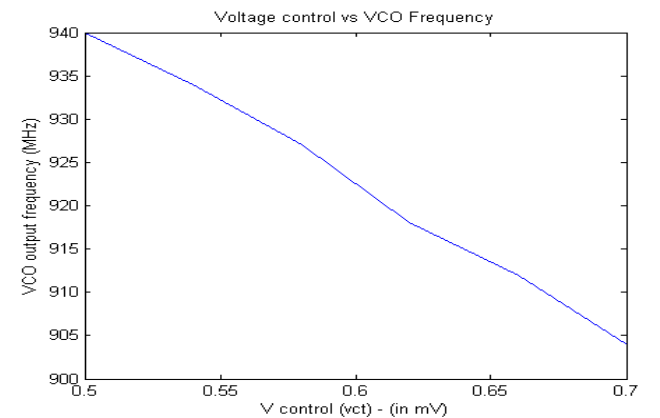


Fig. 12: VCO Frequency Tuning

D. Input Referred 1dB Compression Point (P_{1dB})

The P_{1dB} plot is shown in Fig. 13. The P_{1dB} obtained is -41dB which is comparable to the reference [1]. This plot also shows a linear conversion gain of 46dB till the P_{1dB} point.

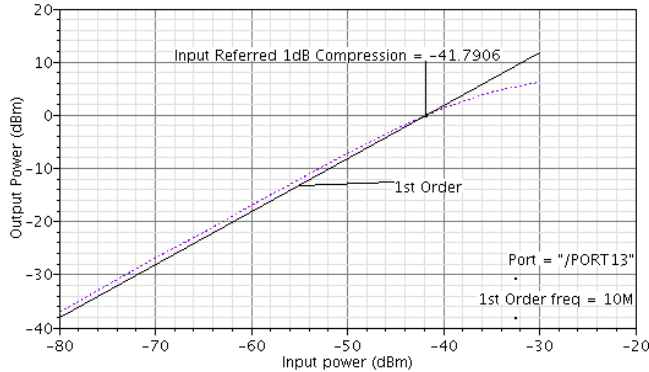


Fig. 13: Input-referred 1dB compression point

E. Noise Figure

Noise figure (NF) measured for the circuit with IF_1 and IF_2. The former gave a good overall NF of 9.8dB and the latter gave 12dB.

F. Performance Table

Table 1 shows the performance of our QLMV cell with IF_1 and IF_2 loads with respect to [1].

TABLE 1: PERFORMANCE TABLE

	QLMV (IF_1)	QLMV (IF_2)	[1] GPS Rx
S_{11} (dB)	< -10	< -10	< -10
IIP3 (dBm)	-21.5	-55	-30
P_{1dB} (dBm)	-41.5	-65	-40
Conversion gain (dB)	46	42	42.5
Noise Figure (dB)	9.8	12	6.5
VCO Phase Noise (dBc/Hz) @1 Mhz	-116	-116	-110
VDD (V)	1.2	1.2	1
Current QLMV (mA)	1.8	1.8	1
Current IF Amp (mA)	1	1.8	1

IV. LAYOUT

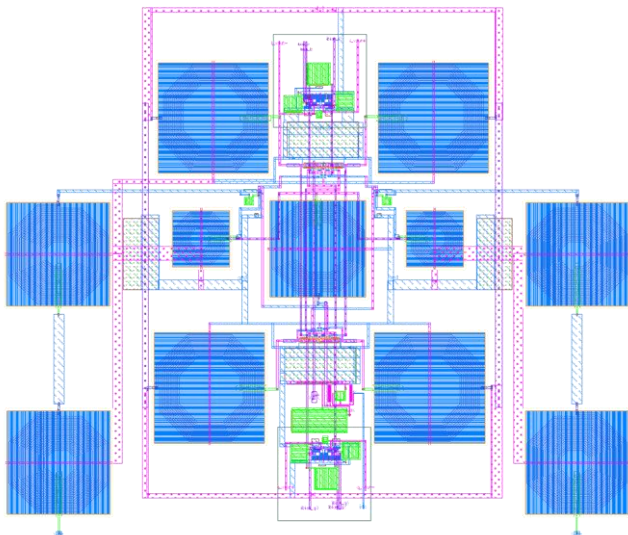


Fig. 14. Layout

The layout is shown in Fig. 14. The die area is 2.5mm^2 . All blocks and signal paths have been laid out symmetrically to reduce mismatch.

V. FUTURE WORK

As this architecture uses I and Q demodulation, we can use polyphase filters to provide a 90° phase shift which can be cascaded with the I path to do image rejection. As we designed our VCO tuning voltage range to be between 500mV-700mV, a phase locked loop (PLL) can be implemented to control the VCO frequency. To make a complete RF front end system, an ADC can be attached to the output of IF load which can feed directly to a digital signal processor (DSP) for baseband processing.

VI. CONCLUSION

In this paper, we have presented a current re-use front end architecture for ISM band. The proposed QLMV cell consists of a LNA, mixer and VCO in a cascode with the output being fed to the IF load. We also presented two different transimpedance amplifiers which behave as IF loads, namely IF_1 (basic differential amplifier) and IF_2 (current-feedback based differential amplifier). IF_1 amplifier consumes $300\mu\text{W}$ per cell and IF_2 consumes 1mW per cell. Overall noise figure due to IF_1 is 9.8dB and due to IF_2 is 12dB. Simulation results obtained were comparable to [1].

VII. ACKNOWLEDGEMENT

We wish to thank Prof. David Wentzloff and Prof. Michael Flynn for their advice and thoughtful suggestions.

VIII. REFERENCES

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