EECS 570

Midterm Review

Parallel Computer Arch

Intel Paragon XP/S

Winter 2025

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http://www.eecs.umich.edu/courses/eecs570/

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1: Intro

- ILP Wall
- Power Wall
- Dennard Scaling / Post-Dennard Scaling
- Motivating Multiprocessors

2: Models and MPI

- Complexity analysis
  - Work & Depth
  - Critical Path
- Scheduling
  - Greedy scheduler
- Ahmdahl's Law
- Message Passing
  - Asynchronus vs Synchronus
  - Deadlock

3: Shared Memory + DLP

- Global address space
- Virtual addressing
- Synchronization
  - Locks
  - Barriers
- Bus based interconnect
- Point-to-point interconnects

- Vector Processing

4: Synchronization

- Aquire/Wait/Obtain
- Locks
  - Need atomic operations for Read-Modify-Write
    - Test&set
    - Fetch&op
    - Swap
    - Compare&swap
  - Test and Set Spin
  - Test and Test and Set Spin
  - Ticket Locks
  - Array Based Queue Locks
  - MCS Lock
- Barriers
  - Sense reversing barrier
  - Tree-Based

5: Transactional Memory

- Insert, lookup, delete -> transfer
- Fine grained locking – difficult to program
- Coarse grained locking – too slow
- Create TM (Read set, Write set)
- Version management (Eager or Lazy)
- Conflict Detetction (Eager or Lazy)

- Where does TM not work at replacing locks

6: Snooping

- Single Reader Multiple Writer – or – Data value invariant
- Caches snoop all requests on single bus
- Make decisions about cacheline state
- Valid – Invalid
- M – O – E –S –I
- Update vs. Invalidate protocols

7: SMP Designs

- Coherence Control Implementation
- Writebacks, non-atomicity, serialization/order
- Hierarchical caches
- Split Busses
- Deadlock, livelock & starvation
- TLB Coherence

8: Directory Protocols

- Snooping has bus bandwidth and snooping bandwidth problems
- Make a NoC, and add directory protocol
- Centralized vs Distributed
- Share list options
  - Bit vector, pointers, linked-lists, coarse vectors
- 4-hop vs 3-hop transactions
- Use of Ack's
- Race conditions
- Bounding messages

9: Memory Consistency Models

- Type of consistency models
  - Sequential consistency
  - TSO
  - Relaxed consistency
- Language-level vs hardware-level consistency models
- Data-race-free memory model
- Speculative hardware optimizations for memory-ordering overhead
  - In-window speculation
  - Out-of-window speculation
  - Type-based (local vs shared) optimization
- SC-preserving compiler