On the Rules of Low-Power Design

(and Why You Should Break Them)

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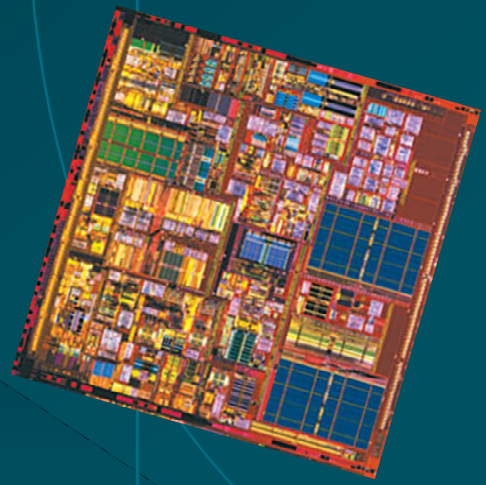
A long time ago, in a not so far away place…



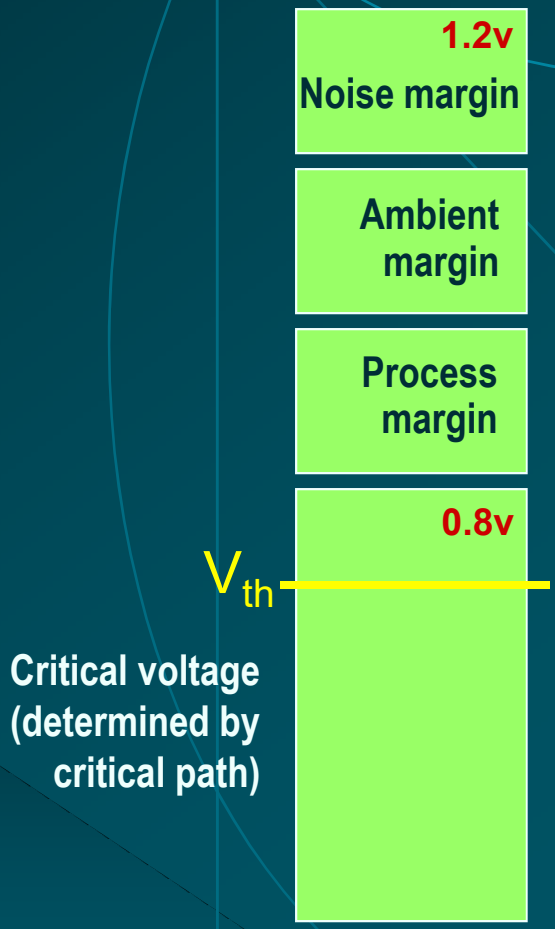
The "Rules" of Low-Power Design

$$P = aCV^2f + VI_{leak}$$

1. Minimize switching activity
2. Design for lower load capacitance
3. Reduce frequency
4. Reduce leakage

and the most important of all:

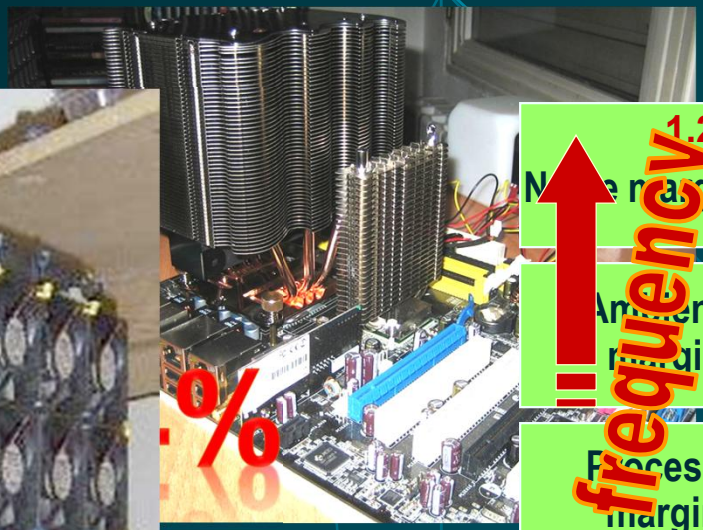
5. *Decrease supply voltage!*

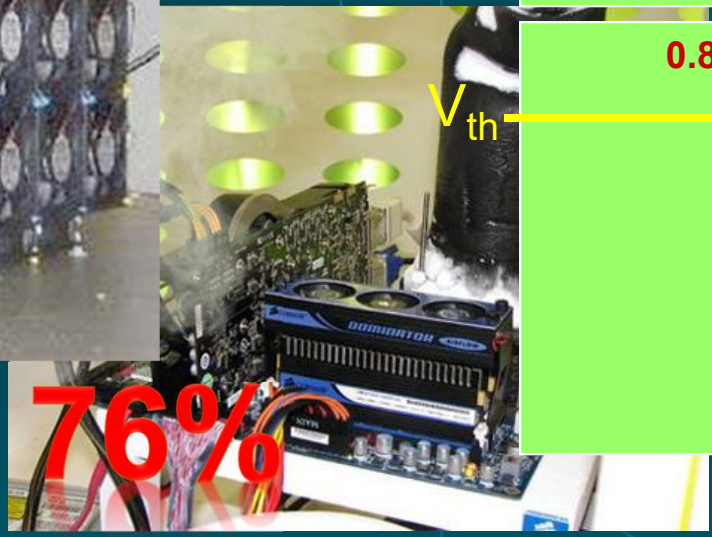


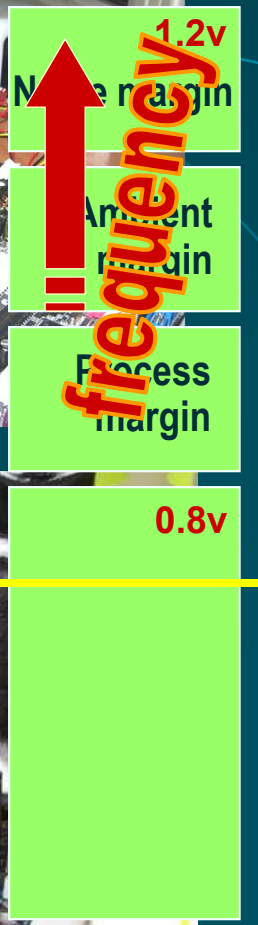
Goals of This Presentation

- Review some of the rules of low-power design ✔
- Show how clever designs can break these rules
  - **Razor** resilient circuits
  - **Subliminal** subthreshold voltage processor
- Highlight the benefits of taking a rule-breaking approach to technical research

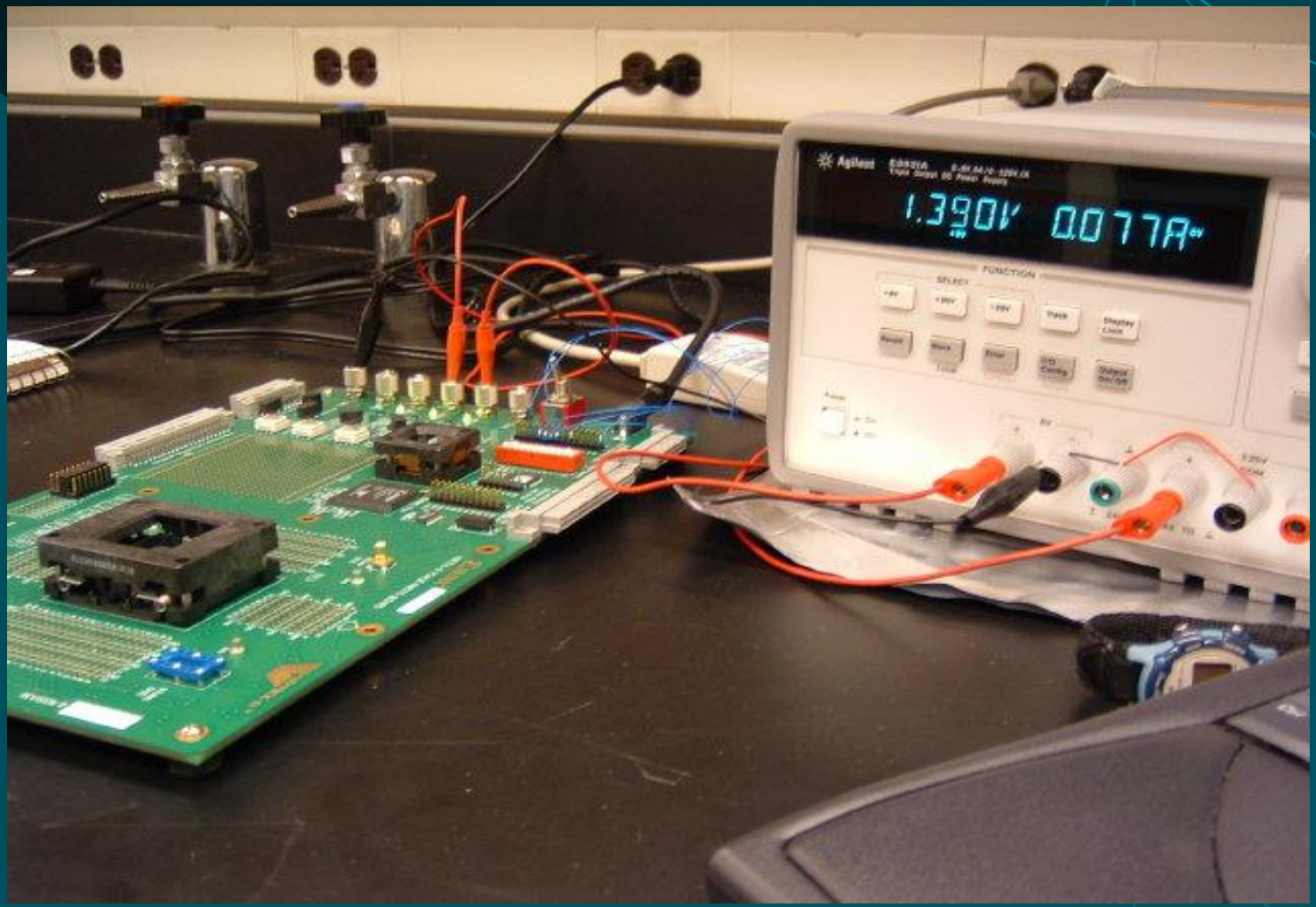
Overclockers Break the Rules



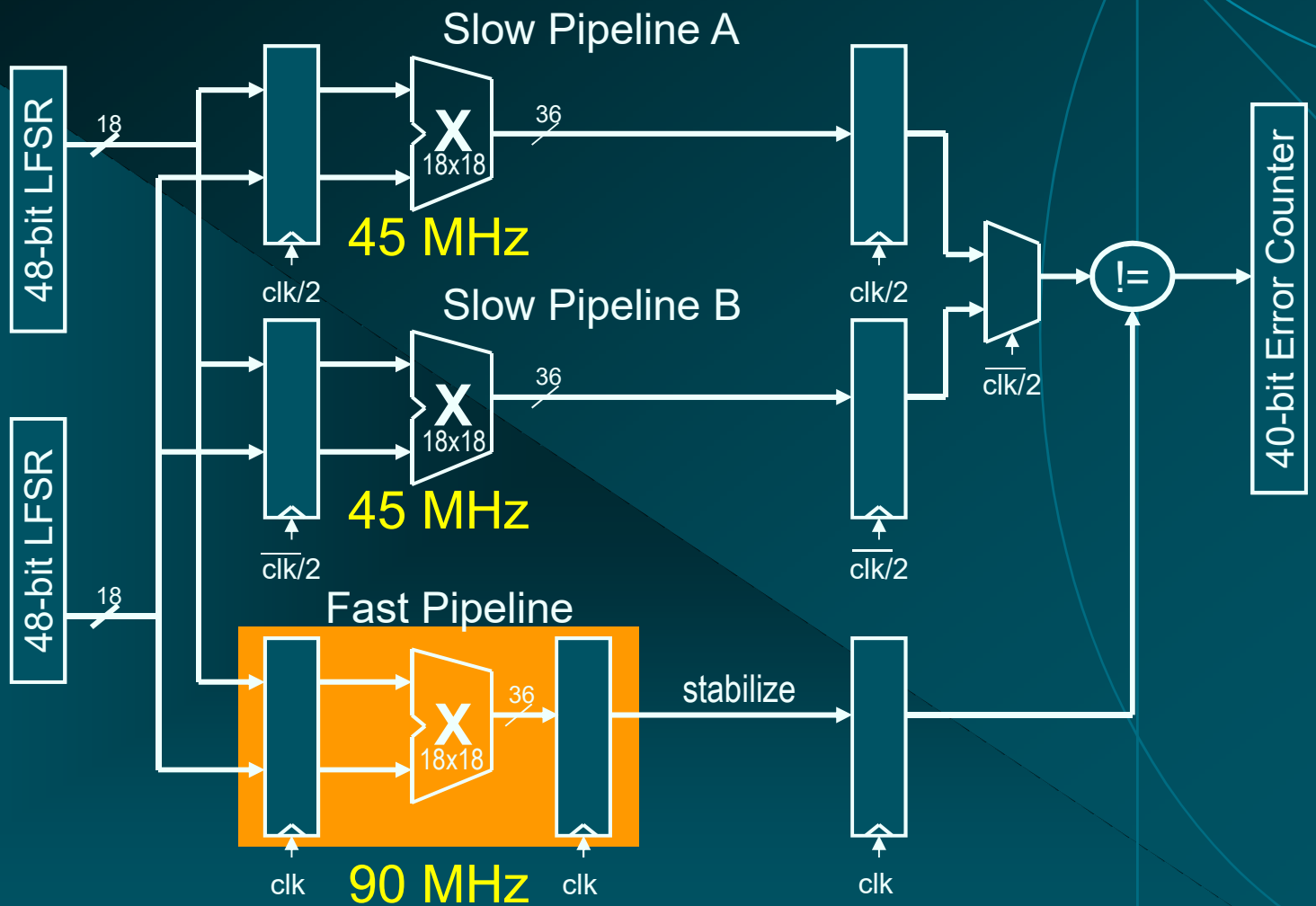




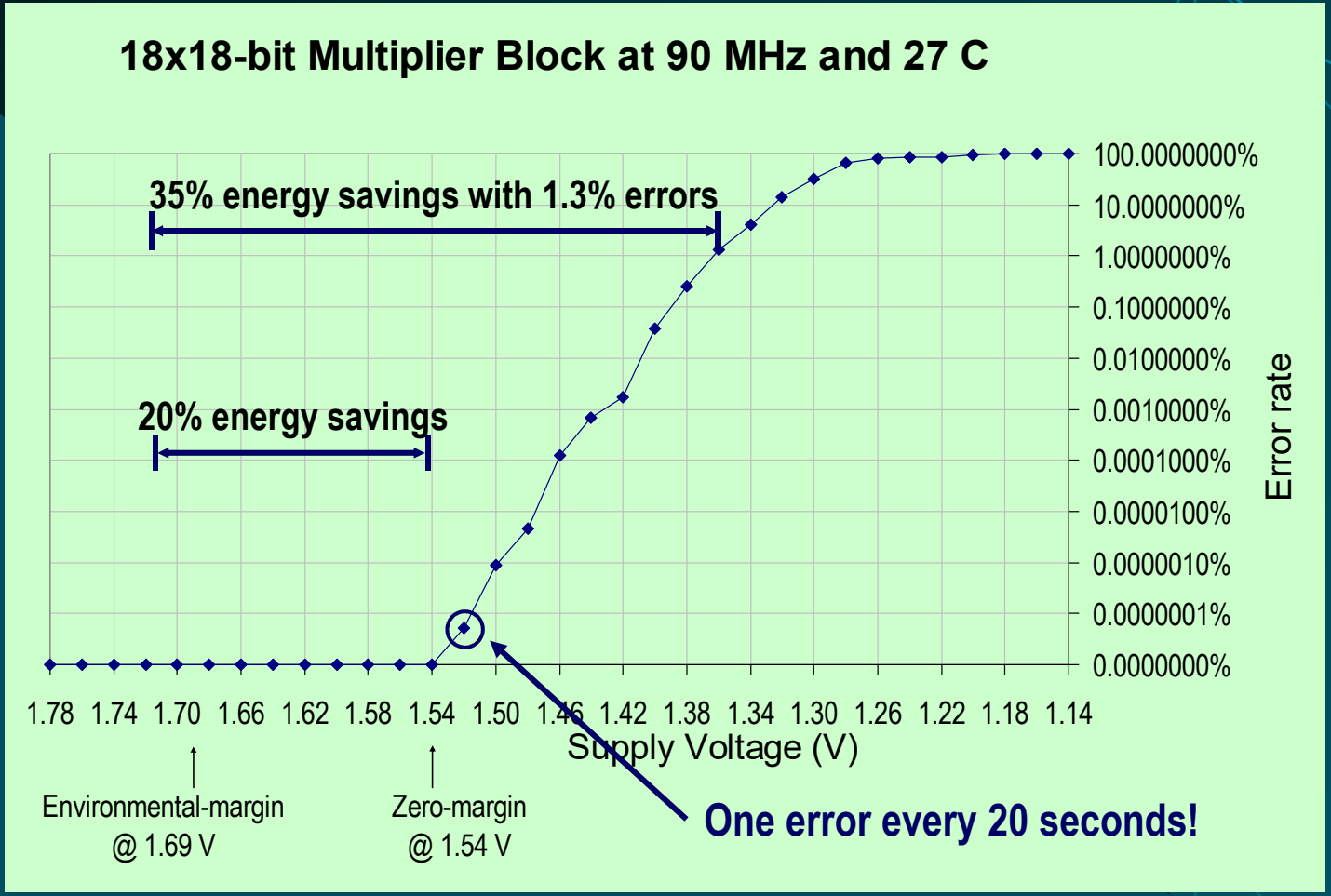
Investigating Overclocking



Two Slow Pipelines Check a Fast Pipeline

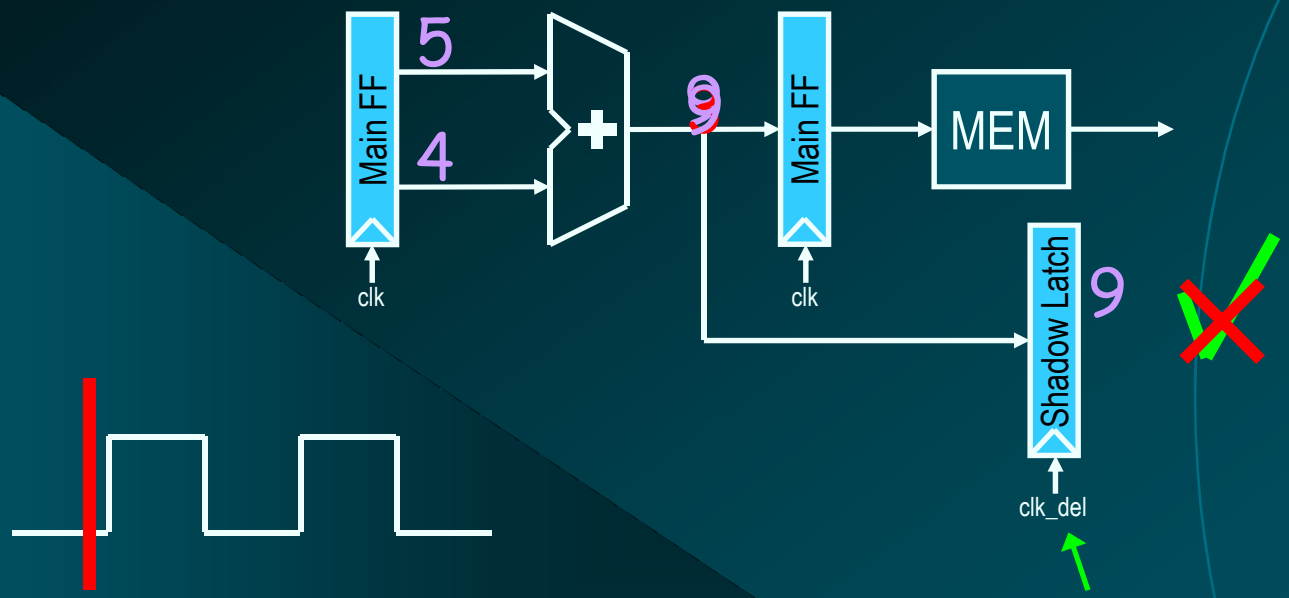


Discovery: Voltage Margins Are Plentiful



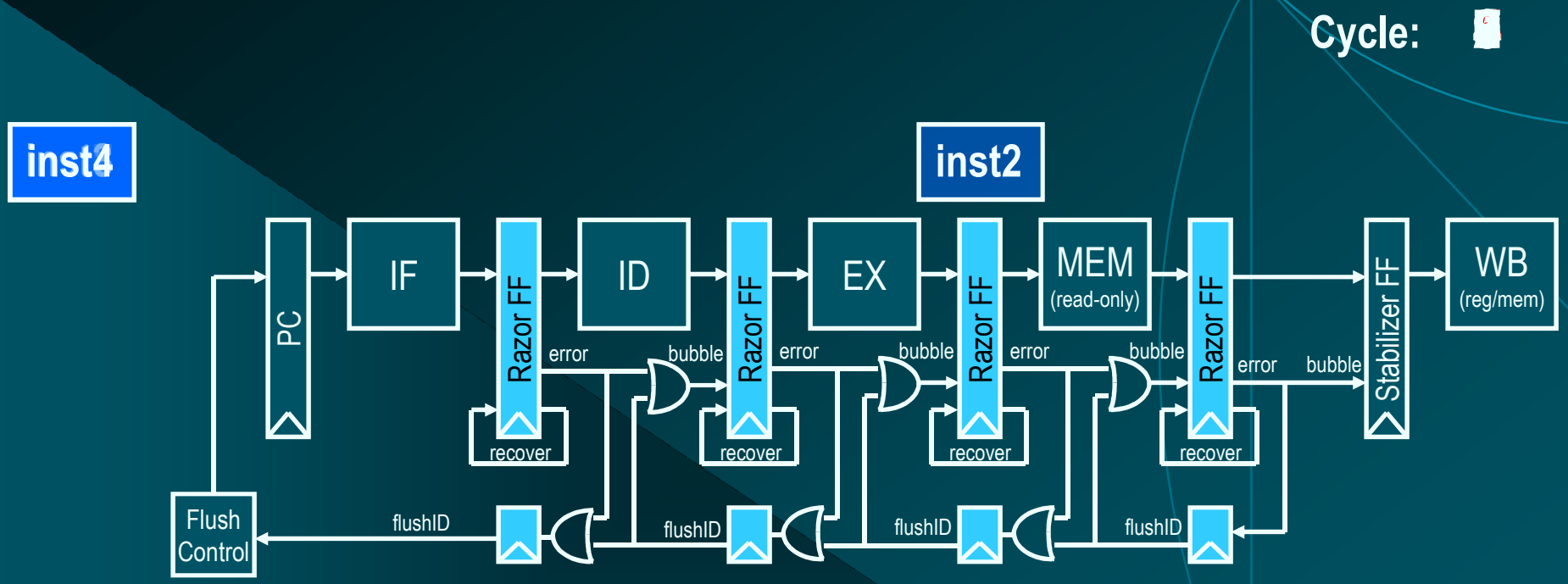
- Margin grows if a few (~1%) errors can be tolerated

Razor Resilient Circuits *[MICRO'03]*



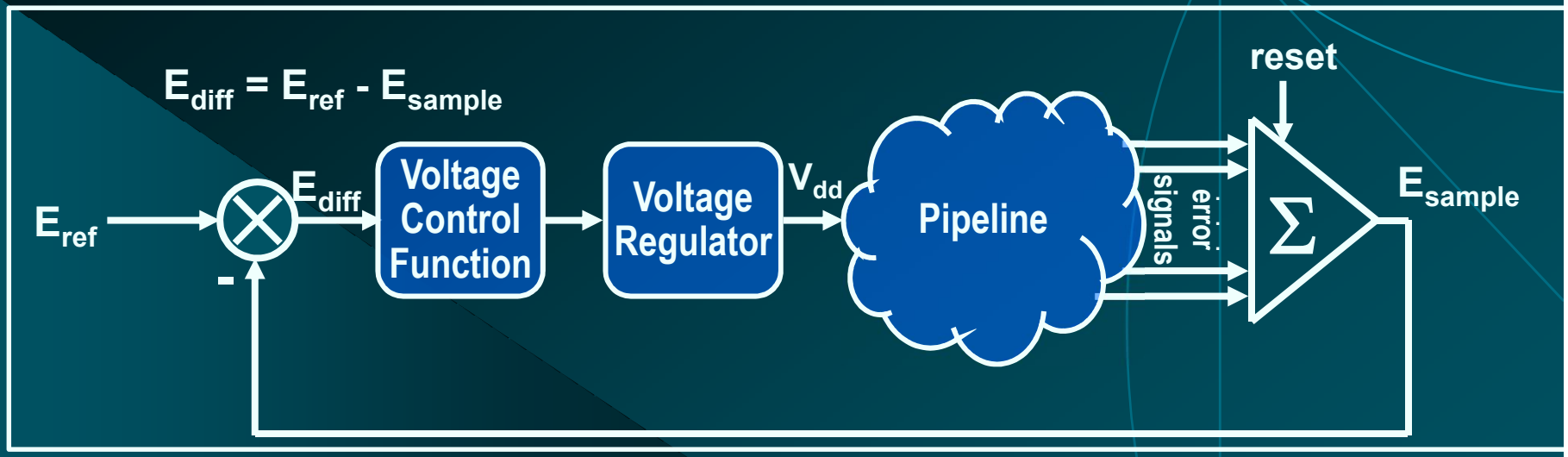
- Double-sampling metastability tolerant latches detect timing errors
  - Second sample is correct-by-design
- Microarchitectural support restores program state
  - Timing errors treated like branch mispredictions

Distributed Pipeline Recovery



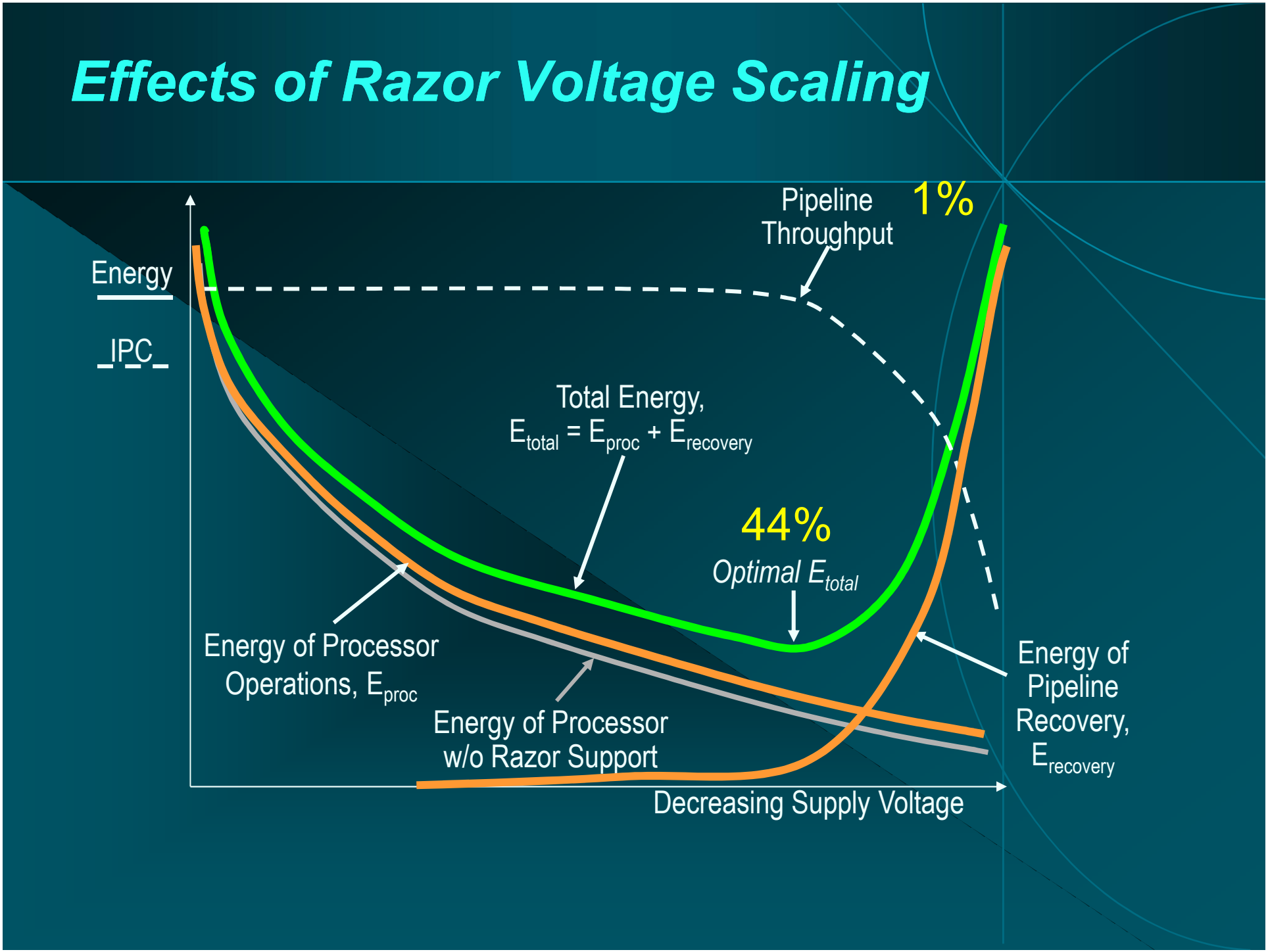
- Builds on existing branch prediction framework
- Multiple cycle penalty for timing failure
- Scalable design as all communication is local

Razor-Based Dynamic Voltage Scaling

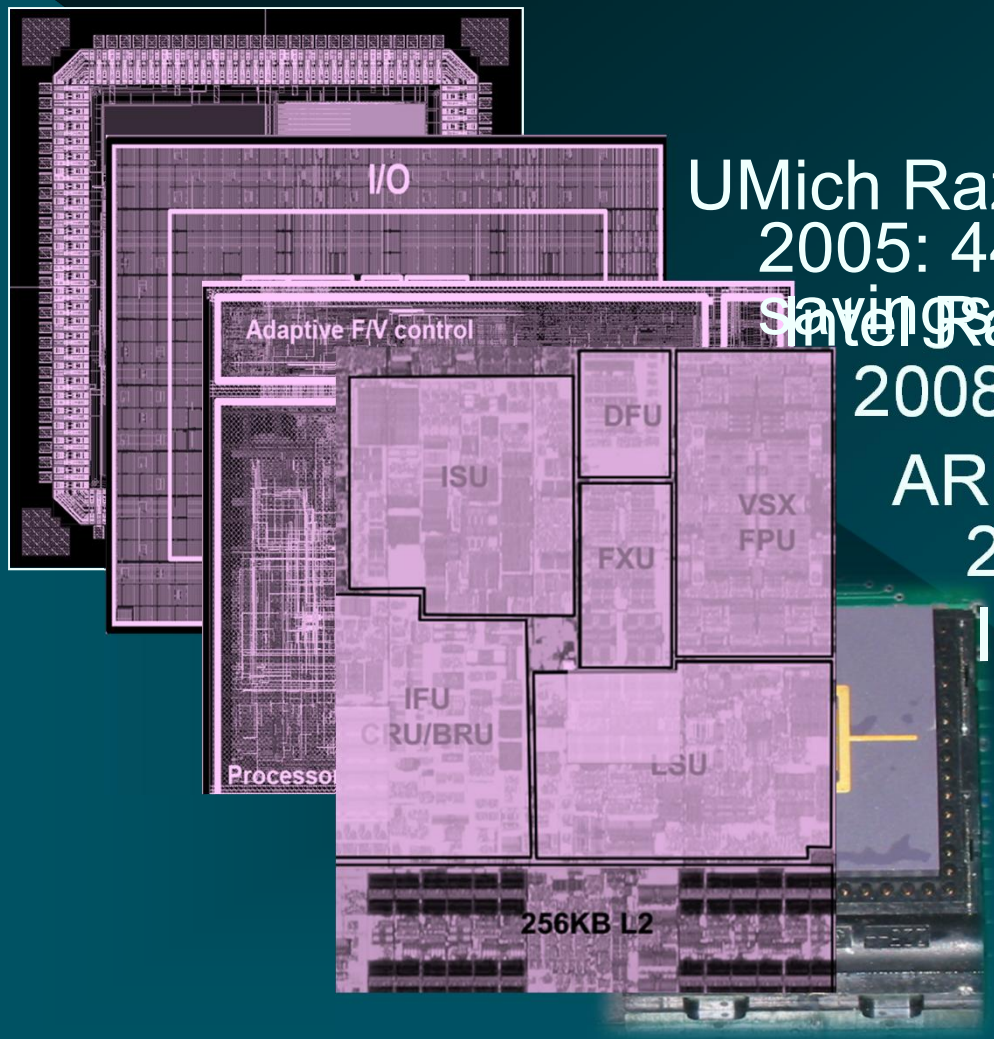


- Current design utilizes a very simple *proportional* control function
  - Control algorithm implemented in software

Effects of Razor Voltage Scaling



Razor (and Razor-like) Prototypes



UMich Razor Prototype
2005: 44% energy savings

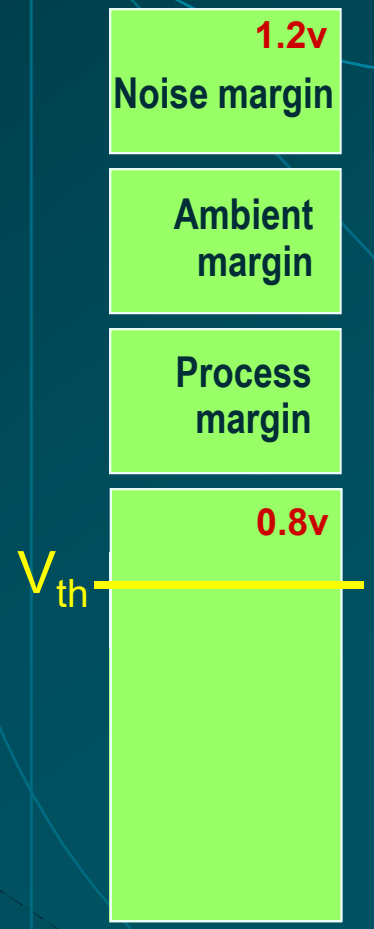
Intel Razor Prototype
2008: 32% power savings

ARM Razor Prototype
2010: 52% power savings

IBM Power7 Deployment
2011: 24% power savings

How Razor Breaks the Rules

- Traditional worst-case design techniques observe margin rules for reliable operation
- Incorporating timing-error correction mechanisms allow margins to be erased
- Infrequent use of critical paths allow for even deeper cuts in V_{dd}



What I Really Learned…

- A *rule-breaking approach* to technical research is effective and engaging
- You will often find yourself on very fertile ground
  - The "rules" create artificial barriers that hide good ideas
- You will more fully engage your community
  - One half will think your crazy idea will never work
  - One half will be intrigued (with your crazy idea)

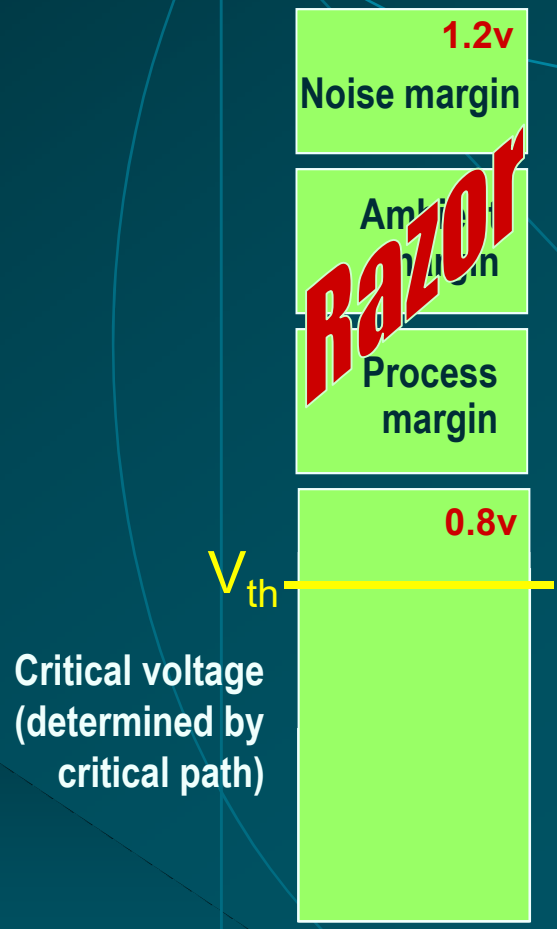
Back to the "Rules"

$$P = aCV^2f + VI_{leak}$$

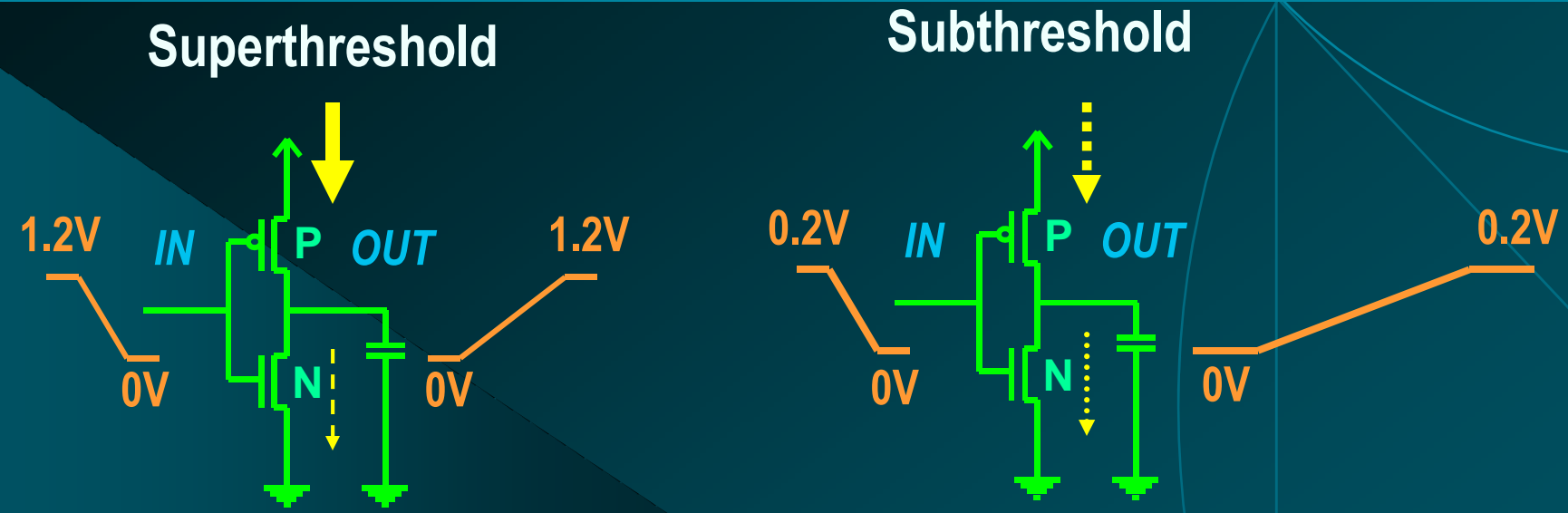
1. Minimize switching activity
2. Design for lower load capacitance
3. Reduce frequency
4. Reduce leakage

and the most important of all:

5. *Decrease supply voltage!*



Subthreshold Circuits Break The Rules



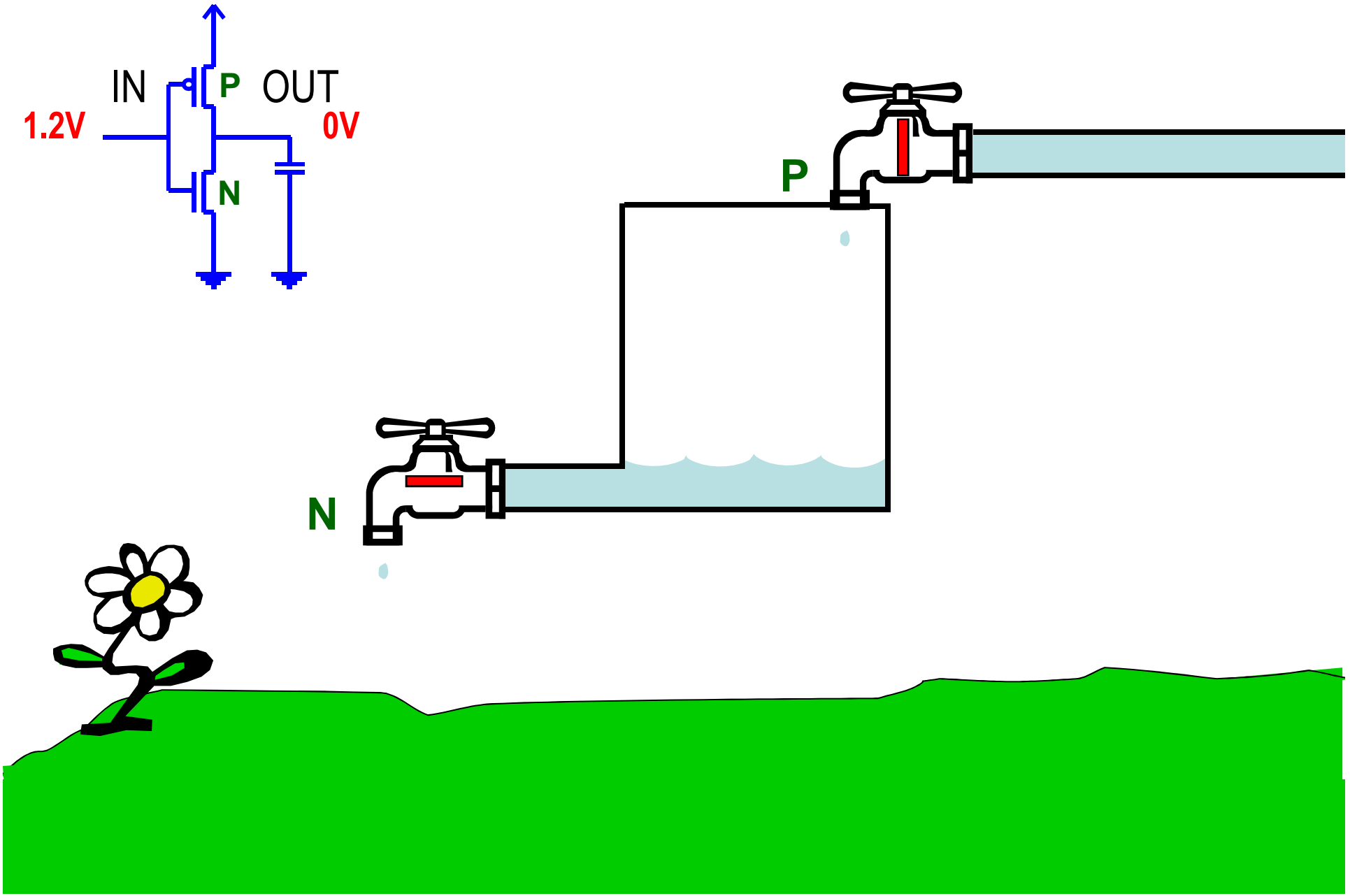
- Static logic still works below V_{th}
  - Differences in I_{leak} continue to (dis)charge outputs
  - But diminished I_{on}/I_{off} ratio results in big delays

The Basics of Subthreshold Circuit Operation

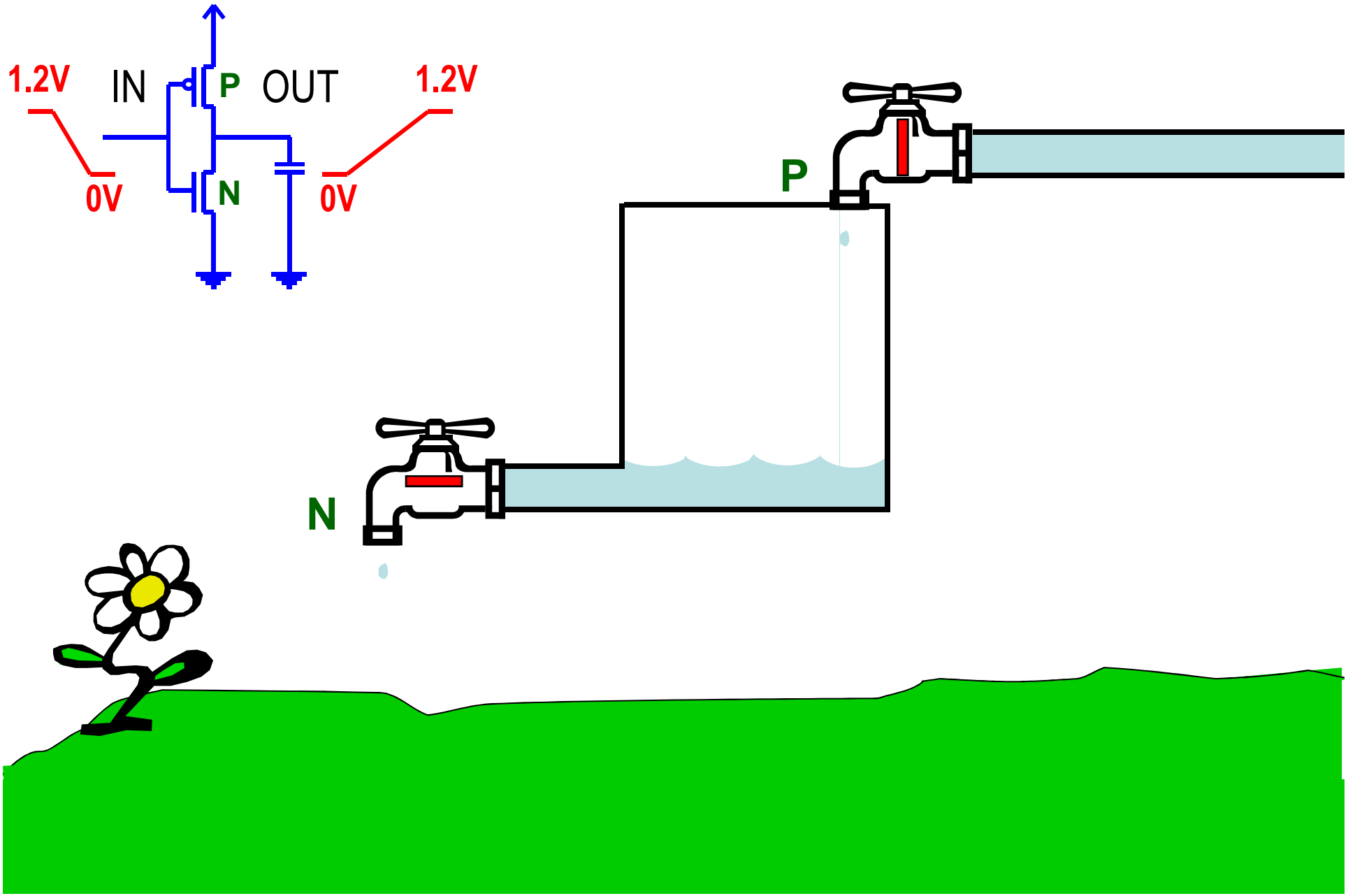
A Short Animation
by Leyla Nazhandali
@ Virginia Tech

Episode 1: Inverter operation in superthreshold domain

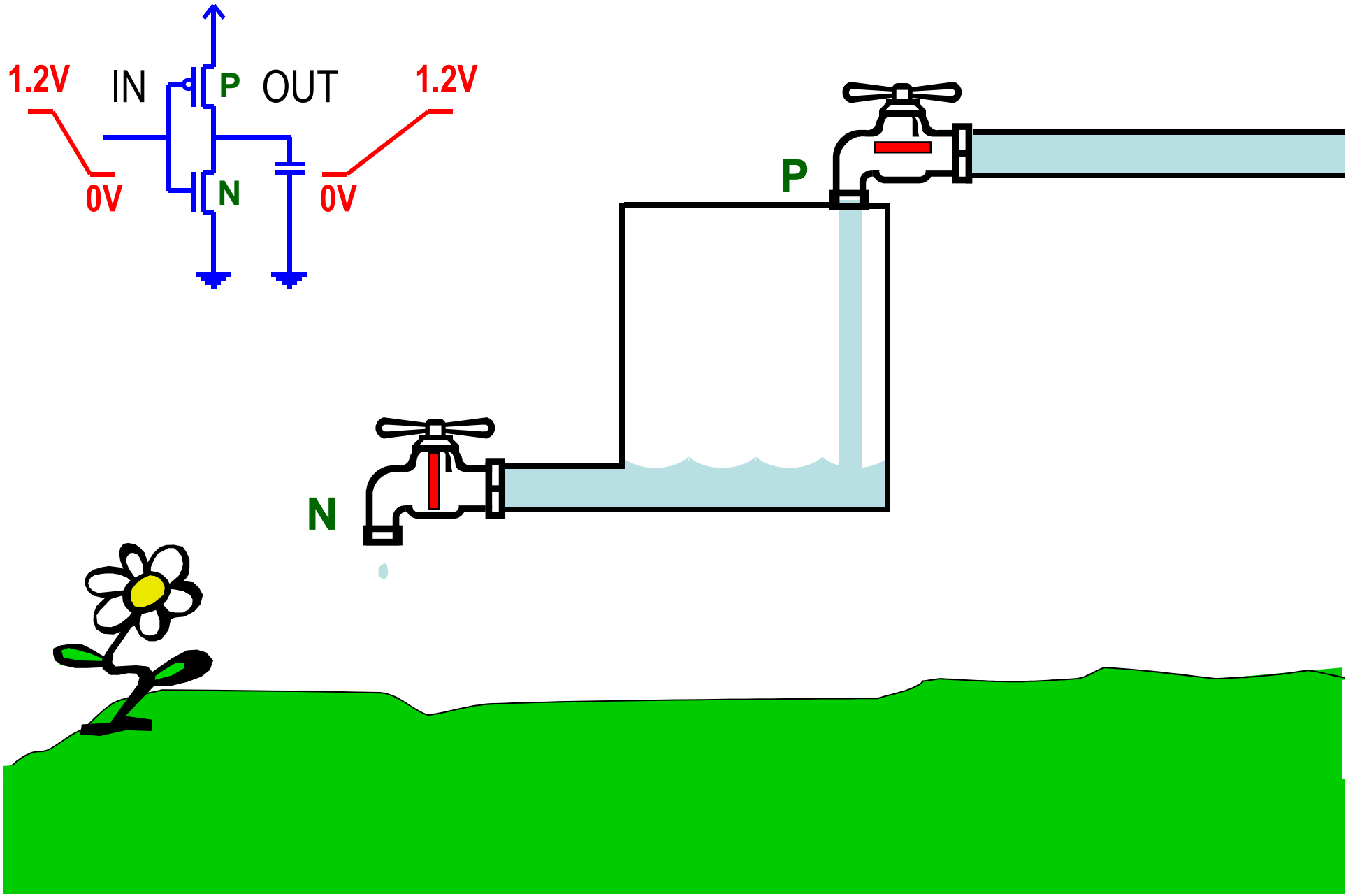
Superthreshold



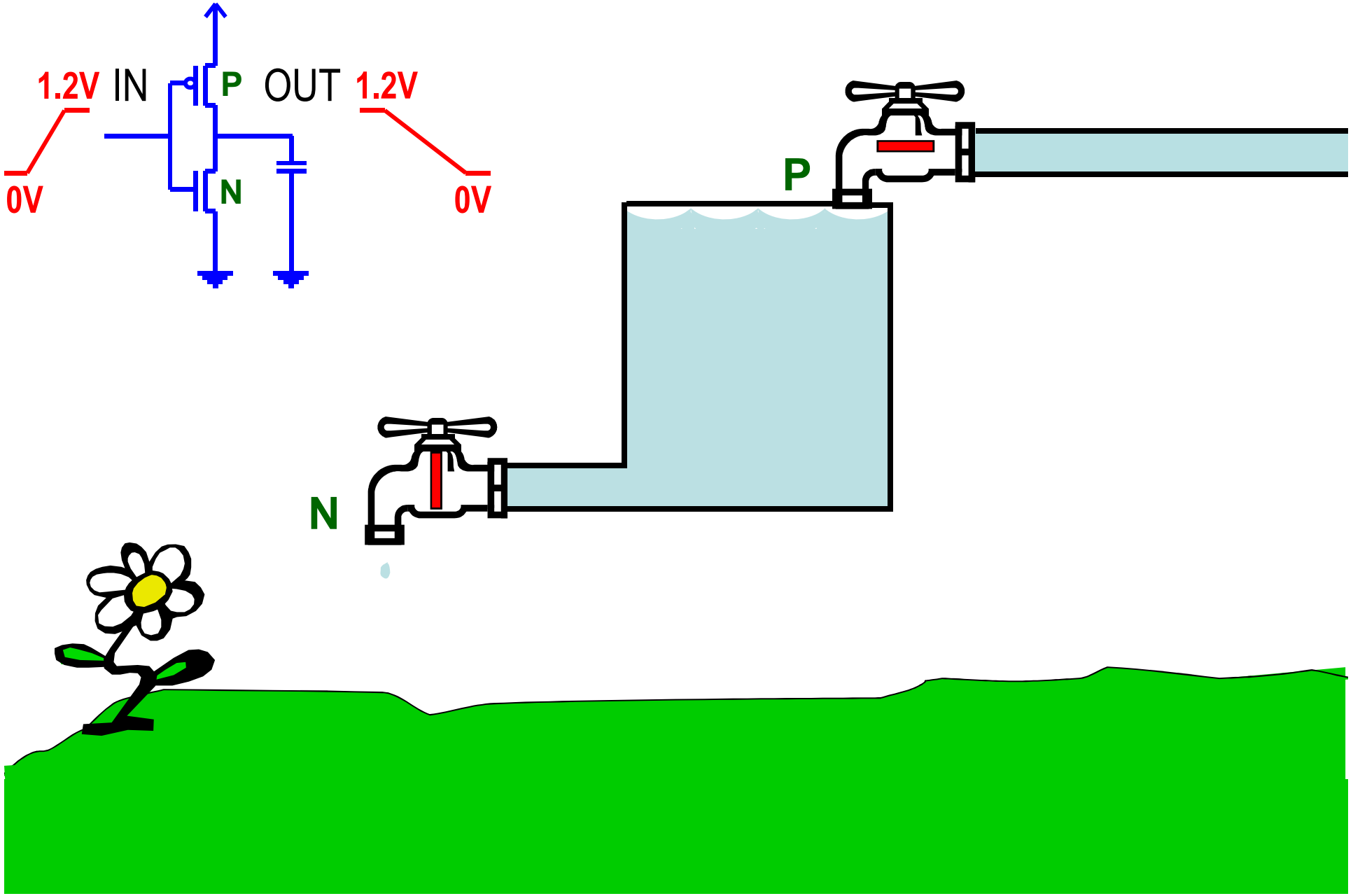
Superthreshold



Superthreshold

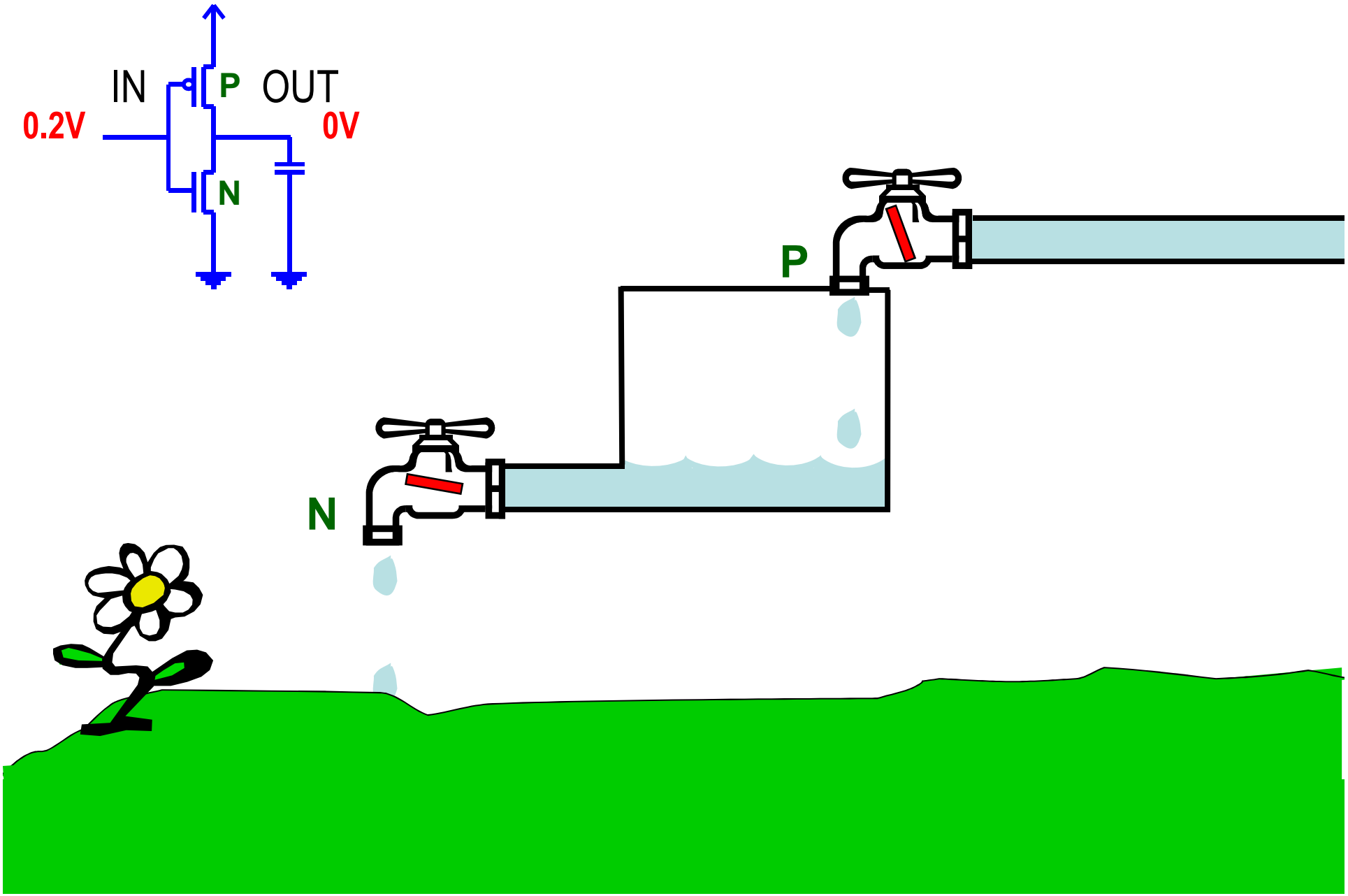


Superthreshold

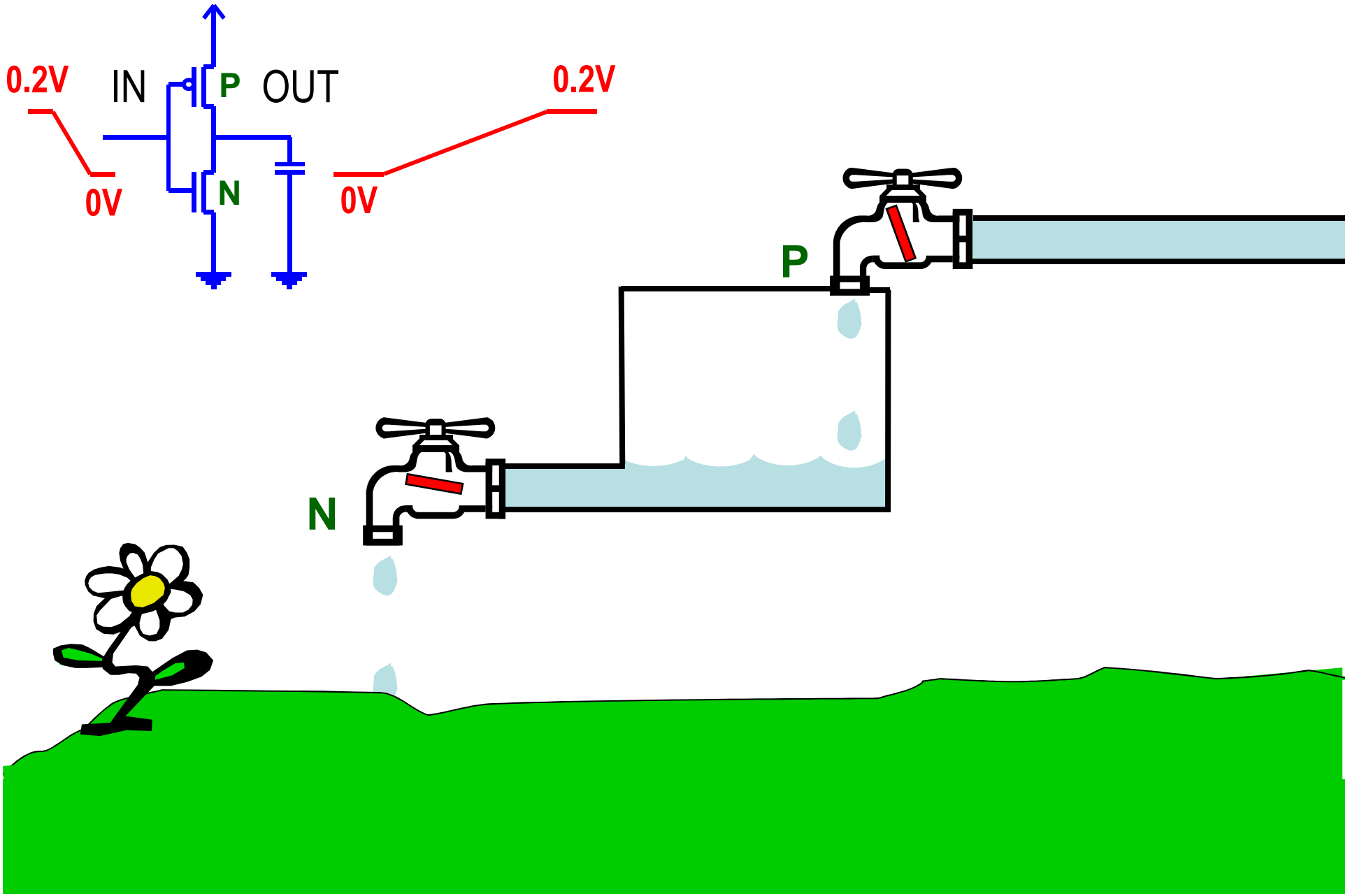


Episode 2: Inverter operation in subthreshold domain

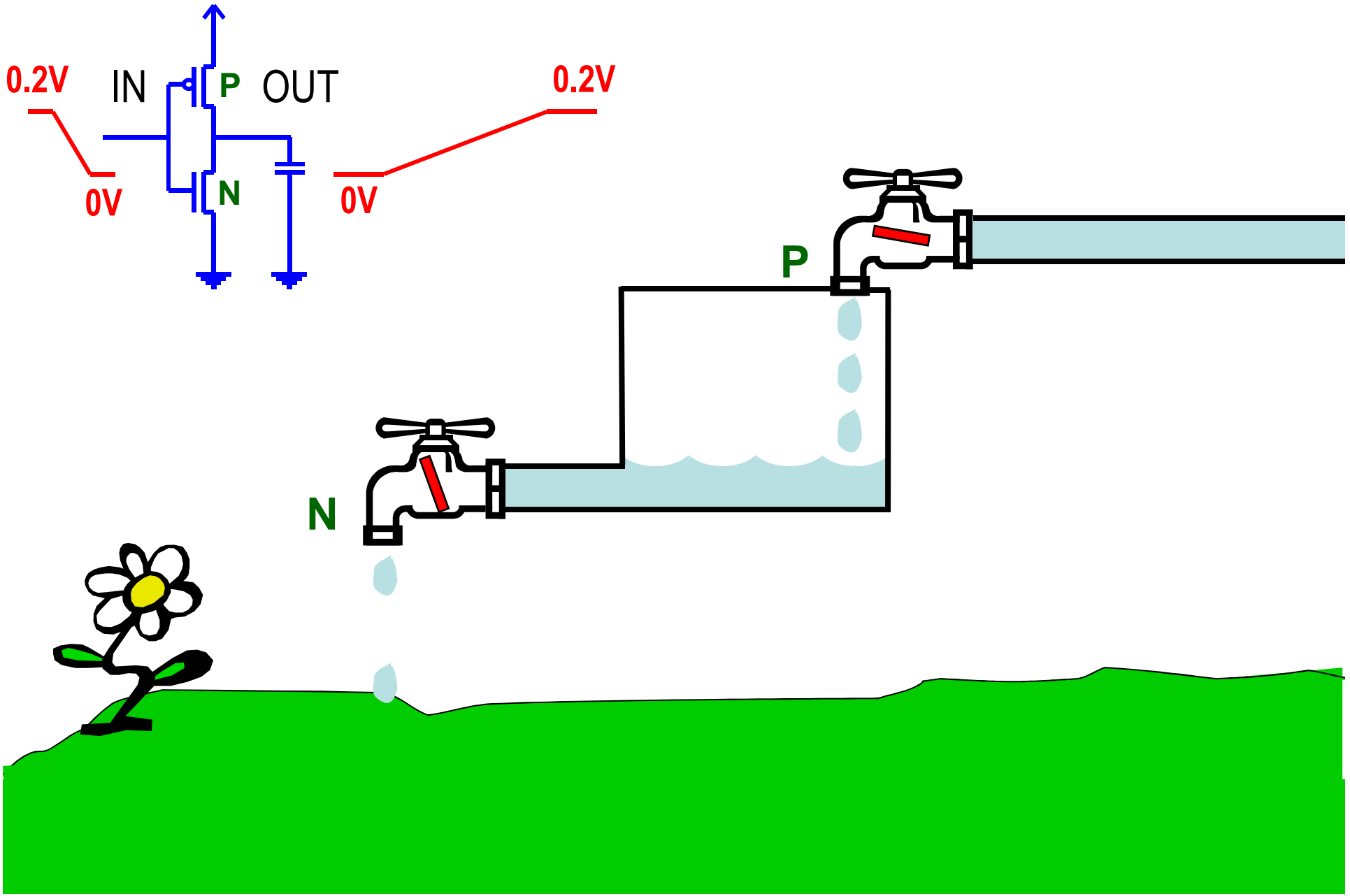
Subthreshold



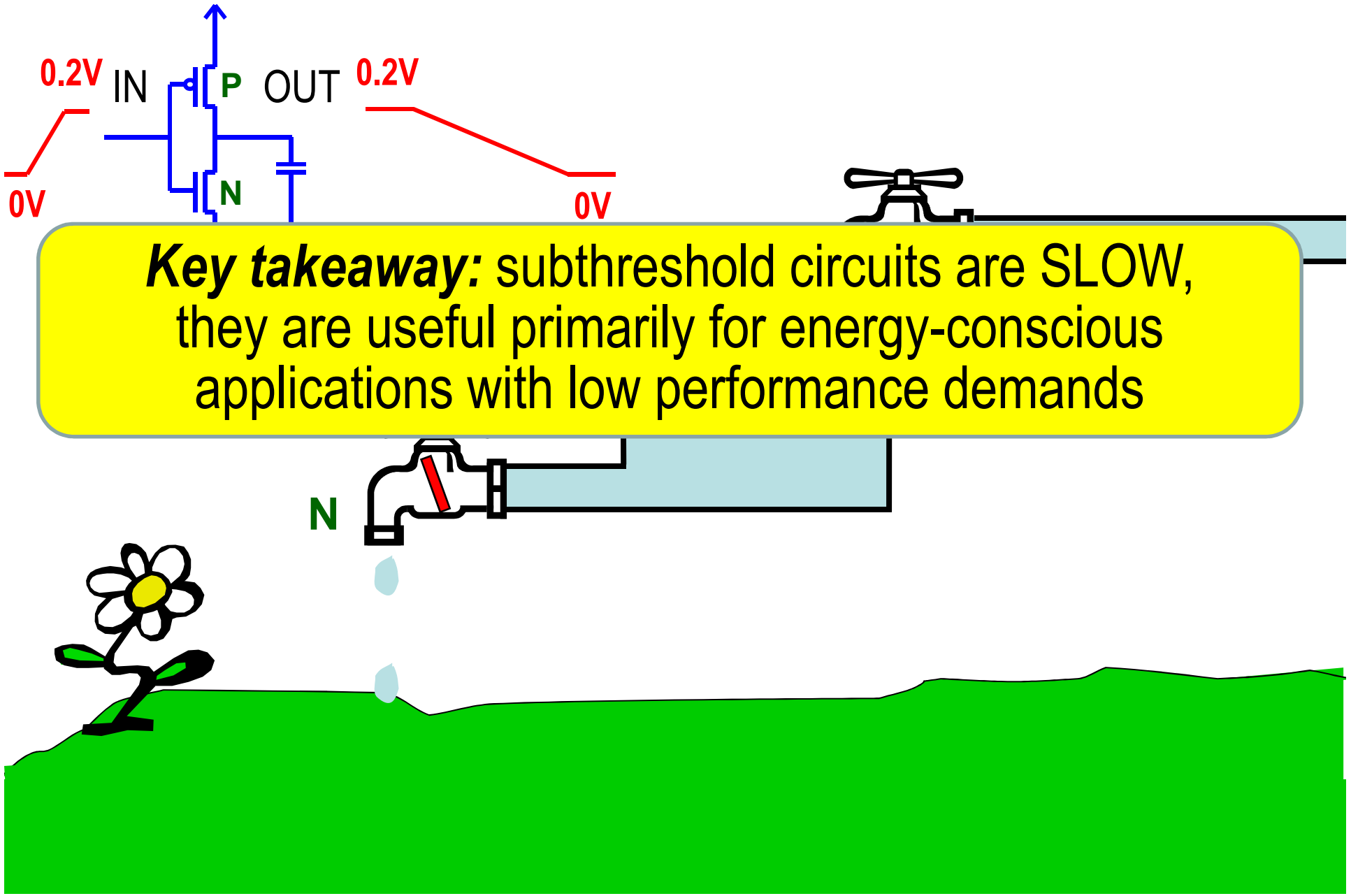
Subthreshold



Subthreshold

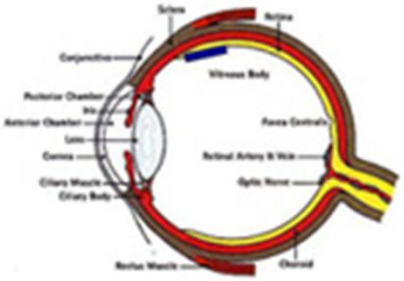


Subthreshold



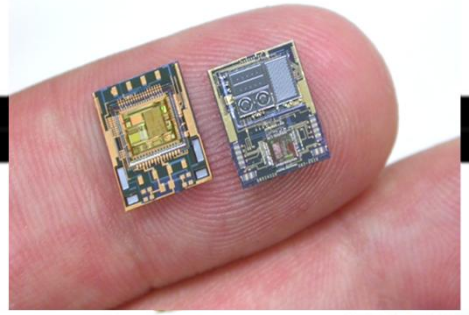
Key takeaway: subthreshold circuits are SLOW, they are useful primarily for energy-conscious applications with low performance demands

(Not Too Demanding) Sensing Applications



Security

Biomedical



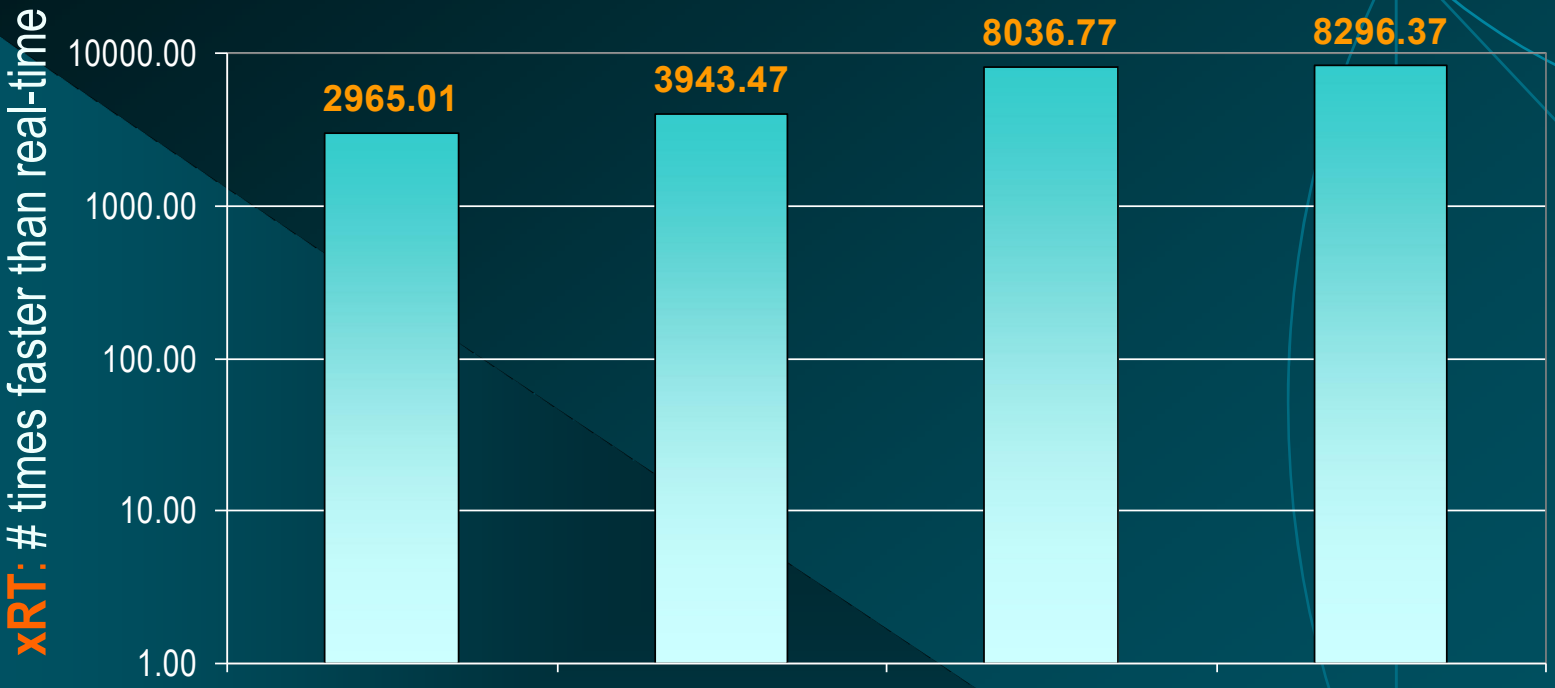
Environmental

Industrial

Sensor Processing Data Rates

Phenomena	Sample Rate	Sample Precision
Low Frequency Band (< 100 Hz)		
Ambient light level	0.017 - 1 Hz	16 bits
Atmospheric temperature	0.017 - 1 Hz	16 bits
Body temperature	0.1 - 1 Hz	8 bits
Natural seismic vibration	0.2 - 100 Hz	8 bits
Heart rate	0.8 - 3.2 Hz	1 bit
Wind speed	1 - 10 Hz	16 bits
Oral-nasal airflow	16 - 25 Hz	8 bits
Blood pressure	50 - 100 Hz	8 bits
Mid Frequency Band (100 Hz - 1 kHz)		
Engine temperature and pressure	100 - 150 Hz	16 bits
EOG (eyeball electrical activity)	100 - 200 Hz	16 bits
ECG (heart electrical activity)	100 - 250 Hz	8 bits
High Frequency Band (> 1 kHz)		
EMG (skeletal muscle activity)	100 - 5 kHz	8 bits
Audio (human hearing range)	15 Hz - 44 kHz	16 bits

Sensing Performance Demands are Low



Platform	ARM 720T	ARM 7TDMI	ARM 920T	ARM 1020T
Voltage (V)	1.2	1.2	1.2	1.2
Speed (Hz)	100M	133M	250M	325M

Fast Growing Leakage Complicates Design

$$E_{inst} = E_{cycle}\ CPI$$

- CPI → Cycles per Instruction
- E_{inst} → Energy per Instruction
- E_{cycle} → Energy per Cycle

$$E_{cycle} = \tfrac{1}{2}\alpha C_s V_{dd}^2 + V_{dd} I_{leak} t_{clk}$$

- α → Activity factor - average number of transistor switches per transistor per cycle
- C_s → Total circuit capacitance
- V_{dd} → Supply Voltage
- I_{leak} → Leakage current
- t_{clk} → Clock period

Fast Growing Leakage Complicates Design

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Activity factor - average number of transistor switches per transistor per cycle

Total circuit capacitance

Supply Voltage

Leakage current

Clock period

Impact of voltage reduction					
	I_{leak}	t_{clk}	E_{leak}	E_{dyn}	E_{cycle}
Superthreshold	⇓ linear	⇑ linear	~const.	⇓ quad.	⇓ quad.
Subthreshold	⇓ linear	⇑ exp.	⇑ ~exp.	⇓ quad.	???

Tension

Fast Growing Leakage Complicates Design

Impact of voltage reduction					
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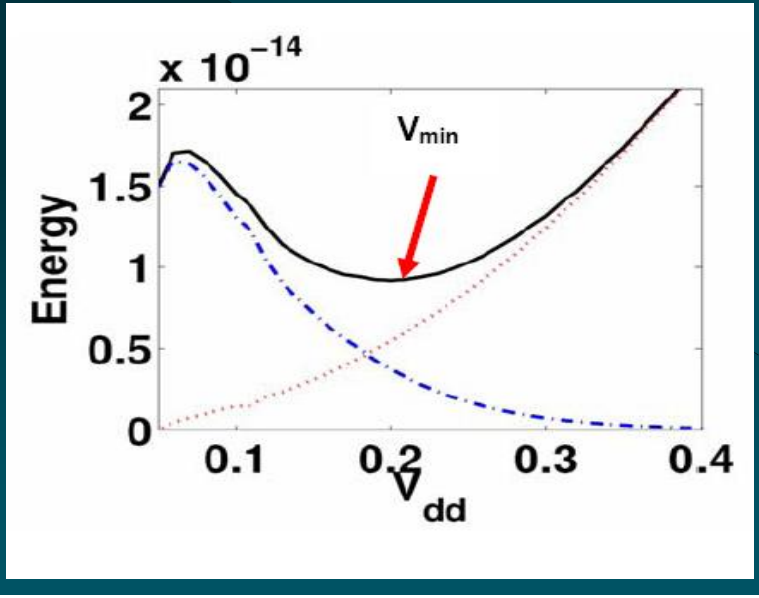
Superthreshold	⇓ linear	⇑ linear	~const.	⇓ quad.	⇓ quad.
Subthreshold	⇓ linear	⇑ exp.	⇑ ~exp.	⇓ quad.	???

Tension



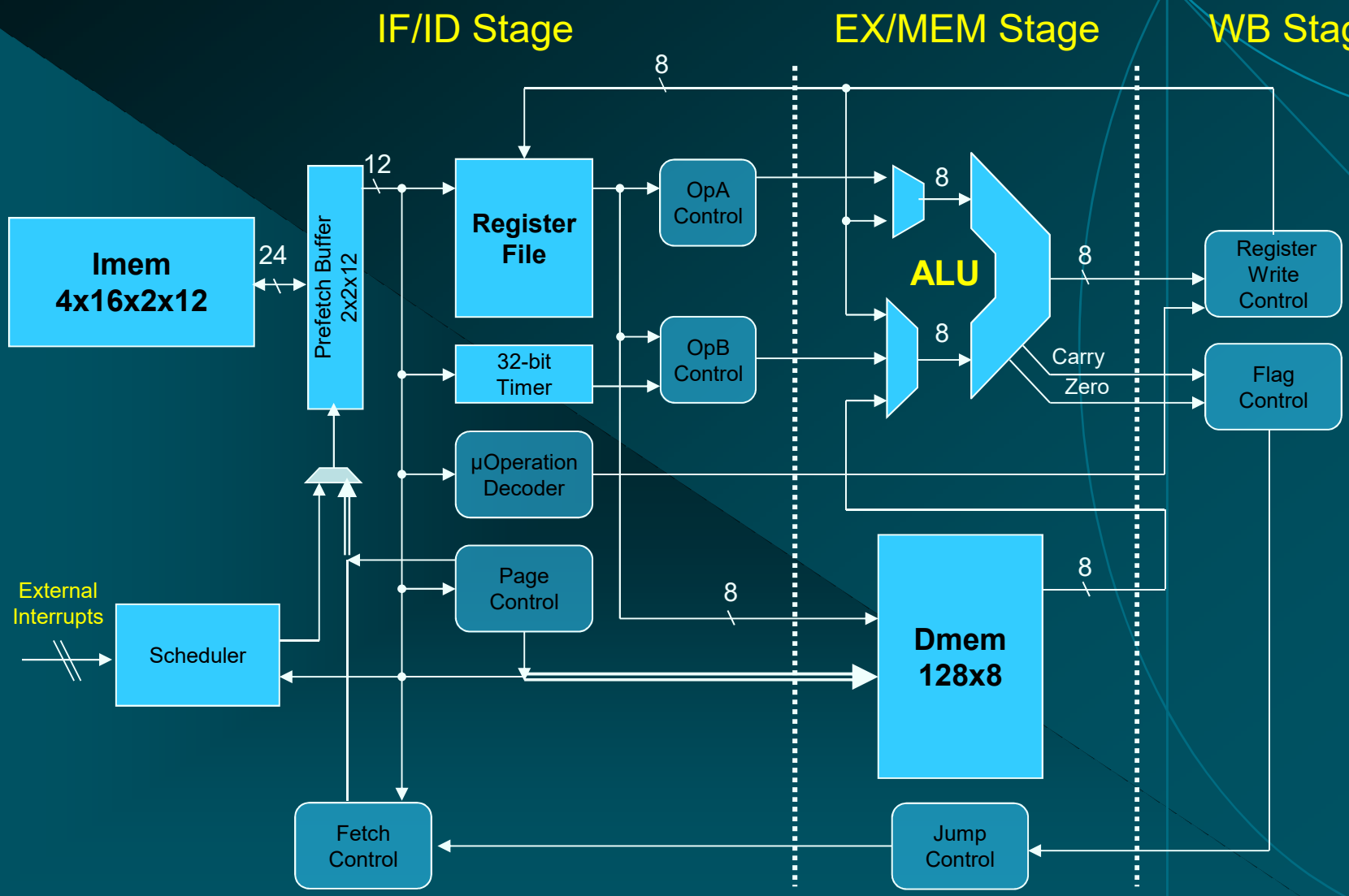
Lessons from Architectural Studies [ISCA'05]

- **To minimize energy at subthreshold voltages, architects must:**

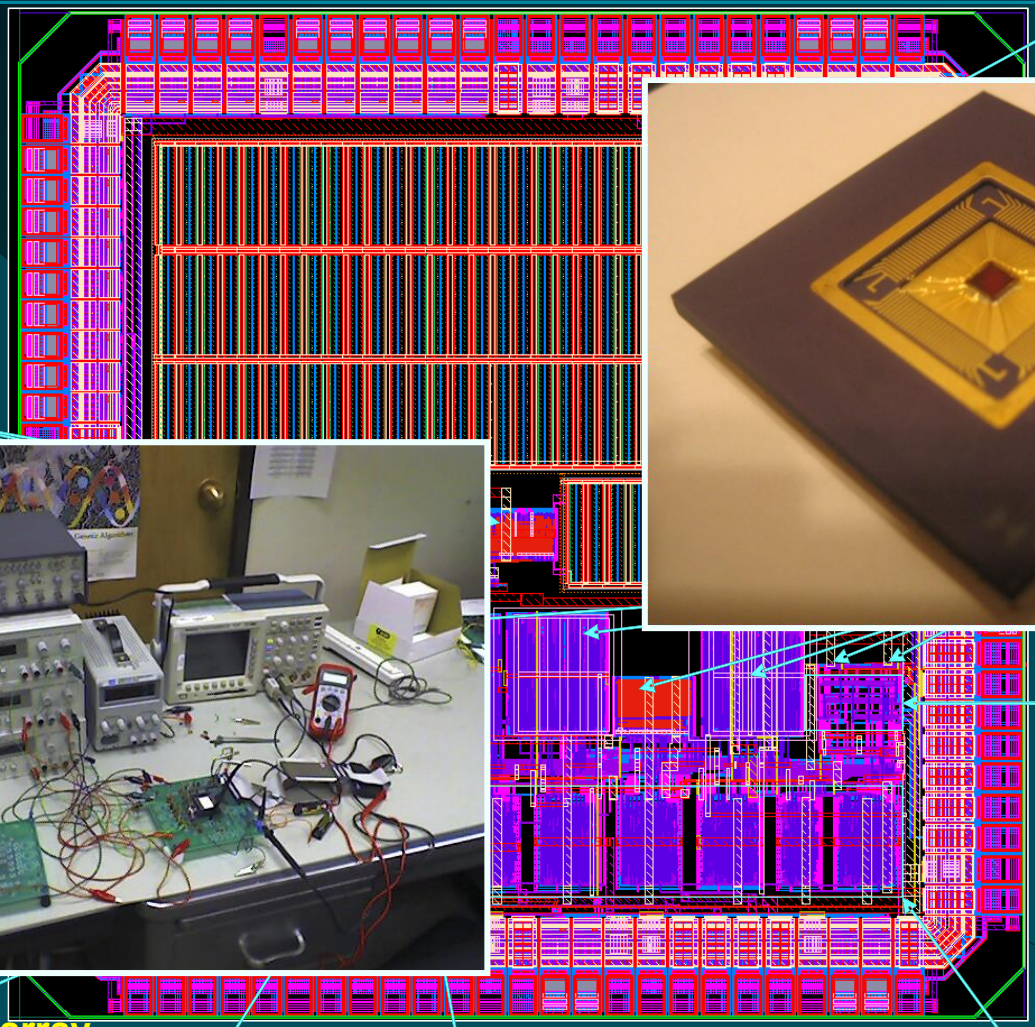
Minimize area	⇨	To reduce leakage energy per cycle
Maximize Transistor utility	⇨	To reduce V_{min} and energy per cycle
Minimize CPI	⇨	To reduce Energy per instruction

- **Winning designs tend to be compromising designs that balance area, transistor utility and CPI**
- **Memory comprises the largest leakage energy, therefore, efficient designs must minimize storage**

Subliminal Architecture Overview



First Subliminal Chip *[JSSC'08]*



Large solar cell

cessor

Custom memories

rete cells

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Test

T

level converter array

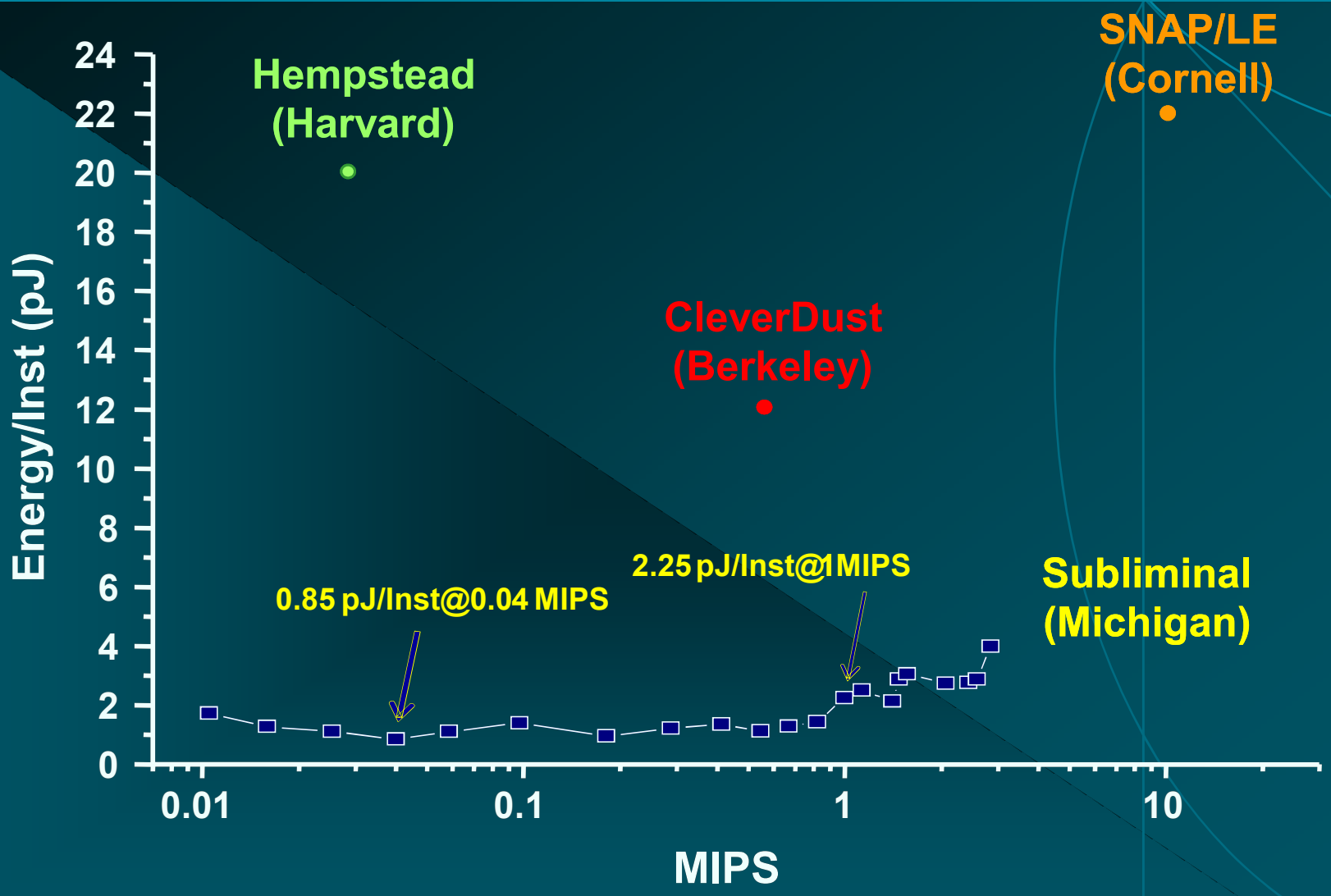
Level converter array

Solar cell for adders

Discrete adders

Subliminal processors

Pareto Analysis of Sensor Network Processors



How Subliminal Breaks the Rules

- Traditional circuit design relies an transistor switching to perform computation
- Static logic circuits continue to operate below V_{th} by modulating leakage currents
- Approach lends itself to low-demand sensor apps, as long as care is taken to build an efficient processor

More Thoughts on Research…

- A rule-breaking approach is more prone to failure
  - "If you're not failing every now and again, it's a sign you're not doing anything very innovative." -Woody Allen
- Getting the word out is critical to an idea's success
  - Be an evangelist for your project
  - Name your project so the community can talk about it
- Building H/W (ASICs) is a double-edged sword
  - + Sometimes you can't be convincing w/o a physical demo
  - + If you build it, they (i.e., industry) will come
  - - ASICs are hungry: they eat money, time people, opportunity
  - - Often physical demos render limited insights

Concluding Thoughts

- The "rules" of low-power design guide much of the work in academia and industry today
- Breaking these rules, can lead to significant benefits
  - **Razor** resilient circuits use resiliency mechanisms to eliminate voltage margins
  - **Subliminal** subthreshold voltage processor minimizes energy by deftly operating below the threshold voltage
- To me, research is all about breaking the "rules", perhaps you too might find it a great way to identify new and exciting opportunities

Questions