

Threadmill: A Post-Silicon Exerciser for Multi-Threaded Processors

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Presenters: Abraham Addisie and Dong-hyeon Park

Outline

Motivation

Overview of Threadmill

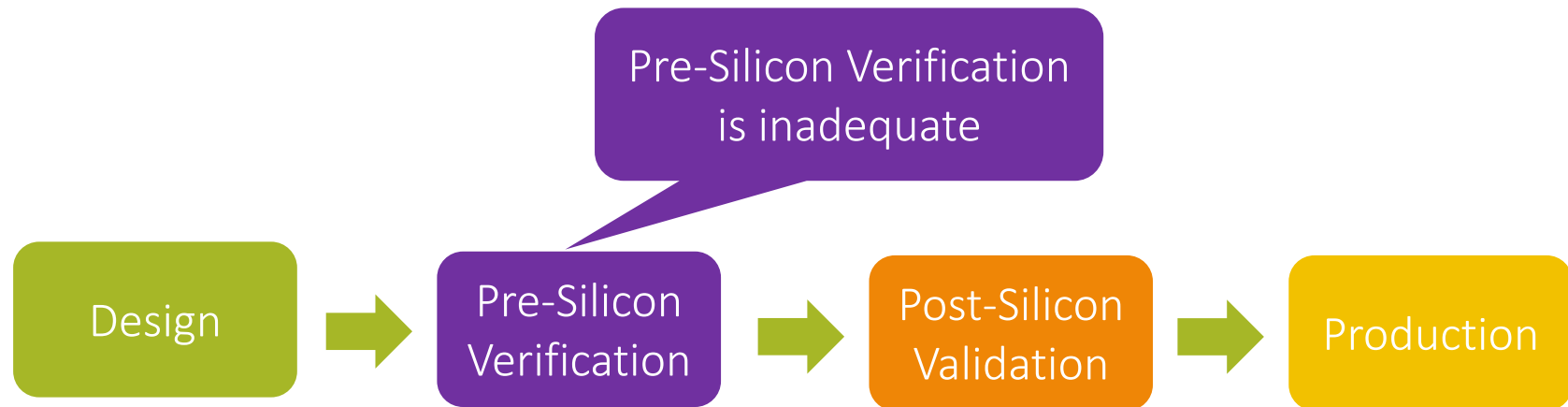
Key Techniques of Threadmill

Conclusion

Questions

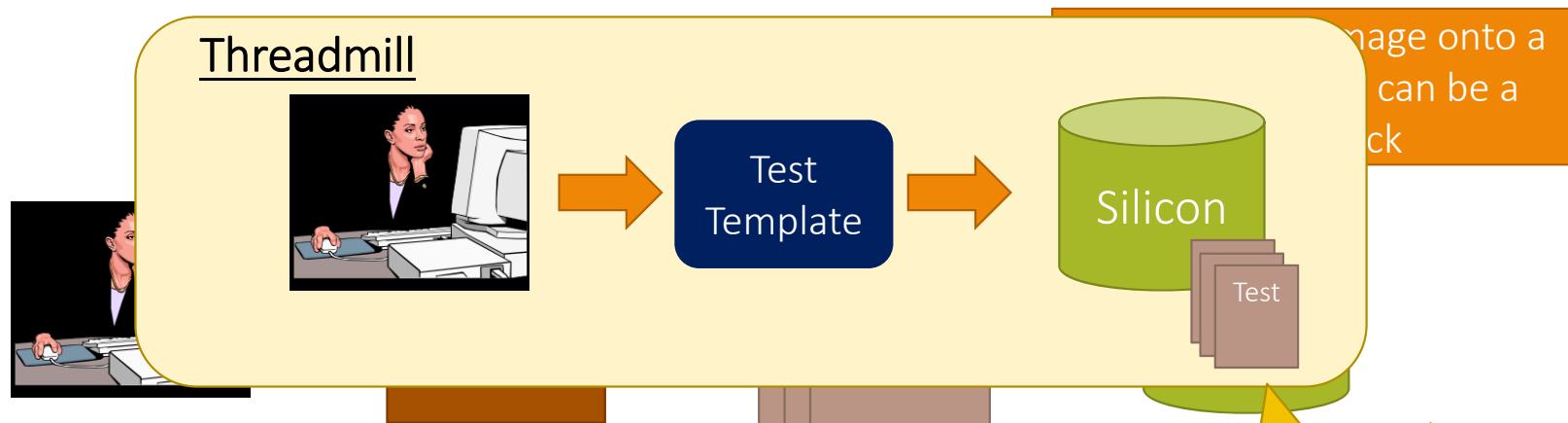
Debate!

Motivation – Why Post Silicon?



- Post-Silicon validation is becoming the next-level vehicle for functional verification

Problems of Post-Silicon Validation



- Loading tests externally have high communication and memory overhead
- Existing on-platform test generators are too slow
- Developing full OS system takes time

Solution:
Simple on-platform
test generator

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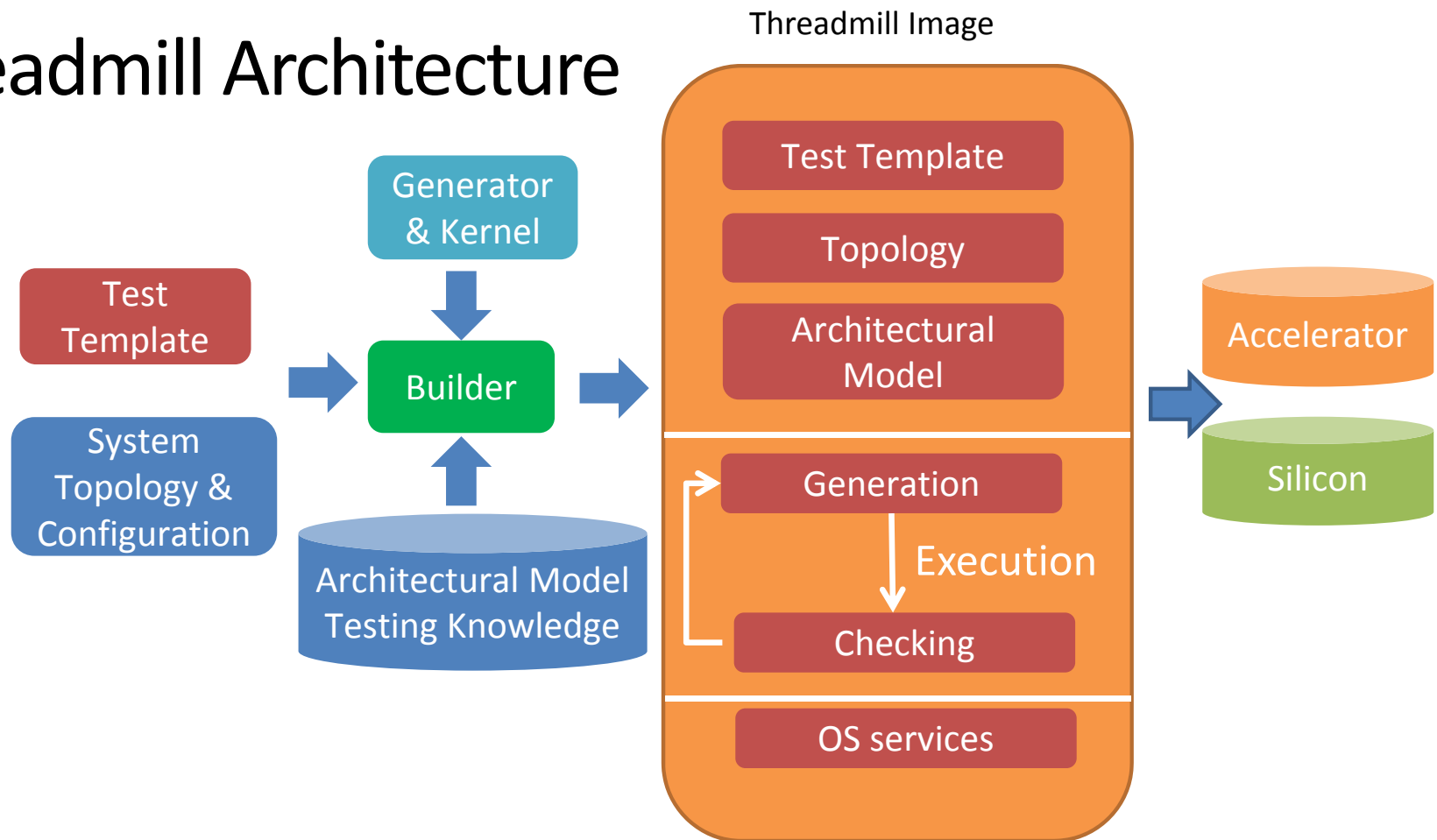
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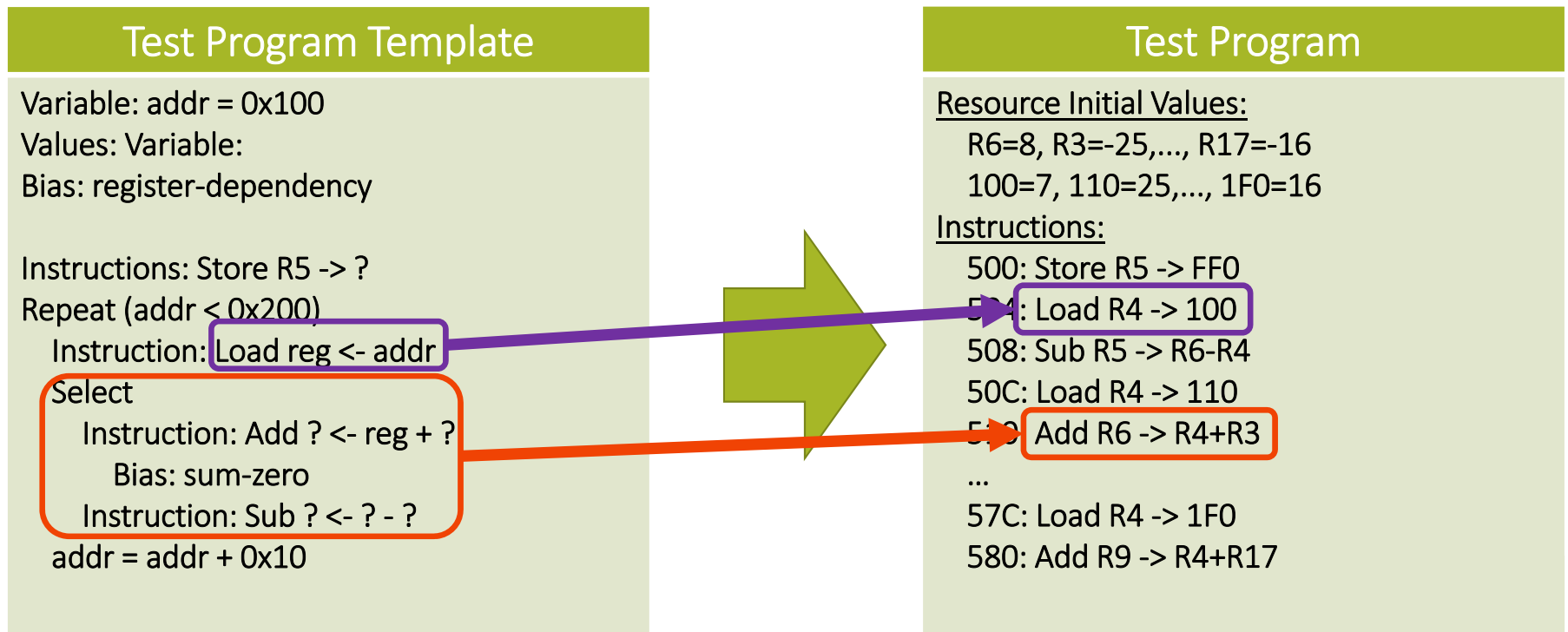
Questions

Debate!

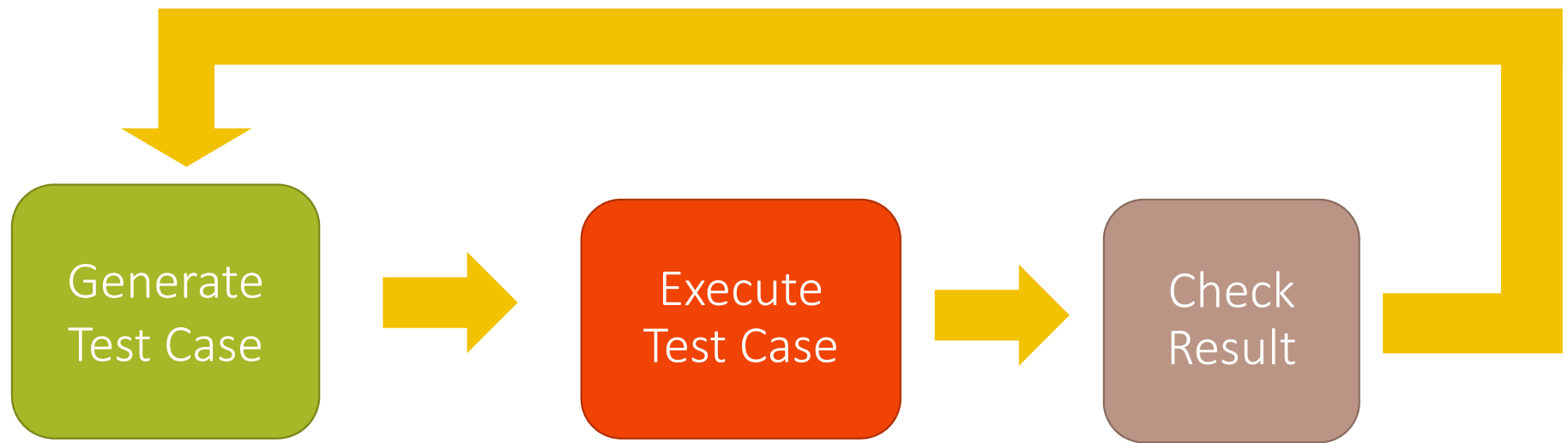
Threadmill Architecture



Test-Template Language



Execution Process



Outline

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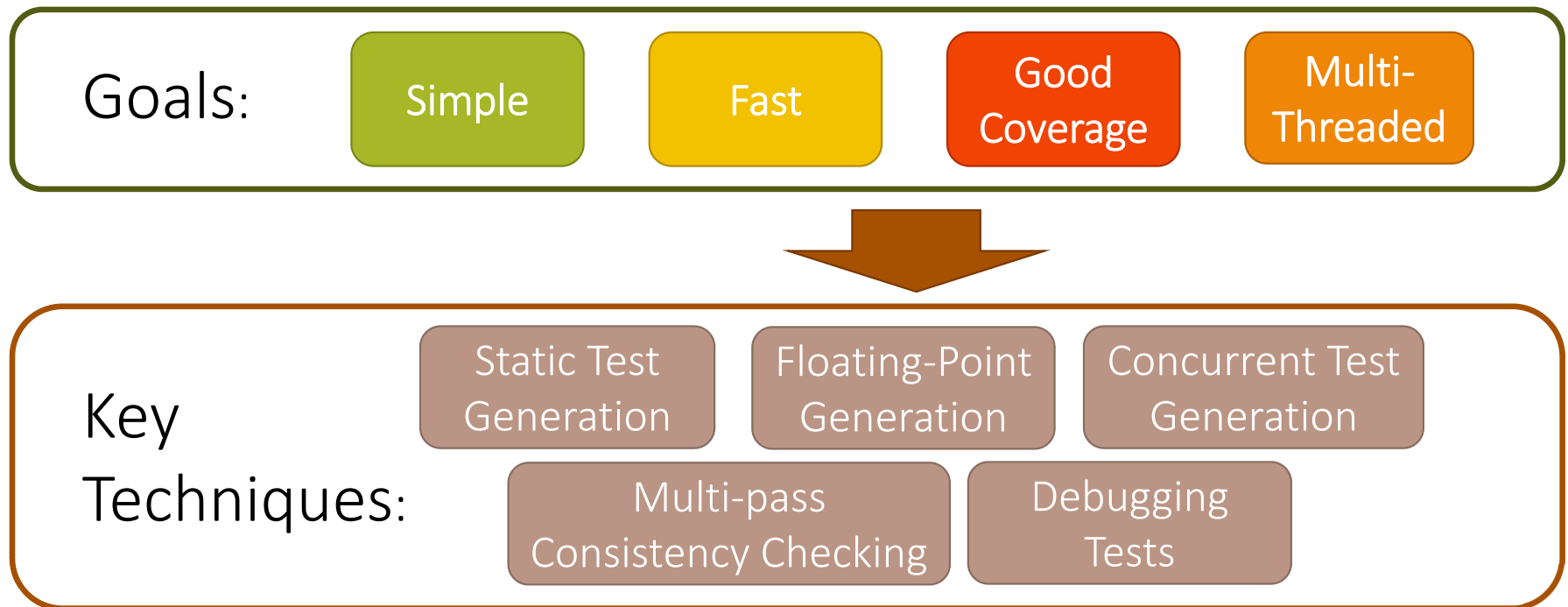
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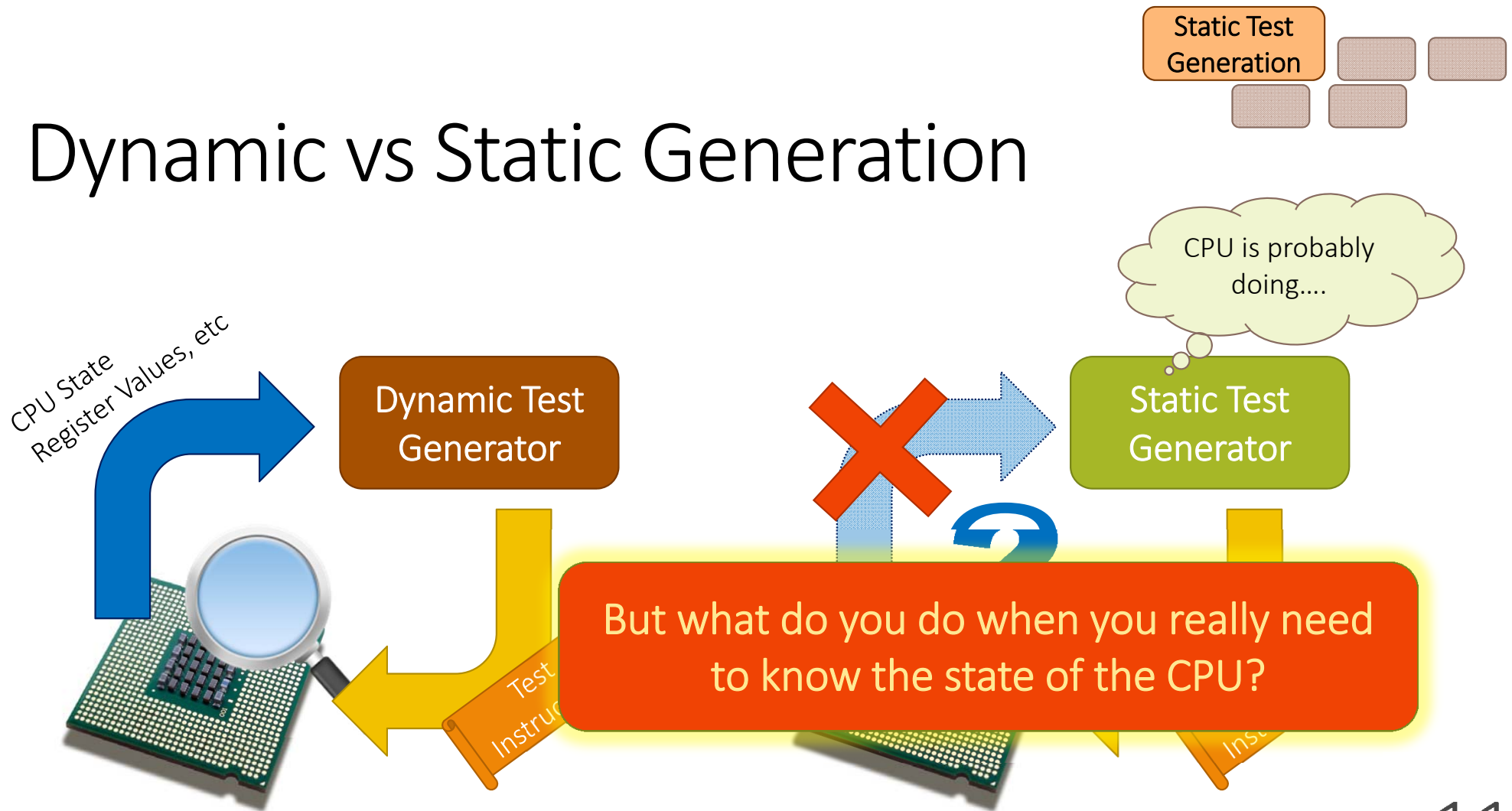
Questions

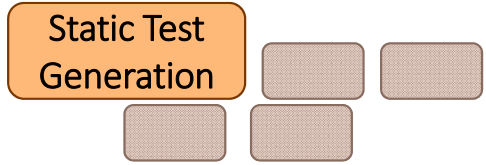
Debate!

Threadmill Design



Dynamic vs Static Generation

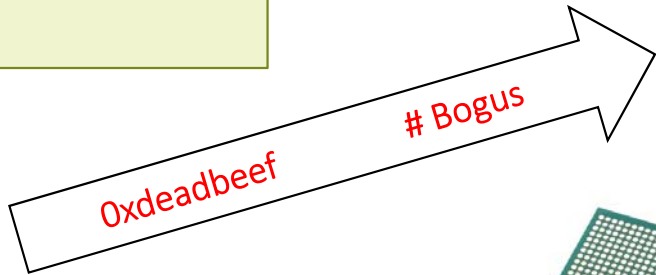




Observing Machine State

I want to send:
`beq $s0, $s1, exit` *# if (x==y)*
 but will it branch or not?
 What's \$s0? \$s1?

Threadmill



Instruction Stream

PC →

```

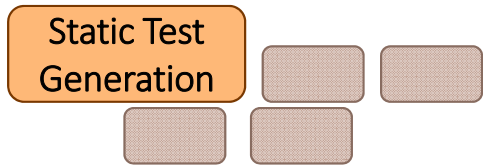
addi $t1, $t1, 1    # i = i+1
add $s0, $s0, $t1   # x = x+i
sub $s1, $s1, $t1   # y = y-i
  
```



uArch State

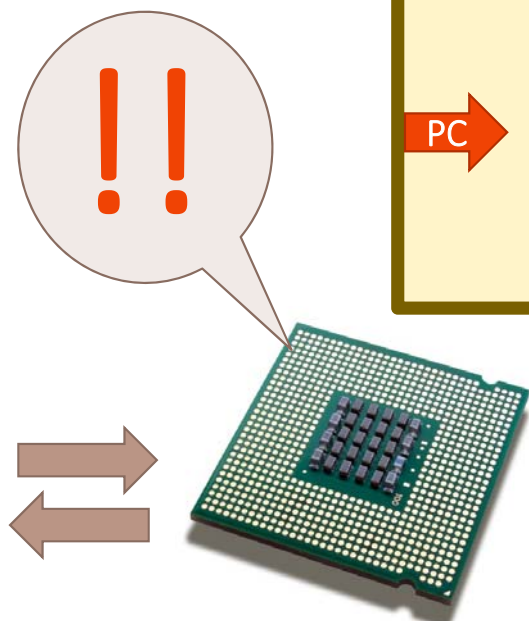
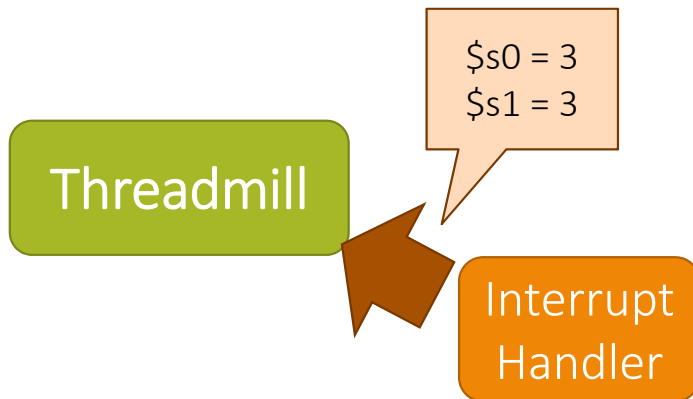
\$t1	7
\$s0	3
\$s1	3

Observing Machine State



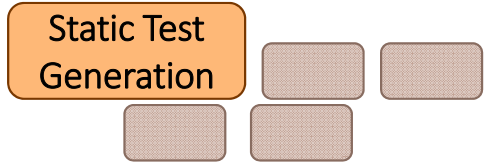
Instructions Executed

```
addi $t1, $t1, 1    # i = i+1
add $s0, $s0, $t1   # x = x+i
sub $s1, $s1, $t1   # y = y-i
PC → Oxdeadbeef     # Bogus
```



uArch State

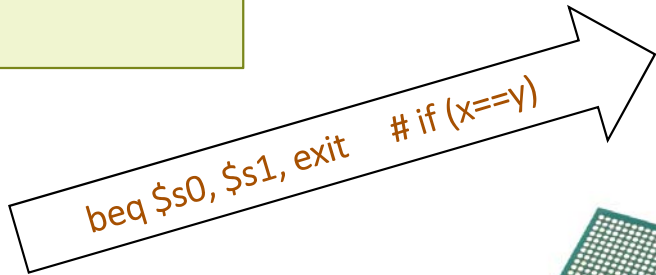
\$t1	7
\$s0	3
\$s1	3



Observing Machine State

Now I know \$s0=\$s1, so
`beq $s0, $s1, exit` # if (x==y)
 will branch to exit.

Threadmill



Instructions Executed

```

addi $t1, $t1, 1    # i = i+1
add $s0, $s0, $t1   # x = x+i
sub $s1, $s1, $t1   # y = y-i
beq $s0, $s1, exit  # if (x==y)
  
```

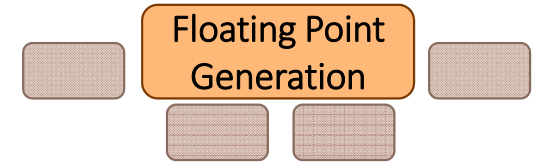
PC →



uArch State

\$t1	7
\$s0	3
\$s1	3

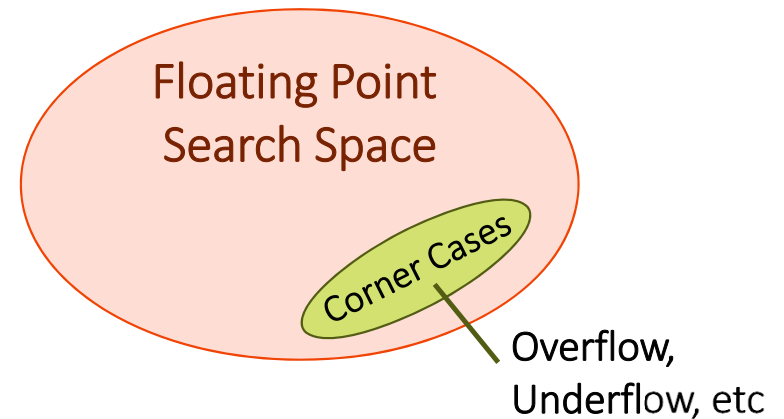
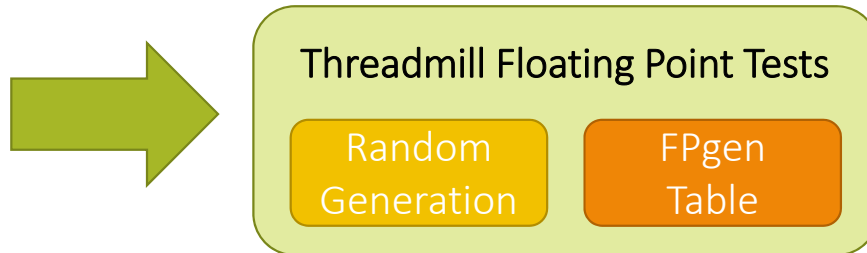
Floating-Point Instructions

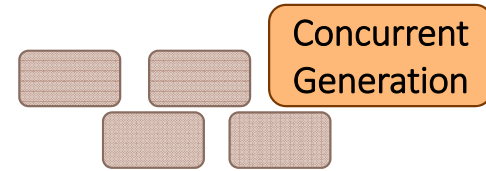


How to choose argument values?

random  inefficient

FPgen: Generate table of interesting test cases "off-line"





Concurrent Test Generation

`shared_addr = 0xBASE + random()`

Possible Collision Types

Write-Write

True Collision

Write-Read

False Collision

⋮

⋮

Need to be random, but consistent across all the test threads

~~Synchronization Techniques~~

Shared Random Seed

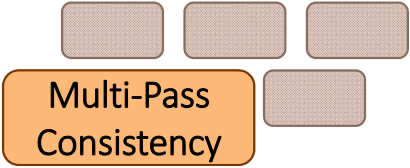
seed=42

Test Thread 0

Test Thread 1

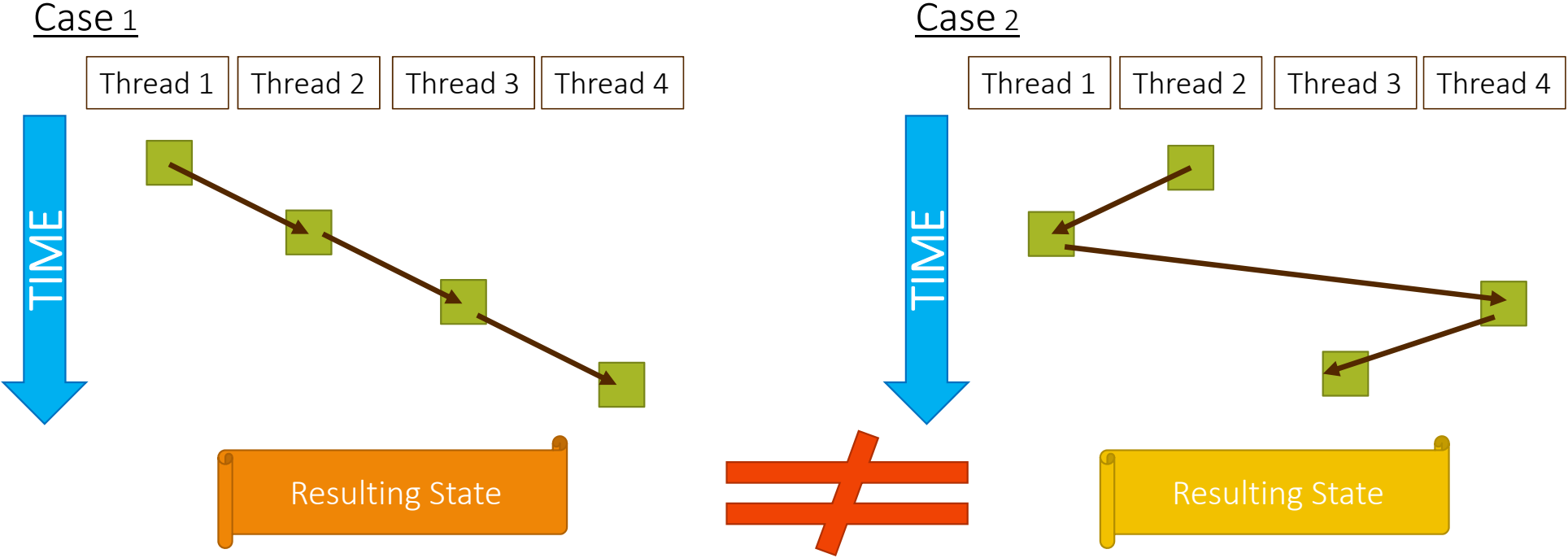
Test Thread 2

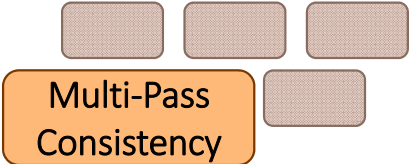
Test Thread 3



Multi-Pass Consistency Checking

Main Focus: Detecting Bugs in Multi-Threaded Consistency

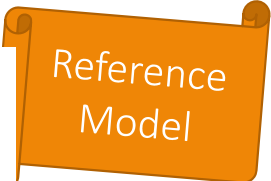
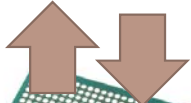
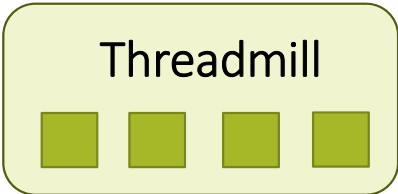




Multi-Pass Consistency Checking

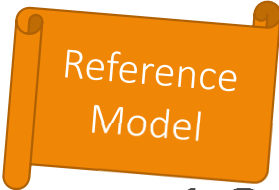
Main Focus: Detecting Bugs in Multi-Threaded Consistency

Execution 0



Registers,
Memory values, etc

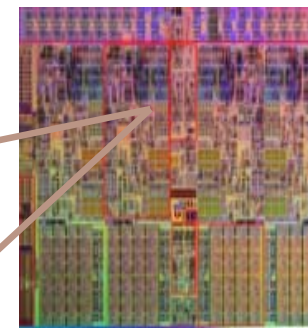
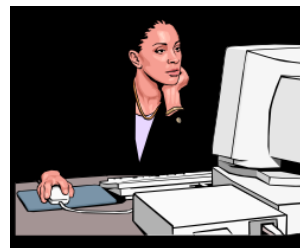
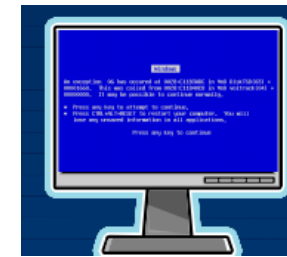
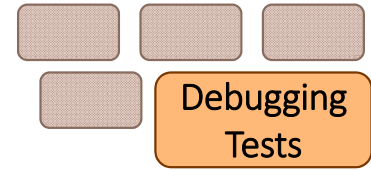
Execution i+1



Each execution can have different timing or order of operation, but should end with the same result.

Debugging Tests

- Restart the failed exerciser image a few test-cases before the failure
- Take the test-template that causes the bug and run it on a pre-silicon test generation



Conclusion

Strengths

- ✓ Fast and Light-weight.
- ✓ Automatic testing and checking of multi-threaded execution.

Weakness

- ❑ Doesn't check datapath or permanent bugs.
- ❑ Little evaluation of performance or coverage of the platform (paper).

Questions?

Debate

Threadmill's failure detection mechanism only checks for bugs in multi-threaded interactions, and do not check bugs in the datapath. Is this adequate?

Instead of generating tests on-chip, isn't it better to simply load pre-generated tests?

