Project Title: Robust Cache Coherence Protocol Verification with Inferno

Team Name: FLY-Bee

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Problem to be addressed:

Fault-tolerant architectures are emerging to guarantee reliable functionality on vulnerable silicon devices. For a fault-tolerant architecture, the RTL design is more complex than a normal one and is more likely to introduce design bugs.

Why does this problem matter?

Fault-tolerant architectures are popular in current circuits design industry. However, the verification of such a complex RTL design is a time consuming and costly task that is likely to become a bottleneck in the release of new architectures. Thus, finding an efficient way for debugging would speed up the verification process.

Idea/Solution to be investigated by the project:

This project will focus on the debugging process of a fault-tolerant directory-based 'MSI' protocol. We will also apply Inferno++ in our debugging process and evaluate this novel tool. To start with, the robust protocol proposed in 'A Systematic Methodology to Develop Resilient Cache Coherence Protocols' can be used to implement the resilient architecture. In the process of implementing the resilient architecture, we expect to run into several bugs. Both traditional debugging methods and Inferno++ will be used to locate bugs and their efficiency will be evaluated and compared in a systematic way. In our case, the efficiency of inferno++ will be evaluated based on its ability of locating bugs. Our analysis should provide a reference for future verification process of complex designs.

Plan to develop the project:

We plan to develop an architecture as in Figure 1.
The architecture is composed of three processors with L1 cache, one shared Directory & Memory and four routers. We intend to use the microprocessor core and its corresponding L1 cache from Sijia & Xiaoming's EECS 470 project which uses a 'MESI'-based cache controller. First we will modify their design to create a basic 'MSI'-based cache controller. In addition, we plan to use the RTL model of a router design from Booksim and deploy it in our project. Then we will add basic 'robust' features. The subsequent debugging process will be recorded in our document.

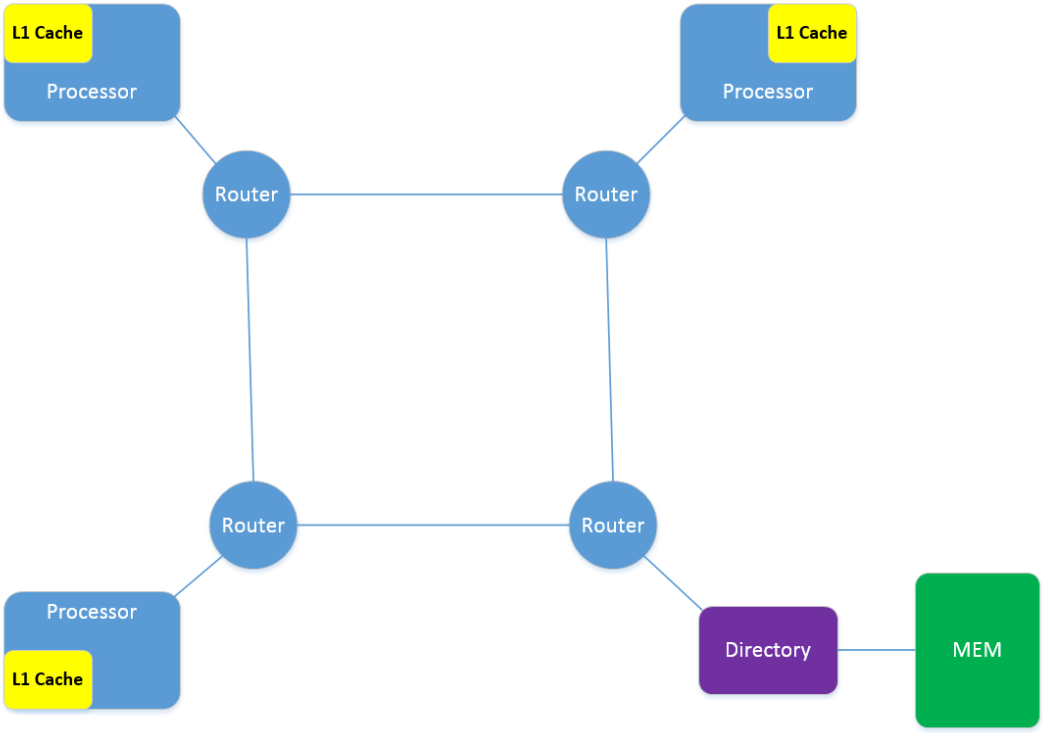

Figure.1. Proposed Multi-core Network for Design

Plan to evaluate the project's result:

In the debugging process, the number of bugs, the type of bugs, the way to locate the bugs and the hours for locating each bug will be recorded in a LOG file. The efficiency of Inferno++ will be evaluated by the number of bugs it is able to locate and the time it costs for locating bugs compared to a traditional approach.

Timeline:

Baseline integration:	10/10/2015 - 10/25/2015
Robust Protocol Deployment:	10/26/2015 - 11/08/2015
Verification with Inferno and normal way	11/09/2015 - 11/30/2015
Developing test stimulus	12/01/2015 - 12/04/2015
Documenting all the bugs	12/05/2015 - 12/10/2015
Report & Presentation Preparation	12/11/2015 - 12/15/2015