3D Fabric for Multicore Resilient Systems

The Master and PhDs

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Technological trends into the nanometer regime have led to significantly higher failure rates. Consequently, high reliability and fault tolerance are now getting more emphasis. We are attempting to solve these issues of reliability and tolerance on a simple pipeline, generally using in many-core designs and GPUs. We have based our work on StageNet[1], which uses a reconfigurable and adaptable network of replicated and isolated processor pipeline stages to maximize the useful lifetime of a chip. Replacing the direct connections at each pipeline stage boundary by a crossbar switch interconnection would form this network.

OUR IDEA

We are using 3D circuits to deal with these issues. By taking advantage of the third dimension, we can place more units in shorter distance with each other in different layers and make the communication latency between them minimum by connecting them vertically using Through Silicon Vias (TSVs).

PROGRESS

The baseline 2D-StageNet architecture has been implemented and simulated to verify its functionality. We have created the RTL for our top module, 4-core processor with all the crossbar switches connecting all stages of the cores. This RTL model can be used for both 2D and 3D-StageNet. In 2D, the regular crossbar would work as the connection between different cores and in 3D it would be replaced by the TSV delays.

We used the core layout to create the layout for 4-core 2D structure. By doing this, we were able to create the layout for switch bars and measure the delay and frequency of having 2D-switch structure in which this design would work.

To make sure that aforementioned steps have done successfully and also to simulate the delay and failure scenarios in the future, we tried to run the post synthesis and layout simulation. One of the problems that we have been facing in almost all the steps is to adapt the design, script and testbenches to our new libraries as we couldn't use the original ones from 470 course. We have been able to proceed to layout step to have a realistic estimation and condition of connections. We are still facing some issues in this step as our post synthesis and layout functional simulations are not working.

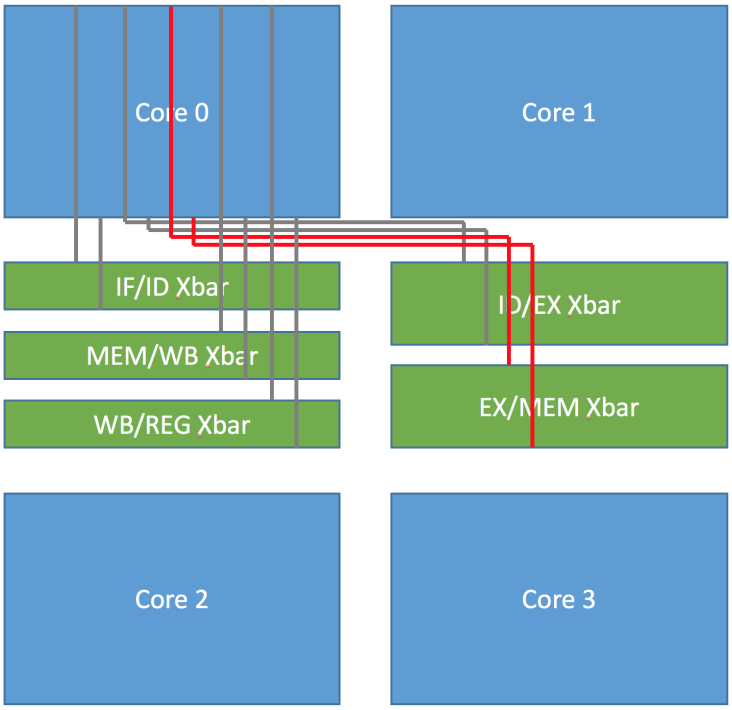
With the estimated routing distance in 2D structure and TSV parameters, SPICE simulation has been performed. The signal delay between each stage to crossbar is measured and reduced from 950 ps in 2D to 50 ps 3D.

FUTURE STEPS

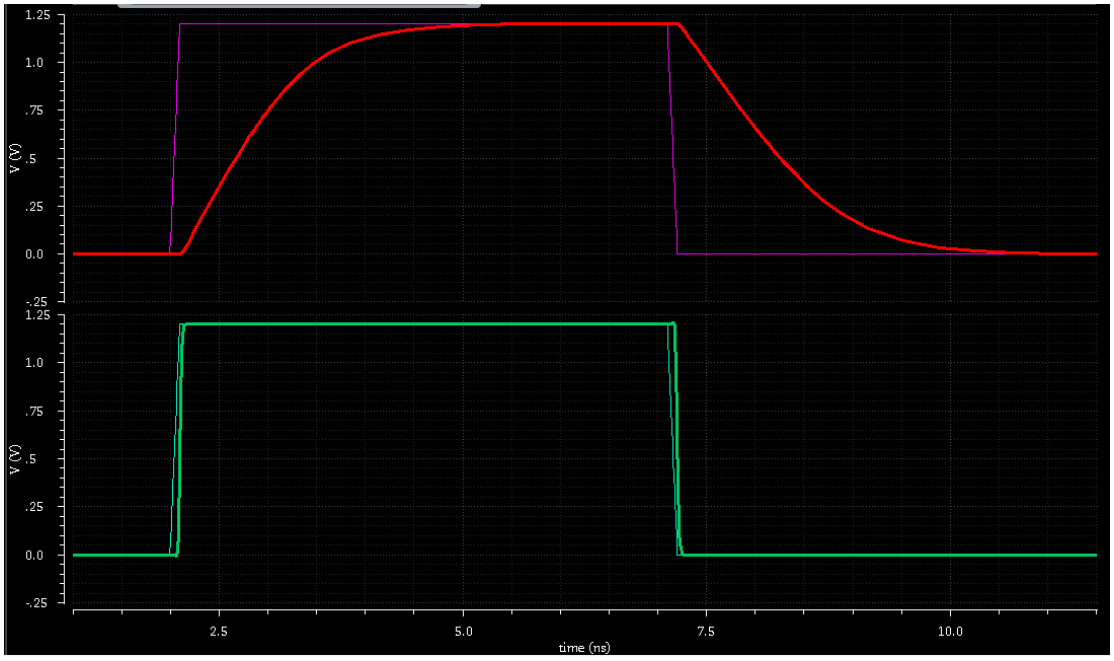
In order to simulate an accurate frequency and delay, we need to have correctly simulated layouts (by running post-layout and post-synthesis functional simulations). Once we have that, we would proceed with integrating the TSV delays in 3D structure. If this doesn't work, we have a Plan B. We would do an

RTL simulation rather than post-layout simulation for both the designs along with the switches and TSVs that has been modeled via spice simulations.

We plan to make the layout for our 4 cores, to be used for both 2D and 3D design and simulations.



2D structure and its critical path



SPICE simulation

(Top) 2D-Metal line delay: ~ 950 ps, (Bottom) 3D-TSV delay: ~ 50 ps