3D Fabric for Multicore Resilient Systems

The Master and PhDs

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Technological trends into the nanometer regime have led to significantly higher failure rates. Consequently, high reliability and fault tolerance are now getting more emphasis in the mainstream desktop, clamshell and mobile market. In an effort to assuage these concerns, there has been a shift towards multi-core and GPU inspired designs that use simple cores.

WHY IT MATTERS

There are many existing solutions for this, such as dual/triple modular redundancy, DIVA, Bulletproof, etc. Another work, StageNet[1], uses a reconfigurable and adaptable network of replicated and isolated processor pipeline stages to maximize the useful lifetime of a chip. The network is formed by replacing the direct connections at each pipeline stage boundary by a crossbar switch interconnection. This structure is shown in Figure 1.

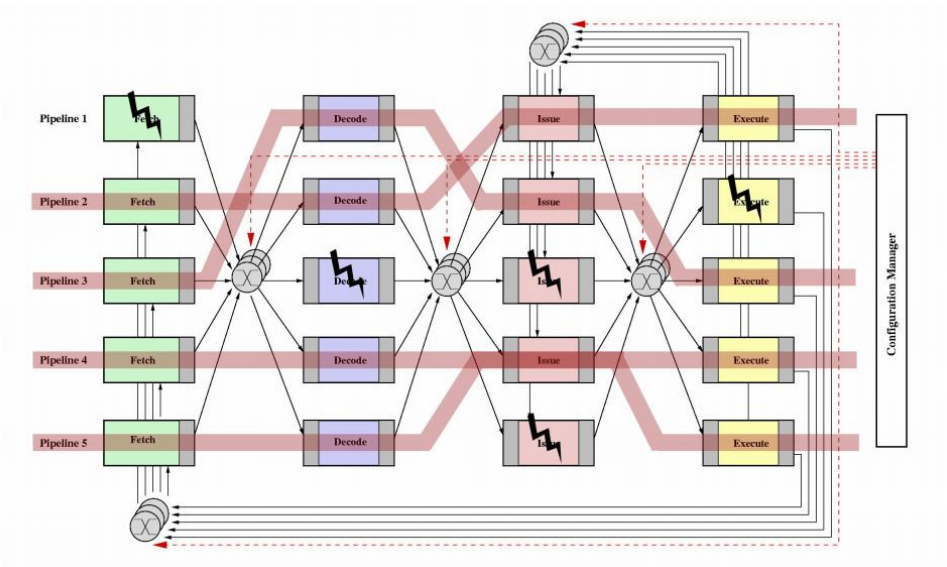

Figure 1: A 4 stage pipeline structure with 5 StageNet units and switches between stages [1]

But, this leads to high communication latency and low communication bandwidth between stages. Specifically, if the complexity of the processor and consequently the area of each unit increases or more number of parallel units (e.g. 8 parallel units instead of 4) is targeted, the communication latency will become a huge challenge.

OUR IDEA

We propose to use 3D circuits to deal with these issues. By taking advantage of the third dimension, we can place more units in shorter distance with each other in different layers and make the communication latency between them minimum by connecting them vertically using Through Silicon Vias (TSVs).

INFRASTRUCTURE

We plan to use EECS 470 Project 3 infrastructure which implements a conventional 5-stage pipeline architecture. It is a simple in-order core similar to the commercially available embedded processors. TSVs must also be modeled and simulated to be used in this project too.

EVALUATION

The results will be evaluated using verilog simulations. SPICE simulations can be done for the estimation of latencies of the TSVs. TSVs can also be modeled as component with data obtained from literature [2]. Comparing the performance of the 3D processor with the same processor in 2D integration in terms of performance, reliability and power and cost. We can measure speed, power and area.

TIMELINE

23rd October	Modify the verilog for the simple core. Implement crossbar or any switch. Partial implementation of 2D StageNet.
30th October	Implement 2D StageNet. Model TSV and extract its latency and area
13th November	Implement 3D StageNet and other designs if needed
27th November	Verilog simulations for both designs.
4th December	Debugging of designs.
10th December	Simulations and report.

REFERENCES

[1] Gupta, Shantanu, et al. "The stagenet fabric for constructing resilient multicore systems." *Proceedings of the 41st annual IEEE/ACM International Symposium on Microarchitecture*. IEEE Computer Society, 2008.

[2] Giridhar, Bharan, et al. "Exploring DRAM organizations for energy-efficient and resilient exascale memories." *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis*. ACM, 2013.