MaPnet: A Three-Dimensional Fabric for Reliable Multi-core Processors

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Introduction

• Reliability is a big concern in Multi-core Processors as the technology nodes are scaling
• Inter-Core resource sharing increases reliability in presence of fault (e.g. StageNet Architecture)
• This leads to high communication delay
• 3D integration is a promising solution to increase density and performance

Objective

• Use StageNet based structure with two functionalities in case of failure
  – Arranging healthy resources in different cores to create one healthy pipeline (Virtual Pipeline)
  – Sharing healthy resources in other cores when they are not being used
• Use 3D integration to reduce communication delay and hence improve performance over 2D design
• Model Through-Silicon Vias (TSV) to simulate the 3D design and performance

Architecture

• MaPnet: Using inter-core redundancy to salvage the processor in case of faults.
  – 2D design
  – Core-based 3D design
  – Pipeline-based 3D design

Implementation

• MaPnet design is implemented on a 4-core architecture with simple cores
• TSV delay and behavior is simulated by SPICE simulations and used to determine routing delay and processor frequency

Results

• Each fault forces the processor to reconfigure and adds extra delays cycles into pipeline structure to use resources in other cores
• We simulated a single core for different test cases and measured the IPC for extra delay cycles added in pipeline structure which is reflected in Figure 7.

Single Pipeline Performance

• IPC was measured for each scenario
• Figures 8 reflect the results for baseline 2D and 3D pipelined structures regarding sharing the same resource and no sharing.

Conclusion

• Improvement with 2D and 3D StageNet compared 2 baseline
• 16.3% on average and up to 28.2% improvement in 3D compared to 2D
• area of our 3D design is under than 25% of the traditional 2D design due to reduced interconnection complexity.