MaPnet: A Three-Dimensional Fabric for Reliable Multi-core Processors

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Introduction

- Reliability is a big concern in Multi-core Processors as the technology nodes are scaling
- Inter-Core resource sharing increases reliability in presence of fault (e.g. StageNet Architecture)
- This leads to high communication delay
- 3D integration is a promising solution to increase density and performance

Objective

- Use StageNet based structure with two functionalities in case of failure
  - ✓ Arranging healthy resources in different cores to create one healthy pipeline (Virtual Pipeline)
  - ✓ Sharing healthy resources in other cores when they are not being used
- Use 3D integration to reduce communication delay and hence improve performance over 2D design
- Model Through-Silicon Vias (TSV) to simulate the 3D design and performance

Architecture

- MaPnet: Using inter-core redundancy to salvage the processor in case of faults.
  - ✓ 2D design
  - ✓ Core-based 3D design
  - ✓ Pipeline-based 3D design

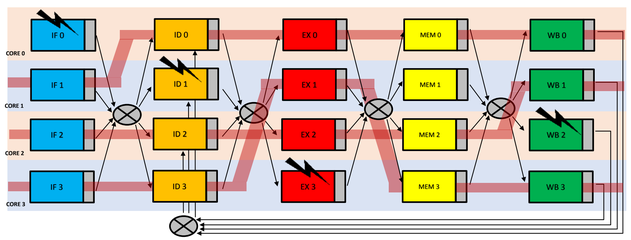
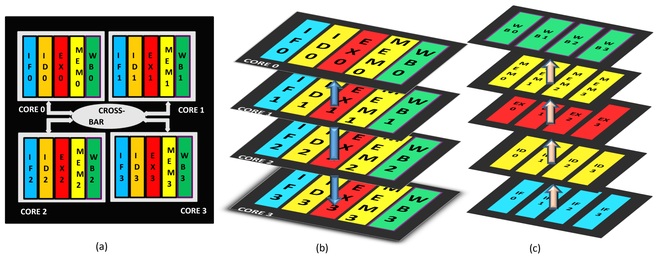


Figure 1. A 5-satge pipeline structure for 4 cores and switches between stages



(a) (b) (c)

Figure 2. Three different designs for MAPnet (a) 2D structure with crossbars (b) Core-based 3D structure (c) Pipeline-based 3D structure

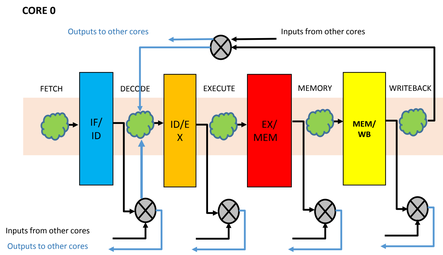


Figure 3. Single core architecture with connection to crossbar and pipeline registers

Table 1. Advantages and disadvantages of each design

	Advantages	Disadvantages
Regular Design	-Easy To Design	-Slow -Low Scalability
Pipelined Design	-Higher clock Frequency -Easy Dynamic Reconfiguration -High Flexibility in Sharing Resources -Better scalability	-Difficult to Design -Need extra control units -Area Overhead

Implementation

- MAPnet design is implemented on a 4-core architecture with simple cores
- TSV delay and behavior is simulated by SPICE simulations and used to determine routing delay and processor frequency

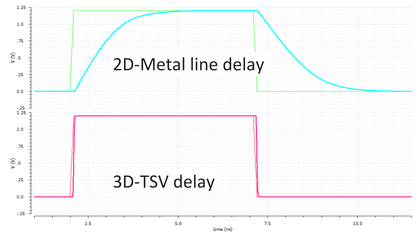
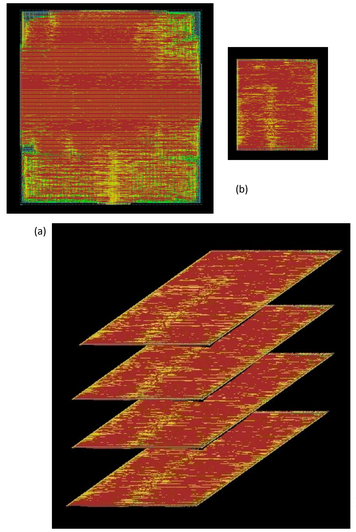


Figure 4. Comparison between routing delay for 2D Metal vs 3D TSVs

- Both 3D designs show performance improvement over the 2D design
- The throughput increases by 1.74X
- On comparing the post-APR frequencies in faulty and healthy cores and considering Table 1, we decided to pipeline both architectures to reduce clock frequency
- Crossbars in 2D and 3D structures need 1 and 2 pipeline stages respectively.
- The RTL was synthesized using Synopsys Design Compiler and Cadence Encounter was used to create the layout

Table 2. Clock Period results after Place and Route (using Encounter)

MAPnet Design	2D	Core-based 3D	Pipeline 3D
Clock (No Fault)	2.5 ns (400 MHz)	2.5 ns (400 MHz)	2.5 ns (400 MHz)
Clock (Fault Condition)	7 ns (143 MHz)	3.95 ns (250MHz)	3.85 (260MHz)
Footprint Area	1200*1200 sq.us	600*600 sq. us	
Layout Density	71%	67%	



(a) (b) (c)

Figure 5. Layouts for (a) 2D 4-core processor, (b) Basic 1-core and (c) Conceptual 3D 4-core Design

- 3D architectures have performance advantage in many core designs (Figure 6)

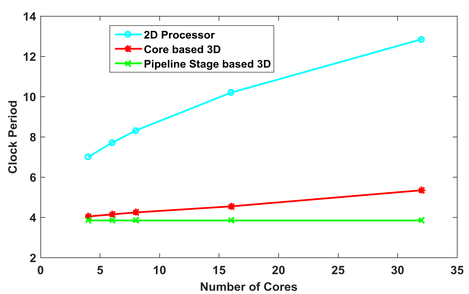


Figure 6. Estimated Clock Period for different number of cores for MAPnet – (a) 2D structure with crossbars (b) Core-based 3D structure (c) Pipeline-based 3D structure

Results

- Each fault forces the processor to reconfigure and adds extra delays cycles into pipeline structure to use resources in other cores
- We simulated a single core for different test cases and measured the IPC for extra delay cycles added in pipeline structure which is reflected in Figure 7.

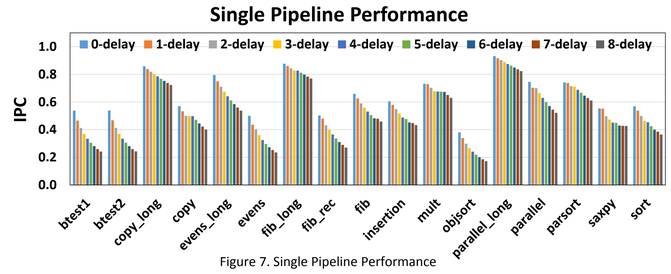


Figure 7. Single Pipeline Performance

- IPC was measured for each scenario
- Figures 8 reflect the results for baseline 2D and 3D pipelined structures regarding sharing the same resource and no sharing.

Table 3. shows 3 different fault scenarios for various fault numbers and locations within pipeline stages

Scenario	Number of Faults	Disabled Resources
Scenario 1	2	IF0, EX1
Scenario 2	4	IF0, ID1, EX2, WB3
Scenario 3	10	IF0, ID1, EX0, MEM1, WB0, IF2, ID3, EX2, MEM3, WB2

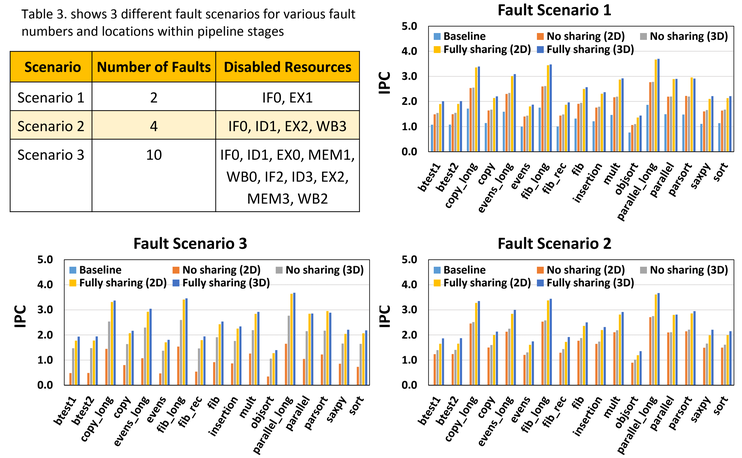


Figure 8. IPC for different fault scenarios

- Improvement with 2D and 3D StageNet compared 2 baseline
- 16.3% on average and up to 28.2% improvement in 3D compared to 2D
- area of our 3D design is under than 25% of the traditional 2D design due to reduced interconnection complexity.

Conclusion

- 3D reconfigurable pipeline design, named MaPNet.
- more-reliable operation, higher performance, lower cost, and/or lower power consumption by taking advantage of the redundancy and capabilities available at each layer in the system stack.