EECS 579: Memory Testing

Recap: Processor Testing

- Complexity requires high-level, functional testing methods
- Fault models not well defined
- Practical tests tend to be heuristic:
  - **CPU**: Bootstrap testing to exercise all circuits and instructions
  - **Memory**: Special, regular exercising tests
  - **I/O Circuits**: Similar to memory tests, with loopback
- Programmable systems such as microcontrollers are tested by (diagnostic) programs
- Intellectual property (IP) cores are especially hard to test

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**Computer Memory System**

```
CPU
  Register file
  IC 1 (microprocessor)

Cache (level 1) → Cache (level 2) → Main memory → Secondary memory

ICs 2m
ICsm

Hard disks, etc.
```
SRAM and RAM Cells

(a)

(b)

DRAM Access Circuitry

Address decoder

Word line \( L = 1 \)

Storage cell

Bit line \( L \)

Disabled input (drive) amplifier

Enabled output (sense) amplifier

Input-output data bus \( B \)
**DRAM Technology Development**

- 1970: First commercial DRAM introduced by Intel at 1024 b = 1 Kbit
- 1984: Apple Macintosh 1 personal computer introduced with a multichip 128-Kbyte RAM

![Graph showing the number of memory cells per chip over the years](image)

**Testing Time for n-bit RAM**

<table>
<thead>
<tr>
<th>Size</th>
<th>Number of Test Algorithm Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$n$</td>
</tr>
<tr>
<td>1 Mb</td>
<td>0.06</td>
</tr>
<tr>
<td>4 Mb</td>
<td>0.25</td>
</tr>
<tr>
<td>16 Mb</td>
<td>1.01</td>
</tr>
<tr>
<td>64 Mb</td>
<td>4.03</td>
</tr>
<tr>
<td>256 Mb</td>
<td>16.11</td>
</tr>
<tr>
<td>1 Gb</td>
<td>64.43</td>
</tr>
<tr>
<td>2 Gb</td>
<td>128.9</td>
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</tbody>
</table>
**IC Fault Types**

**Permanent Faults**
- Missing/added electrical connection
- Broken component (IC mask defect or silicon-to-metal connection)
- Burnt-out chip wire
- Corroded connection between chip and package

**Intermittent Faults**
- Loose connections
- Aging components (changed logic delays)
- Hazards and races in critical timing paths (bad design)
- Resistor, capacitor, inductor variances (timing faults)
- Physical irregularities (narrow wire -- high resistance)
- Electrical noise (memory state changes)

**IC Fault Types**

**Transient Faults**
- Cosmic rays
- α particles (ionized Helium atom)
- Air pollution (causes wire short/open)
- Humidity (temporary short)
- Temperature (temporary logic error)
- Pressure and vibration (temporary wire open/short)
- Power supply fluctuation (logic error)
- Electromagnetic interference (signal coupling)
- Static electrical discharge (change state)
- Ground loop (misinterpreted logic value)
**RAM Tests**

**Requirements**
- Good fault coverage
- Easy to program in ATE
- Reasonable test complexity (application time)

**Standard Tests**
- **Checkerboard Test:** basic test that writes 0's and 1's into alternating cells. Complexity is $O(n)$ in terms of the number of reads and writes

- **Walk/March Tests:** write 0 (1) on background of 1s (0s), then read and verify the test cell; “walk/march” the test 0 (1) through the memory. Complexity is $O(n)$

- **Galloping Tests:** write 0 (1) on background of 1s (0s), then read all cells; move 0 (1) through the memory. Complexity is $O(n^2)$, which is generally impractical now.

  Many variants of the above tests exist.

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**Checkerboard Test**

<table>
<thead>
<tr>
<th>Write 1 (0) in every even (odd) address cell</th>
</tr>
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<tbody>
<tr>
<td>Pause for refresh. Read and verify every cell.</td>
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</tbody>
</table>

**No. of R/W steps**

<table>
<thead>
<tr>
<th>Storage array</th>
<th>Sense amplifiers</th>
<th>Storage array</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>n</td>
<td>n</td>
</tr>
<tr>
<td>Total: 4n</td>
<td></td>
<td>n</td>
</tr>
</tbody>
</table>
Standard RAM Tests

Walking 0s/1s Test

Write 0 every cell.
For i = 0 to n – 1 do {
    Write 1 in test cell C_i;
    Read and verify C_i;
    Write 0 in C_i;
    i := i + 1;
}

No. steps

\[ n \times n \]

Repeat with 0 and 1 switched: Total no. steps: 8n

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<thead>
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Standard RAM Tests

March Test Notation

- r  Read a memory location
- w  Write a memory location
- r0 Read a 0 from a memory location
- r1 Read a 1 from a memory location
- w0 Write a 0 to a memory location
- w1 Write a 1 to a memory location
- ↑  Write a 1 to a cell containing 0
- ↓  Write a 0 to a cell containing 1
- ‹  Complement the cell contents
- ‹‹ Increasing memory addressing
- †  Decreasing memory addressing
- †† Either increasing or decreasing
March Test Example

MATS+ Algorithm

M0: {March element \(\uparrow(w_0)\)}
for cell := 0 to n – 1 (or any other order) do
   write 0 to A[cell];
M1: {March element \(\uparrow(r_0, w_1)\)}
for cell := 0 to n – 1 do
   read A[cell]; {Expected value = 0}
   write 1 to A[cell];
M2: {March element \(\downarrow(r_1, w_0)\)}
for cell := 0 to n – 1 down to 0 do
   read A[cell]; {Expected value = 1}
   write 0 to A[cell];
end;

Memory Functional Faults

- Cell stuck
- Read/write line stuck
- Data line stuck
- Short circuit between data lines
- Address line stuck
- Shorts between address lines
- Wrong address access
- Cell can be set to 0 but not to 1 (or vice versa)
- Pattern sensitive cell interaction

Reduced Set
- Stuck-at faults
- Transition faults
- Coupling faults
- Neighborhood pattern sensitive faults
Memory Functional Faults

Stuck-at Faults

(a) State diagram of a good cell.

(b) SA0 fault.  (c) SA1 fault.
Memory Testing Summary

- Multiple fault models are essential
- Combinations of tests are essential:
  - March tests: SRAMs and DRAMs
  - NPSF tests: DRAMs
  - DC parametric tests: Both
  - AC parametric tests: Both
- Inductive fault analysis is now desirable