Permanent vs. Temporal Defects

- **Permanent defects**
  - The faulty behavior lasts forever.
  - For example, a metal residue connects a gate input and VDD. (stuck-at 1 fault)
- **Temporal defects**
  - The faulty behavior lasts for a finite time $T$.
  - If $T$ is greater than the specified threshold, the temporal defects make the circuit under test fail to operate in the designed time.
  - Temporal defects are usually revealed as a longer delay of a gate or a path.
Growing Importance of Delay Fault Testing

- Integrated circuit technology trends
  - Increasing circuit speeds
    - 2 GHz Pentium4 = 0.5 ns clock cycle
  - Narrowing process feature size
    - 0.3 μm ASIC process; 0.1x μm DRAM process

- Imperfect manufacturing process
  - Defect mechanisms increasing circuit delays
    - Process variations - e.g. decreased interconnection wire width
    - Spot defects - e.g. spot laid on a interconnection wire
  - Such defects could be more dominant in future

Delay Faults

- Defects resulting in slow 0 → 1 or 1 → 0 signal changes so that the circuit under test cannot operate in the specified rate.

- Sources
  - Stray capacitive loads
  - Narrow interconnects
  - Poor connections
  - Threshold voltage shift
  - Incorrect doping density
Delay Fault Models

- Basic models
  - Gate delay fault model
    - A lumped delay fault associated with a gate.
    - Assumption: a gate delay becomes large enough to make a circuit fail to operate in the specified rate.
  - Path delay fault model
    - A distributed delay fault associated with a path.
    - Realistic fault model.

- Other models
  - Many of them are variants of the path delay fault model.

Path Delay Faults

- A path is an alternating sequence of lines and gates from a primary input or a clocked flipflop to a primary output or a clocked flipflop.
- A path delay fault associated with a path $p$ causes an excessive delay when a signal transition propagates through $p$.
- Two path delay faults are associated with $p$ depending on the transition direction at the path input (slow-to-rise $\uparrow p$ and slow-to-fall $\downarrow p$).
An Example

- A sequence \( t = \langle a' b', a b' \rangle \) of input patterns propagates a rising transition through path \( adz \).
- That is, \( t \) detects a slow-to-rise fault \( f = \uparrow adz \).

Path Delay Tests

- On- and off-path inputs
  - Consider a gate \( G \) on the path \( p \) of interest. An input \( i \) of \( G \) is an on-path input of \( p \) if \( i \) is on \( p \); otherwise \( i \) is an off-path input.

- Static sensitization
  - A vector \( v \) static sensitizes a path \( p \) if \( v \) sets all off-path inputs of \( p \) to non-controlling values.

- Tests for path delay faults
  - A test \( t = \langle v_1, v_2 \rangle \) for a path delay fault \( f = \uparrow p \downarrow p \) is a sequence of two input patterns where \( v_2 \) static sensitizes \( p \) and \( t \) initiates and propagates the desired transition along \( p \).
Revisiting Example

\[ t = \langle v_1, v_2 \rangle \text{ where } v_1 = \overline{a'b} \text{ and } v_2 = ab' \]

\( v_2 \) static sensitizes path \( adz \)

Path Delay Tests: Classifications

- Robust (path delay) test
  - A robust test \( t_R \) detects a fault \( f_R \) independent of the delays in the rest of the circuit under test; \( f_R \) is called a robust (path) delay fault.

- Non-robust (path delay) test
  - A non-robust test \( t_{NR} \) detects a fault \( f_{NR} \) when no other path delay fault is present; \( f_{NR} \) is called a non-robust delay fault.
Example

Is $t = <ab', ab>$ a robust or non-robust test for $f = \uparrow bcez$?

Example

Is $t = <a'b', ab'>$ robust or non-robust?
Path Delay Tests

Observations

- Signal changes produce glitches (hazards) that interact with faults in complex ways that are impractical to deal with.
- A robust test does not incur hazards while a non-robust test does.
- Some path delay faults cannot be tested.
  - E.g. $\downarrow acdz$ and $\downarrow bcez$.

Challenges

- **Huge number of faults in practical circuits**
  - The number of paths in a logic circuit can be very huge.
    - e.g. The ISCAS85 c6288 benchmark, a 16X16-bit multiplier has $1.98 \times 10^{20}$ paths.
  - Very long automatic test pattern generation (ATPG) time.
  - Need large memory space to store detected and undetected faults for both ATPG and fault simulation.
  - Often path delay testing is limited to the (near) critical paths.
Test Application

- General hardware model and clock timings
  - Every line in the circuit under test (CUT) must be stable by initialization vector $v_1$ before test vector $v_2$ is applied.

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Test Methodologies

- Slow-clock combinational test
  - Input and output latches are independently clocked.
  - Input and output latches can be either part of the circuit or provided by the automatic test equipment (ATE).
  - Useful when the ATE is slower than the circuit under test.
Test Methodologies

- Normal-scan sequential test
  - In test $t = \langle v_1, v_2 \rangle$, $v_1$ is scanned in in normal fashion.
  - $v_2$ is applied either by a 1-bit shift of the scan register or by propagation through the preceding combinational logic.

![Diagram of normal-scan sequential test]

- Enhanced-scan sequential test
  - A special register is used in the scan path to hold $v_1$ while $v_2$ is scanned in so that arbitrary $\langle v_1, v_2 \rangle$ delay tests can be applied.

![Diagram of enhanced-scan sequential test]