EECS598: Nanoelectronics

Introduction

01/09/2007

Topics covered in this course:

•Transport in semiconductors and device performance from a more physical perspective.

(*for a more technical, system designer-oriented discussion on CMOS, including fabrication techniques, EECS523 is recommended*).

•Challenges and technological innovations to sustain the historical scaling trend of MOSFET

- Technology "boosters" (high-k, metal gate, mobility enhancement, ballistic enhancement)
- Non-conventional CMOS structures (UTB FD, DG)

•Emerging technologies beyond MOSFET
(single-electron devices, 1D structures, molecular devices, spin based devices, new nanoarchitectures).

Prerequisite: EECS421 or permission by instructor.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2005 EDITION

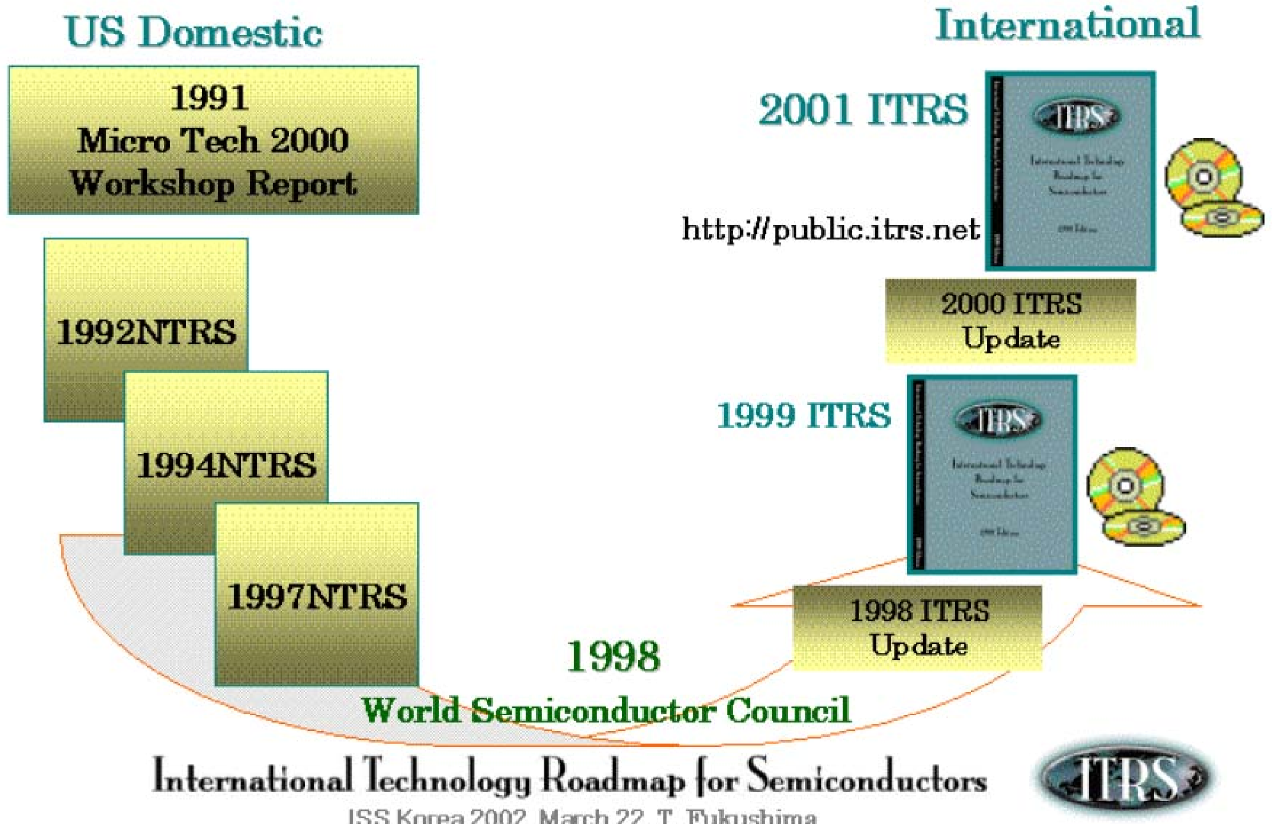
December, 2005

"… predicts the main trends in the semiconductor industry spanning across 15 years into the future." (2005-2020)

•8 years in the nearest future (up to 2013) as the Near Term
•subsequent 7 years (up to 2020) as the Long Term

Updated version, December, 2006

http://www.itrs.net/links/2006Update/2006UpdateFinal.htm



http://public.itrs.net/

- Coordinated by The Semiconductor Industry Association (SIA)
- Published every two years
- Reviewed (updated) every year

For the 2005 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- **Process Integration, Devices, and Structures**
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- **Emerging Research Devices / Emerging Research Materials**
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

http://www.itrs.net/Common/2005ITRS/Home2005.htm

Minor changes were made in the PIDS chapter, and no changes were made in the ERD chapter in the 2006 update

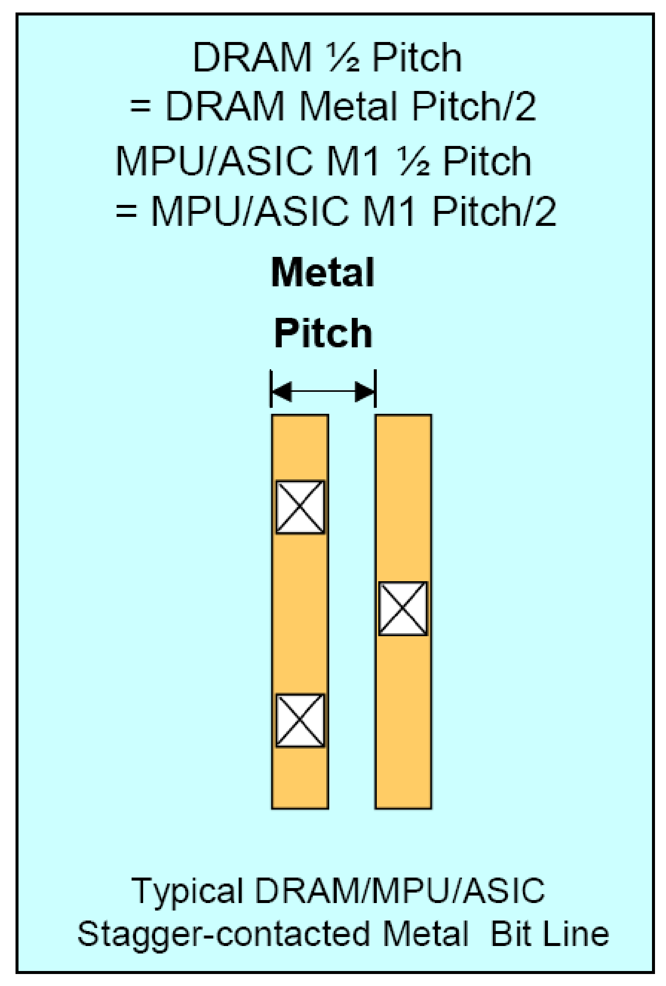
Major relevant changes in 2005/2006 ITRS:

- **A single-number technology node is no longer used (DRAM, MPU and Flash each has its own independent measure)**

- **Timing of a technology cycle may be different for a particular product.** ***Trend cycle: a period of time to achieve 0.71x size reduction per cycle (0.5x per two cycles). Measures packing density.***

- For MOSFET, figure of merit for scaling is the intrinsic speed $1/\tau$, (τ=CV/I, the intrinsic delay). Historical rate of increasing $1/\tau$ by 17% per year is targeted.

- Emphasis of emerging research devices, materials, architectures expected beyond CMOS scaling (year 2020?) (new ERD chapter)



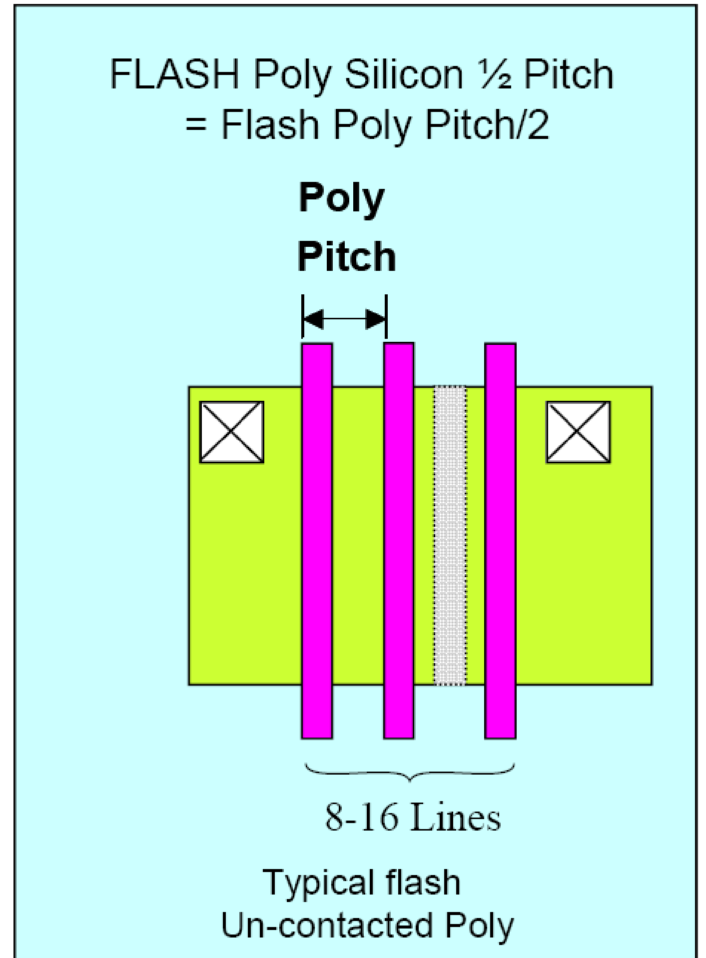


Figure 2 2005 Definition of Pitches

ITRS2005: Executive Summary

Major relevant changes in 2005/2006 ITRS:

- A single-number technology node is no longer used (DRAM, MPU and Flash each has its own independent measure)

- Timing of a technology cycle may be different for a particular product.
 Trend cycle: a period of time to achieve 0.71x size reduction per cycle (0.5x per two cycles).

- **For MOSFET, figure of merit for scaling is the intrinsic speed $1/\tau$, (τ=CV/I, the intrinsic delay). Historical rate of increasing $1/\tau$ by 17% per year is targeted.**

- Emphasis of emerging research devices, materials, architectures expected beyond CMOS scaling (year 2020?) (new ERD chapter)

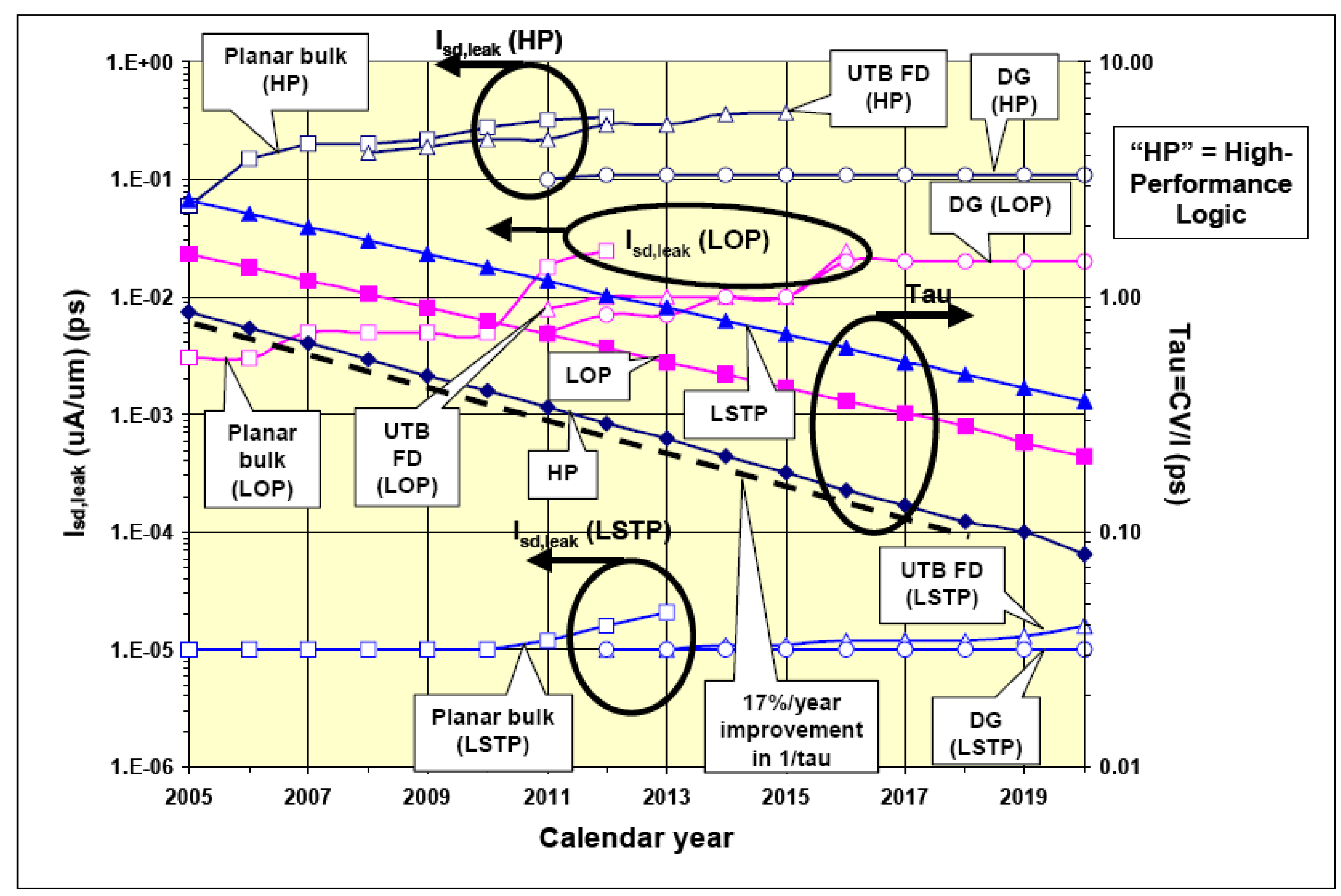


Figure 34 $\tau = CV/I$ and $I_{sd,leak}$ for All Logic Types.
(The dashed line represents the desired 17%/year transistor performance improvement.)

ITRS2005: Process Integration, Devices, and Structures (PIDS)

Table 40a High-Performance Logic Technology Requirements—Near-term UPDATED

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	L_g: Physical L_{gate} for High Performance logic (nm) [1]	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	**12**	**11**	**11**	**10**	**9**	**6.5**	**5**	**5**	
elete	UTB FD (Å)				~~9~~	~~8~~	**7**	**6**	**5**	**5**
	DG (Å)							**8**	**7**	**6**
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended Planar Bulk (Å)	**7.3**	**7.4**	**7.4**	**7.0**	**7.0**	**2.7**	**2.5**	**2.5**	
elete	UTB FD (Å)				4	4	**4**	**4**	**4**	**4**
	DG (Å)							**4**	**4**	**4**
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended Planar Bulk (Å)	**19.3**	**18.4**	**18.4**	**17.0**	**16.0**	**9.2**	**7.5**	**7.5**	
elete	UTB FD (Å)				~~13~~	~~12~~	**11**	**10**	**9**	**9**
	DG (Å)							**12**	**11**	**10**
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	**1.88E+02**	**5.36E+02**	**8.00E+02**	**1.18E+03**	**1.10E+03**	**1.56E+03**	**2.00E+03**	**2.43E+03**	
elete	UTB FD (A/cm^2)				~~7.73E+02~~	~~9.50E+02~~	**1.22E+03**	**1.38E+03**	**2.07E+03**	**2.23E+03**
	DG (A/cm^2)							**6.25E+02**	**7.86E+02**	**8.46E+02**
	V_{dd}: Power Supply Voltage (V) [6]	**1.1**	**1.1**	**1.1**	**1**	**1**	**1**	**1**	**0.9**	**0.9**

ITRS2006(update): Process Integration, Devices, and Structures (PIDS)

Table 40b High-Performance Logic Technology Requirements—Long-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	**11**	**10**	**9**	**8**	**7**	**6**	**5**
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	**5**	**5**					
DG (Å)	**6**	**6**	**5**	**5**	**5**	**5**	**5**
Gate Poly Depletion & Inversion-Layer Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	**4**	**4**					
DG (Å)	**4**	**4**	**4**	**4**	**4**	**4**	**4**
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]							
Extended Planar Bulk (Å)							
UTB FD (Å)	**9**	**9**					
DG (Å)	**10**	**10**	**9**	**9**	**9**	**9**	**9**

ITRS2005: Process Integration, Devices, and Structures (PIDS)

Table 39a Process Integration Difficult Challenges—Near-term

Difficult Challenges ≥ 32 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 32 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), stochastic doping variations, and difficulty in adequately controlling short channel effects. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs.
2. Implementation of high-κ gate dielectric and metal gate electrode in a timely manner **Delayed to 2010 (from 2008)**	High κ and metal gate electrode will be required beginning in ~2008. Timely implementation will involve dealing with numerous challenging issues, including appropriate tuning of metal gate work function, ensuring adequate channel mobility with high-κ, reducing the defects in high-κ to acceptable levels, ensuring reliability, and others.
3. Timely assurance for the reliability of multiple and rapid material, process, and structural changes	Multiple changes are projected over the next decade, such as.: Material: high-κ gate dielectric, metal gate electrodes by 2008 or so Process: elevated S/D (selective epi) and advanced annealing and doping techniques Structure: ultra-thin body (UTB) fully depleted (FD) SOI, followed by multiple-gate structures. It will be an important challenge to ensure the reliability of all these new materials, processes, and structures in a timely manner.

ITRS2005: Process Integration, Devices, and Structures (PIDS)

Table 39b Process Integration Difficult Challenges—Long-term

Difficult Challenges<32 nm	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate MOSFETs) with ultra-thin, lightly doped body will be needed to effectively scale MOSFETs to 11 nm gate length and below. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, nanowires, carbon nanotubes, or other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed.
7. Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs	Fundamental issues of statistical fluctuations for sub-11 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, line edge roughness, and width variation.
8. Identifying, selecting, and implementing new memory structures	Dense, fast, low operating voltage non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness and attaining the very low leakage currents that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.

ITRS2005: Process Integration, Devices, and Structures (PIDS)

Major relevant changes in 2005/2006 ITRS:

- A single-number technology node is no longer used (DRAM, MPU and Flash each has its own independent measure)

- Timing of a technology cycle may be different for a particular product. *Trend cycle: a period of time to achieve 0.71x size reduction per cycle (0.5x per two cycles).*

- For MOSFET, figure of merit for scaling is the intrinsic speed $1/\tau$, (τ=CV/I, the intrinsic delay). Historical rate of increasing $1/\tau$ by 17% per year is targeted.

- **Emphasis of emerging research devices, materials, architectures expected beyond CMOS scaling (year 2020?) (new ERD chapter)**

Beyond CMOS

Table 59 Emerging Research Logic Devices—Demonstrated Projected Parameters

Device		FET [B]	1D structures	Resonant Tunneling Devices	SET	Molecular	Ferromagnetic logic	Spin transistor
Types		Si CMOS	CNT FET NW FET NW hetero-structures Crossbar nanostructure	RTD-FET RTT	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin transistor
Supported Architectures		Conventional	Conventional and Cross-bar	Conventional and CNN	CNN	Cross-bar and QCA	CNN Reconfigure logic and QCA	Conventional
Cell Size (spatial pitch)	Projected	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [D]	3μm [H]	~700 nm [M]	~2μm [R]	250 nm [V, W]	100 μm [X]
Density (device/cm^2)	Projected	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known

ITRS2005: Emerging Research Devices (ERD)

Table 52 Difficult Challenges—Emerging Research Device Technologies

Difficult Challenges ≥32 nm	*Summary of Issues*
Development and implementation into manufacturing of a non-volatile memory technology, scalable beyond 32 nm, combining the best performance features of both volatile and non-volatile memory technologies for both stand-alone and embedded applications.	Identification of the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, non-volatile RAM Development of a manufacturable, cost-effective fabrication technology integrable with the process flow for CMOS logic providing for seamless integration onto a CMOS platform
Difficult Challenges <32 nm	
Toward the maturation of CMOS scaling or beyond, discovery, reduction to practice, and implementation into manufacturing of novel, non-CMOS devices and architectures integrable (monolithically, mechanically, or functionally) with a CMOS platform technology. • 1D to extend charge based devices. • Articulate the fundamental physical principles needed to develop new device technologies. • Find a new information processing technology that addresses these fundamental principles (see the section entitled "Fundamental Guiding Principles"). • Make emerging logic and memory devices compatible. (A new logic technology may require a new compatible memory technology.) • Integrate the materials, device and architectural communities to interact and collaborate in discovering a new information processing technology.	No current approaches support the information processing technology required for "Beyond CMOS" satisfying the need for additional decades of functional scaling. Discovery and reduction to practice of new, low-cost methods of manufacturing novel information processing technologies. Any new technology for information processing must be compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. A knowledge gap exists between materials behaviors and device functions. Current metrologies examine fixed material states, but do not probe the state change dynamics.

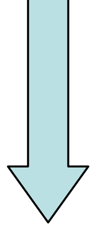
ITRS2005: Emerging Research Devices (ERD)

Table 53 Difficult Challenges—Emerging Research Materials Technologies

Difficult Challenges ≥32 nm	*Summary of Issues*
1D Charge State	Nanotube and nanowire properties, bandgap energy and carrier type, and mobility vary greatly at growth and are controlled by variations in composition, diameter and nanometer scale structure. Nanotubes and nanowires grow in random locations and orientations, which is incompatible with high density memory and logic applications.
Difficult Challenges <32 nm	*Summary of Issues*
Molecular State: Molecules with Controllable, Reproducible Switching Mechanisms	Molecular switching is often highly variable between device lots fabricated with the same chemicals and materials. Contact formation and bond structure may require atomic level control. While groups have been able to fabricate devices that exhibited charge storage, complex interactions have been observed with contact materials and redox reactions, but it is often difficult to determine whether switching and transport are through molecular transport or other mechanisms. No metrology tools are available to measure atomic structure details in carbon-based molecules embedded between two contact layers.
Spin State: Materials that Enable Spin Gain at Room Temperature and Dissipationless Transport	Ferromagnetic (FM) semiconductors only work at low temperatures < 200 K; need a room temperature FM semiconductor. New materials are needed that can enable spin amplification (gain).

ITRS2005: Emerging Research Devices (ERD)

Information Processing Hierarchy



- System function (application)
- Computer architecture
- Micro- or nanoarchitecture
- Circuits
- Devices
- Materials

"*computer architecture*" - all the systems elements, including software, needed to meet the needs of a given information processing application.

"*Micro- and nanoarchitecture*" - implementation details of how the various computing functions can be organized for high information throughput and minimum expense and energy cost.

New "nanoarchitecture" may be needed.

ITRS2005: Emerging Research Devices (ERD)

Information Processing Hierarchy

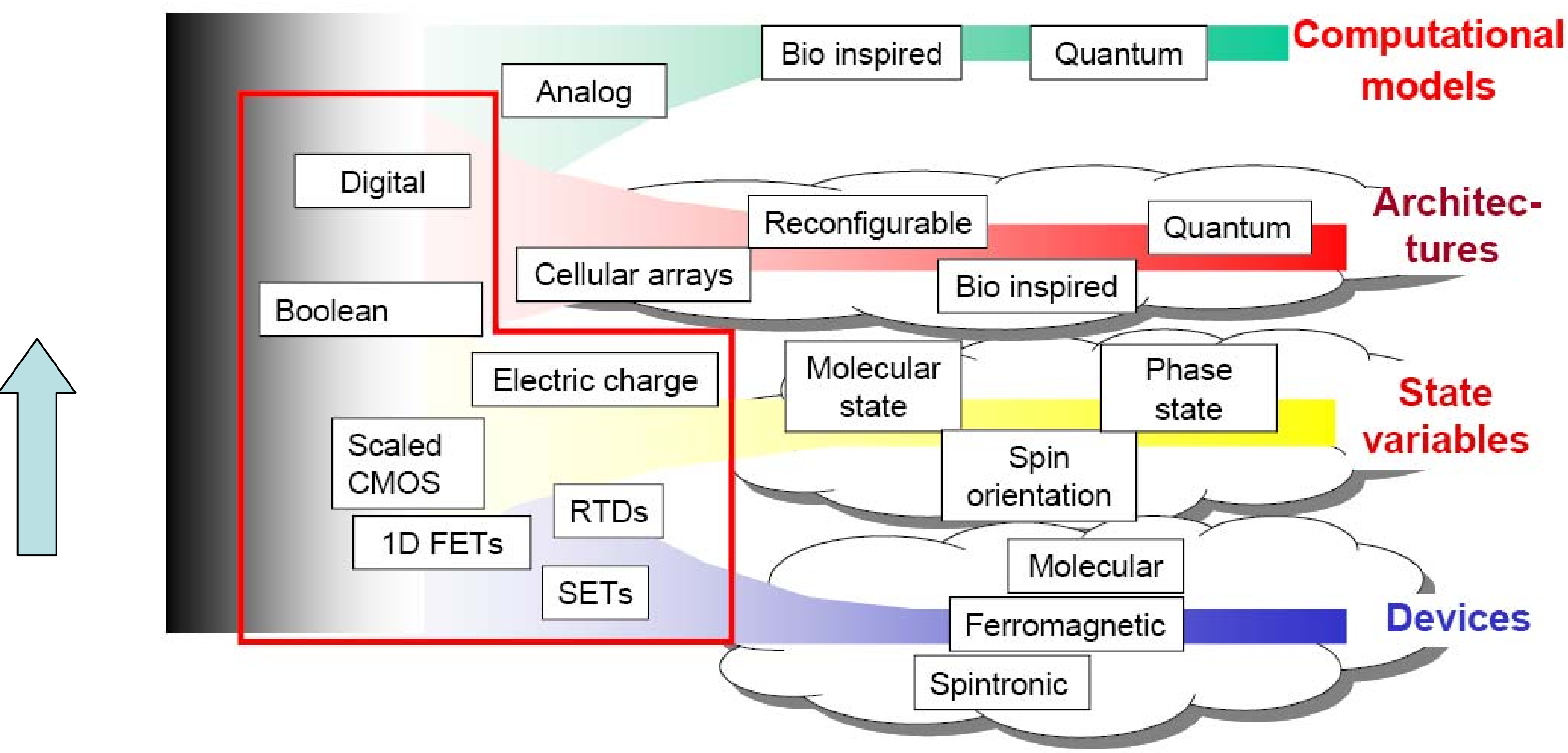


Figure 51 A Taxonomy for Nano Information Processing

ITRS2005: Emerging Research Devices (ERD)

Table 61 Emerging Research Architecture Implementations

Architecture Implementations	*Quantum Cellular Automata*	*Cellular Nonlinear Networks*	*Reconfigurable Implementations*	*Biologically Inspired Implementations*
Application Domain	Complex signal processing	Fast image processing Associative memory Complex signal processing	Reliable computing with unreliable devices Historical example: Teramac FPGA implementation	Goal-driven computing using simple and recursive algorithms High computational efficiency for certain applications
Device And Interconnect Implementations	Arrays of nanodots or molecular assemblies	Resonant tunneling devices, SETs	Molecular switches Crossed arrays of 1D structures Switchable interconnects	Molecular organic and bio-molecular devices and interconnects
Information Throughput	Fan-out =1 throughput constrained by adiabatic clocking requirements	Fan-out close to unity	Fan-out variable but performance degraded slightly by need for defect management schemes	Massive parallelism Requires some long-range data transfer Fan-out very high in brains ($\sim 10^4$)
Power	Power comparable to scaled CMOS (~0.2 MIPS/mW) Data streaming applics will need ~100 MOPS/mW	Power comparable to scaled CMOS (~0.2 MIPS/mW) Data streaming applics will need ~100 MOPS/mW	Only preliminary estimates, but these are encouraging	High parallelism allows lower operational speeds Power consumption of human brain 10–30 W at millisecond rates
Interconnects	No local interconnects, but many control lines are needed	Local interconnects with neuron-like waveforms	Interconnects by crossed arrays	Interconnects distributed over a range of distances

ITRS2005: Emerging Research Devices (ERD)

Textbooks:

Fundamentals of Modern VLSI Devices by Yuan Taur and Tak H. Ning
Cambridge University Press, 1st edition (October 13, 1998) ISBN: 0521559596

Nanoelectronics and Information Technology by Rainer Waser
John Wiley & Sons 2 edition (April 22, 2005) ISBN: 3527405429

Reference books:

* *Physics of Semiconductor Devices* By S. M. Sze and K. K. Ng
Wiley-Interscience (October 27, 2006), 3rd edition
ISBN: 0471143235

* *The Physics of Low-Dimensional Semiconductors* by John H. Davies
Cambridge University Press (December 13, 1997), ISBN: 052148491X

Physics of Semiconductor Devices by M. Shur
Prentice Hall (January 26, 1990), ISBN: 0136664962

Lecture notes, electronic copy published on course website after each lecture.

Schedule:

- *Introduction. (1 lecture)*
  (ITRS 2005, PIDS, ERD)

- *Energy bands. (1 lecture)*
  Free electron model, Fermi surfaces, carrier density, density of states, energy bands (nearly-free electron model and tight-binding model), effective mass. (Waser 3, Davies 2)

- *Electrons and holes in Si. (1 lecture)*
  Intrinsic carrier concentration, envelope function, doping, Si and GaAs lattice and band structures, valley degeneracy, HH and LH bands, surface states. (Waser 3, Davies 2)

- *Electrical transport. (1 lecture)*
  Boltzmann transport equation, scattering time approximation, mobility, Einstein relation, scattering mechanisms, phonons, screening (Waser 3, Davies 2)

- *Minority carrier diffusion equation and P/N junctions (1 lecture)*
  minority carrier lifetime, diffusion currents, build-in potential (Taur 2.2)

- *MOS capacitor (1 lectures)*
  C-V, interface charges (Taur 2.3)

- *MOSFET devices (2 lectures)*
  Drain-current model, I-V characteristics, subthreshold region, channel mobility, (Taur 3)

- *Short channel and hot carrier effects (2 lecture)*
  velocity saturation, high field effects substrate current (Taur 3.2,2.4)

- *CMOS device design (1 lecture)*
  Threshold voltage design, discrete dopant effects, effective channel length. (Taur 4)

- *CMOS performance factors (1 lectures)*
  S/D resistance, parasitic capacitances, quantum capacitance, gate resistance, interconnect R and C, gate delay. (Taur 5)

- *CMOS scaling and novel device concepts (3 lectures)*
  Scaling rules, high-k dielectrics, metal gates, SOI devices, double gate devices, strained Si (Taur 4.1, 5.4, Waser 13)

- *Schottky barriers and Ohmic Contacts (1 lecture)*
  Metal/semiconductor interfaces, transport mechanisms, Ohmic contacts. (Sze 5)

- *Heterostructure devices (1 lecture)*
  Band bending at the interface, modulation doping, HEMT (Shur 2.12)

- *Quantum size effects (1 lecture)*
  3D, 2D, 1D structures, Resonant tunneling devices (Sze 9, Shur 7.6)

- *Ballistic transistors (1 lecture)*
  Ballistic transport, "contact" resistance, ballistic FET (notes)

- *Single electron devices (1 lecture)*
  Coulomb blockade phenomena, Single electron transistors (Waser 16)

- *Carbon nanotube devices (1 lectures)*
  Band structure, growth, transport, CNTFET (Waser 9)

- *Nanowire devices (1 lecture)*
  Growth, electrical and optical devices, devices on flexible substrates (notes)

- *Molecular Electronics (1 lecture)*
  Single molecule devices, crossbar structures (Waser 20)

- *Magnetism and Spintronics (2 lectures)*
  Magnetic materials, Magnetoresistance effects, spin injection, SFET (Waser 4, 24)

- *Quantum computing (1 lecture)*
  Quantum parallelism, qubits, entanglement, teleportation. (notes)

Grading:
Homework 50% (roughly biweekly basis)
Term paper 45%
Participation 5%

office : 2417-A EECS Building
regular office hours: MW, 10:30-11:30am
phone : (734) 615-2306
fax : (734) 763-9324
email : wluee@umich.edu

Further reading:

Summary, PIDS and ERD chapters of the 2006 ITRS

http://www.itrs.net/links/2006Update/2006UpdateFinal.htm

Next time:

Energy bands. (1 lecture)

Free electron model, Fermi surfaces, carrier density, density of states, energy bands (nearly-free electron model and tight-binding model), effective mass. (Waser 3, Davies 2)