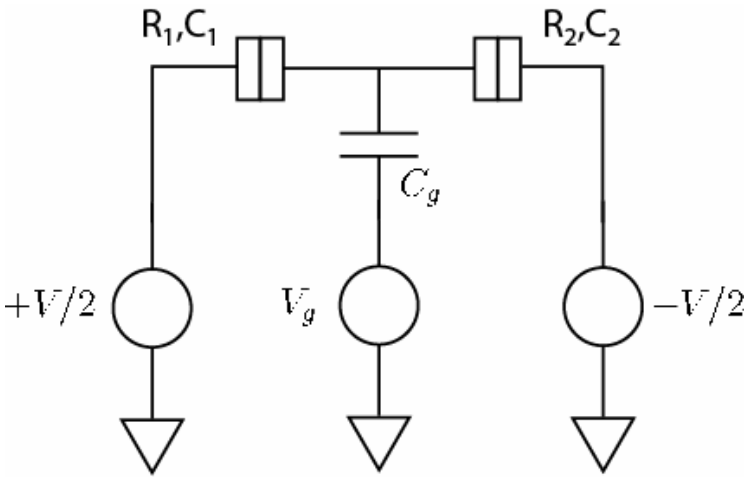
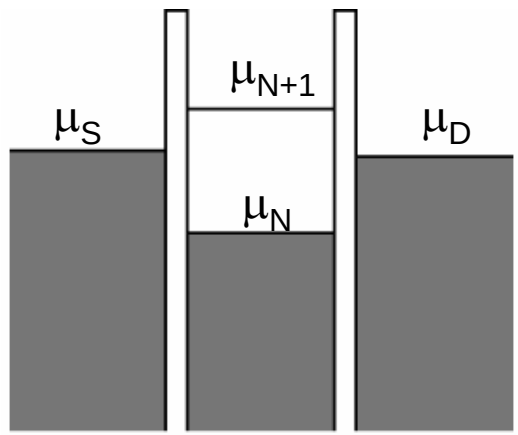
Single electron devices: Fabrication techniques and applications

10/13/2005, week6

Single-electron transistor





Two tunnel barriers, each characterized by R, C
A capacitively coupled gate

$$E_C = e^2 / C_\Sigma$$

$$C_\Sigma = C_1 + C_2 + C_g$$

requires

$$E_C > k_B T$$

$$R_{1,2} > R_Q \equiv h / e^2 = 25.8\mathrm{k}\Omega$$

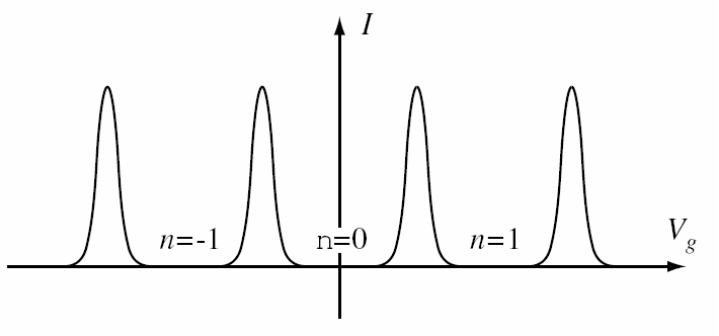
$$\mu_{N+1} = (N + \tfrac{1}{2})\frac{e^2}{C_\Sigma} + \frac{e}{C_\Sigma}\sum_i C_i V_i$$

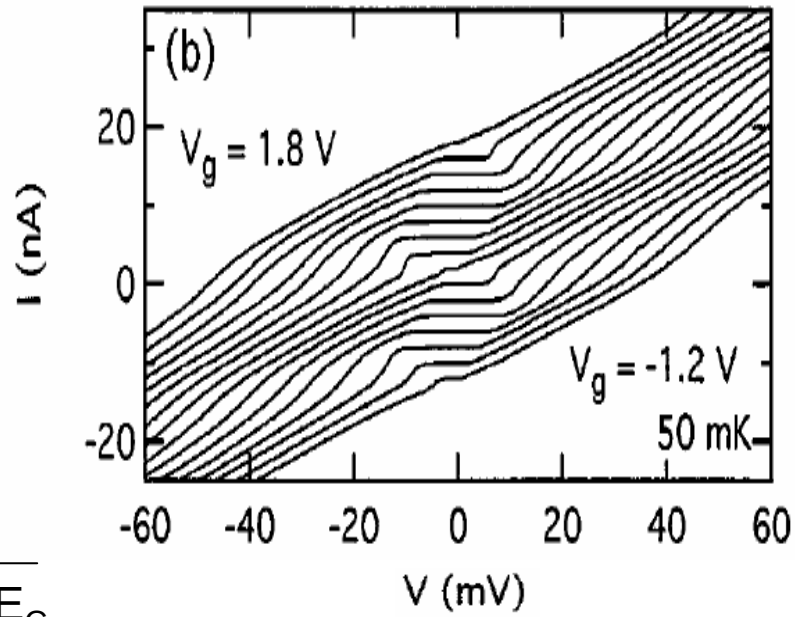
$$= (N + \tfrac{1}{2} + \sum_i C_i V_i / e)\frac{e^2}{C_\Sigma}$$

$C_g V_g$, (effective) offset charge

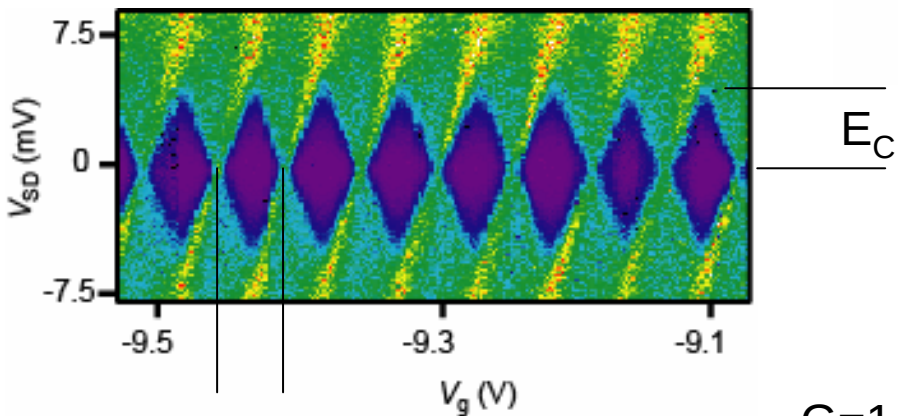
$$\Delta\mu = \mu_{N+1} - \mu_N = E_C = e^2 / C_\Sigma$$

Coulomb blockade





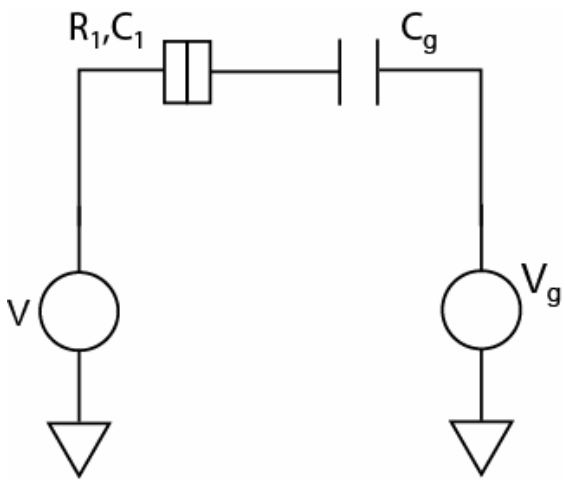
Coulomb diamonds

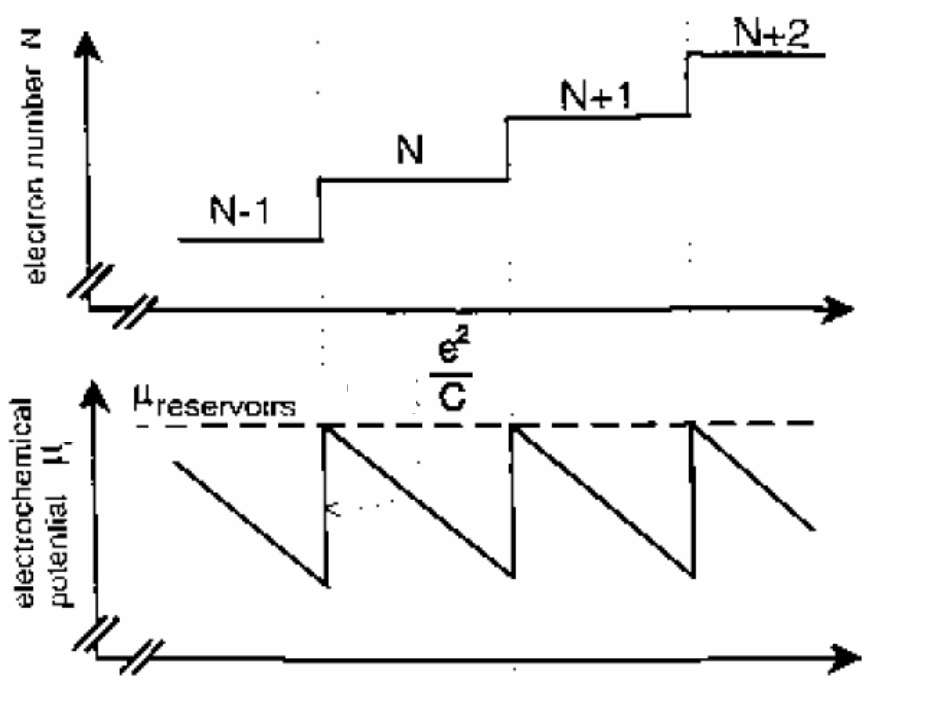


$\Delta V_g = e/C_g$

$G = 1/(R_1+R_2)$ outside blockade region

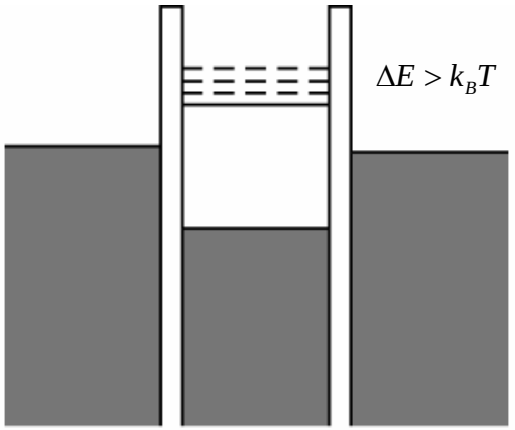
Single electron box

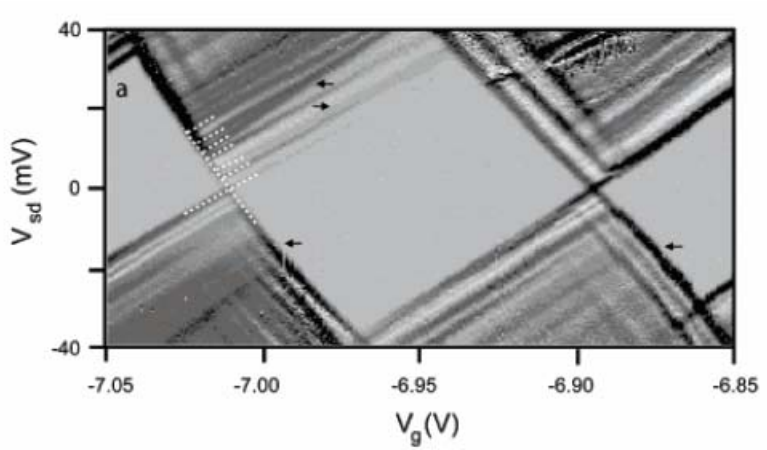


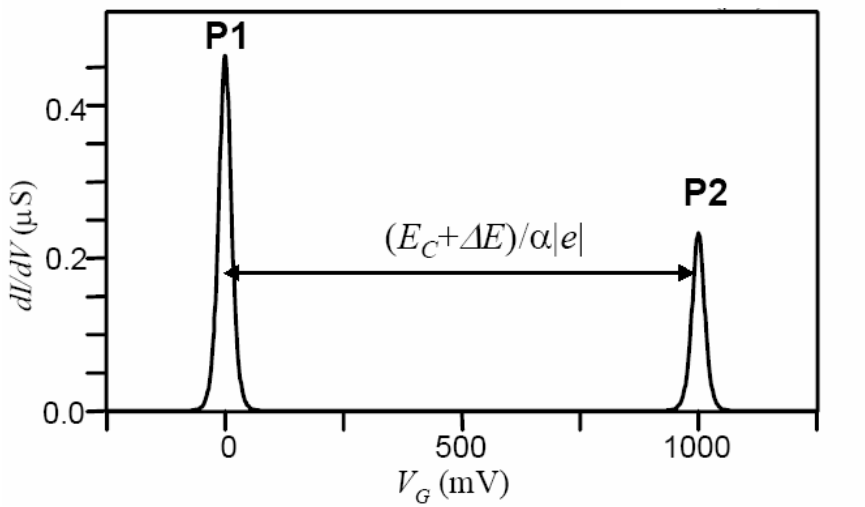


Only one tunnel barrier.
Discrete charge states.

Quantum dot







Peak spacing includes ΔE term
Peak height determined by coupling of the individual energy levels with S/D leads, and no longer uniform.

Implementations of single electron devices

Several different ways of making SETs:

- Shadow-evaporation + oxidation of Al

  Most common approach, best suited for large-scale fabrication of arrays.

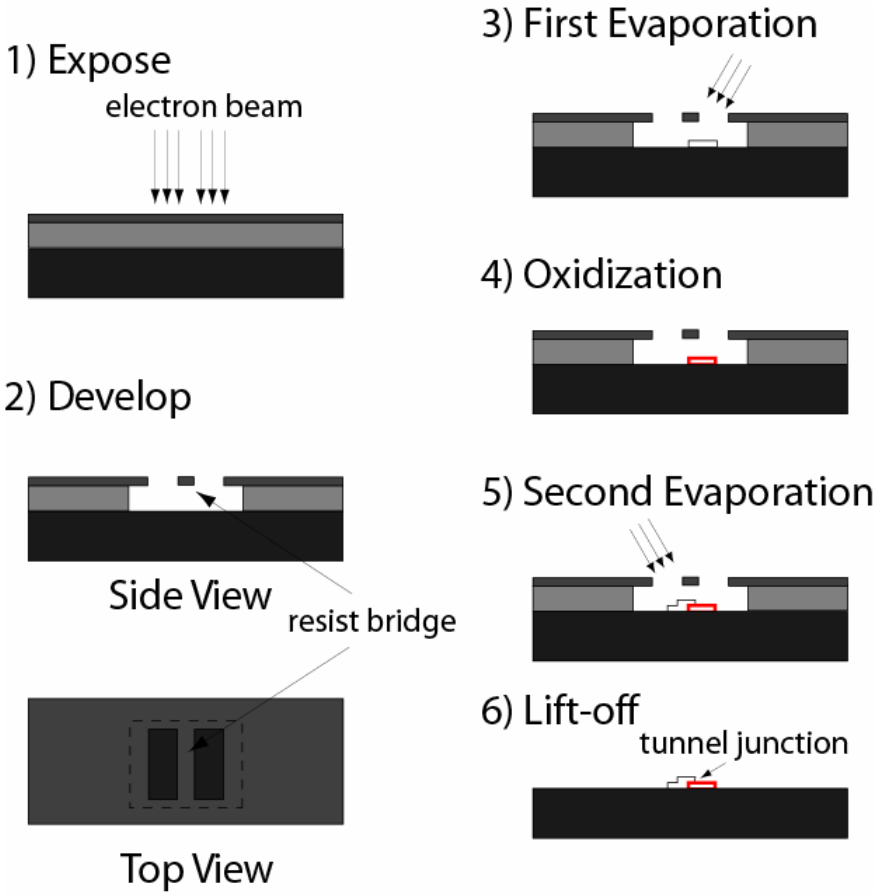
- Oxidation of silicon

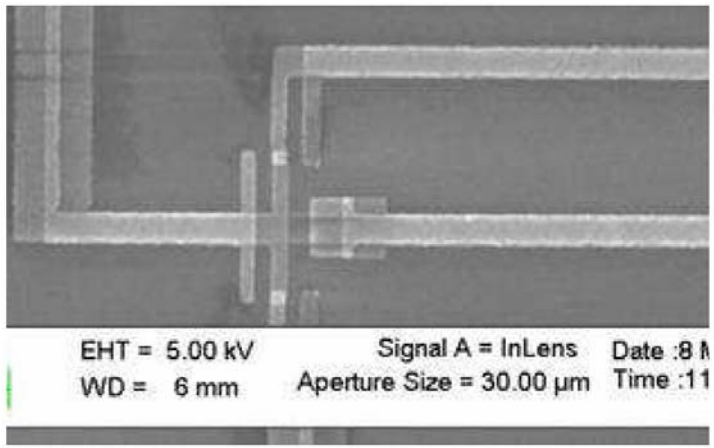
  Compatibility / ease of integration with Si

- Chemically-aided approaches

  Trapped nanoparticles; AFM contacting; molecular devices.

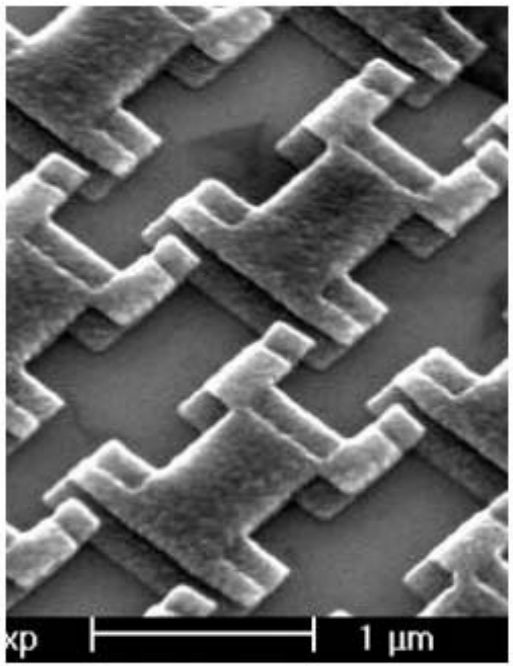
Shadow Evaporation and Oxidation of Al





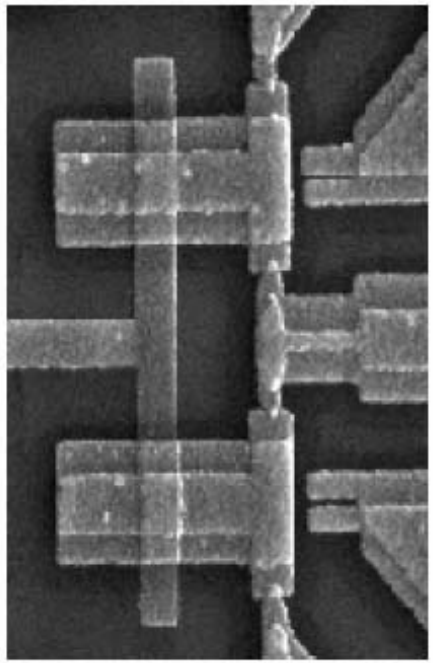
- Takes advantage of ease of growth of thin, high-quality Al_2O_3 for tunnel barriers.
- Uses geometry to make smallest possible junctions.
- Double-layer resist for e-beam lithography leads to overhang.
- Evaporate at an *angle*. Then oxidize
- for controlled length of time.
- Second evaporation from a different angle completes the MIM tunnel junction.

Shadow evaporation and oxidation of Al



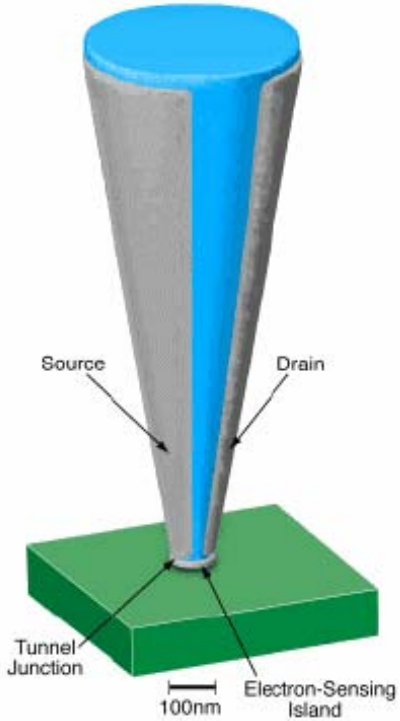
2d Josephson junction array

image from Mooij, Delft, Netherlands



Inverter from two coupled SETs

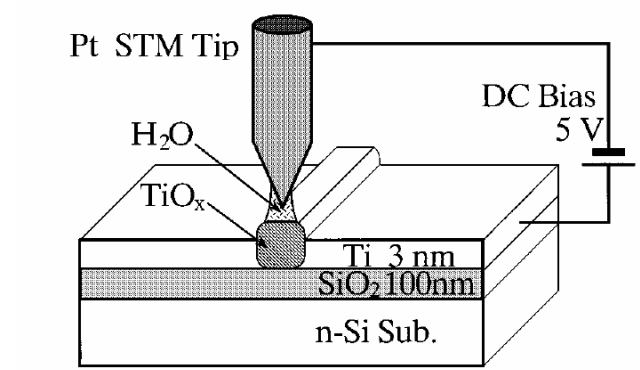
image from Mooij, Delft, Netherlands

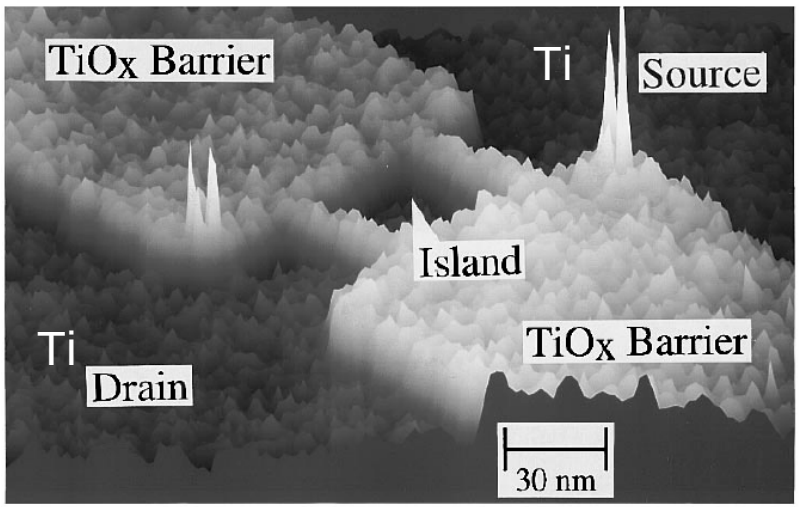


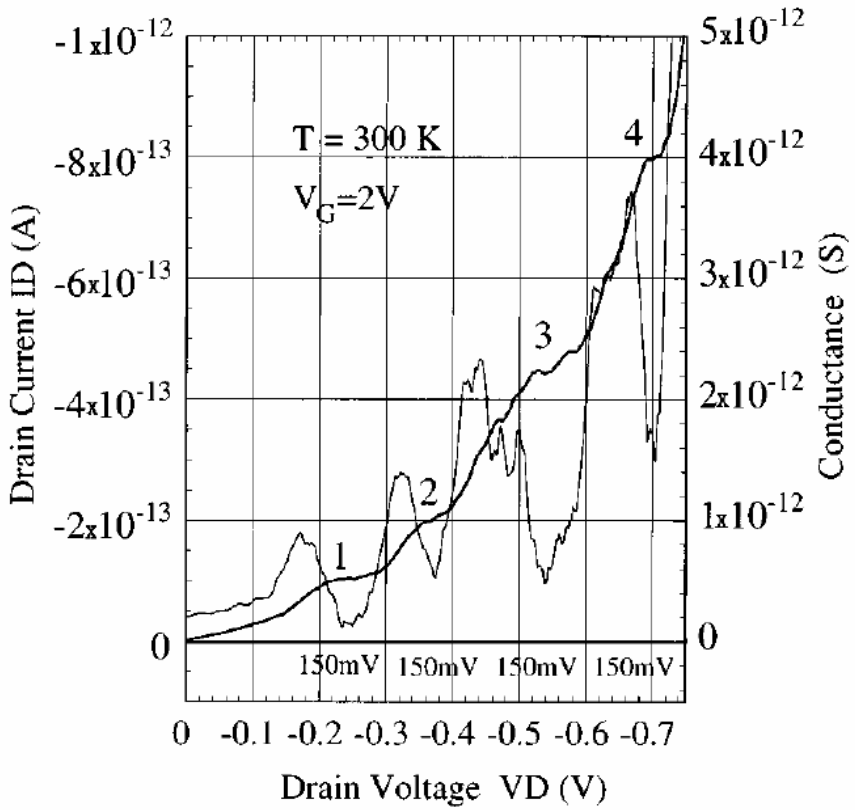
SET on tip of drawn glass fiber

image from Bell Labs

Local oxidation







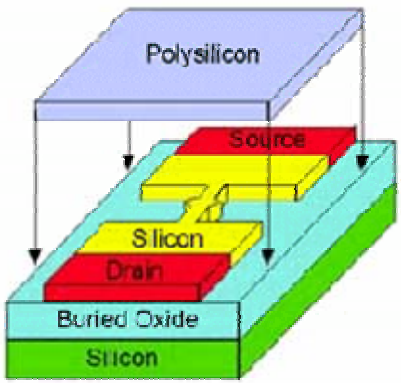
- Local electrochemical oxidation (anodization) used to convert continuous Ti strip into island + insulating tunnel barriers.
- Painstaking fabrication, but payoff is SET with some room temperature functionality.

Matsumoto *et al.*, APL **68** 34 (1996).

Oxidation of Silicon

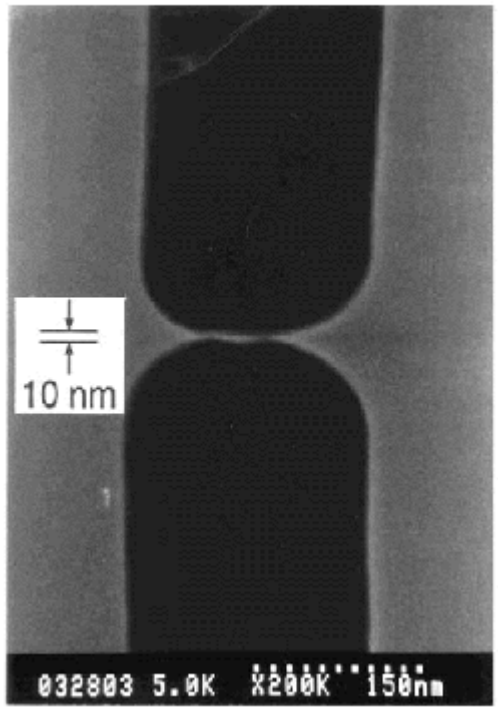
image from Steve Chou, Princeton

Quantum-Dot Transistor on SOI

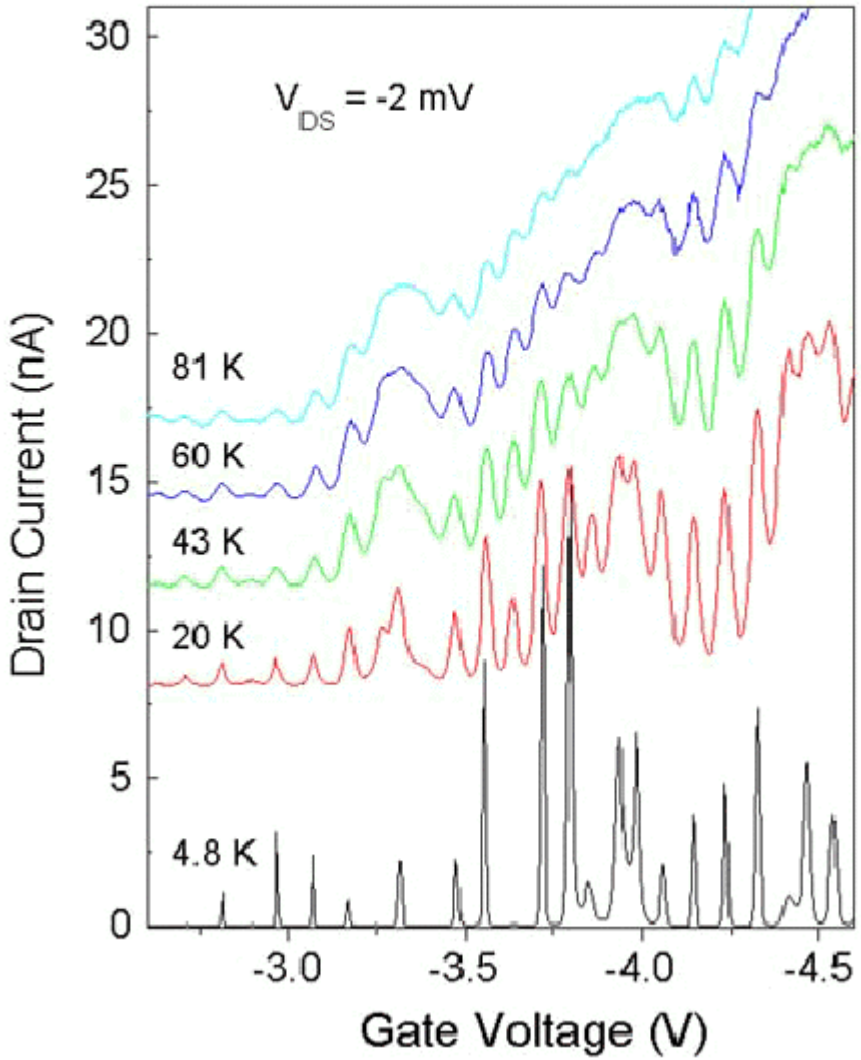


- In-plane size of QD defined by e-beam lithography and reactive-ion etching
- Vertical size of QD defined by top Si layer thickness
- Si QD size Reduced during gate oxidation
- Hard-wall confinement

Silicon Single Electron Transistor
(After Gate Oxidation)



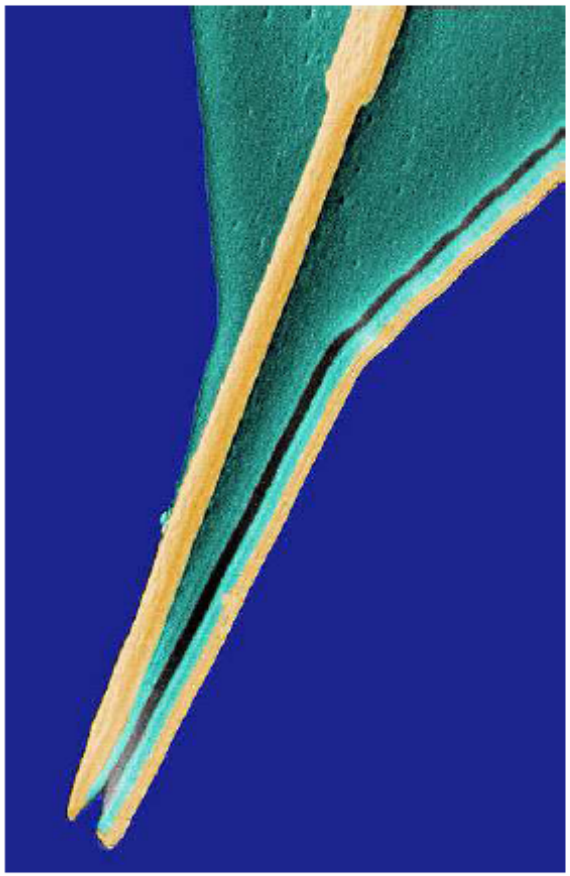
Oxidation of Silicon

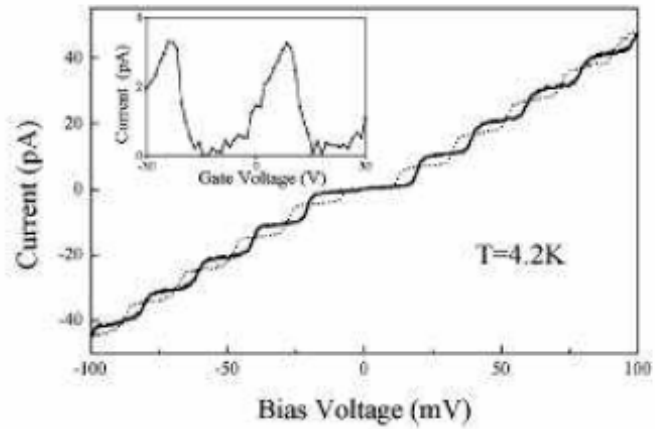


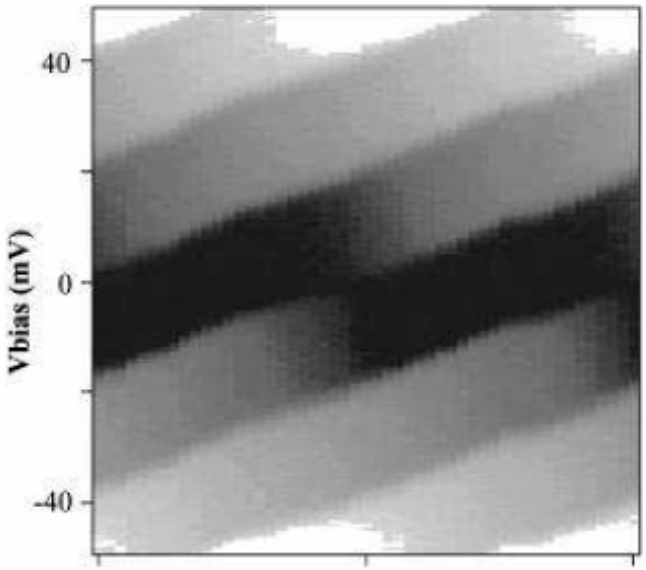
Even for an island as small as this, getting room temperature oscillations is a real challenge.

Nanoparticles on surfaces

Special tip can incorporate gate, too, for SET action.

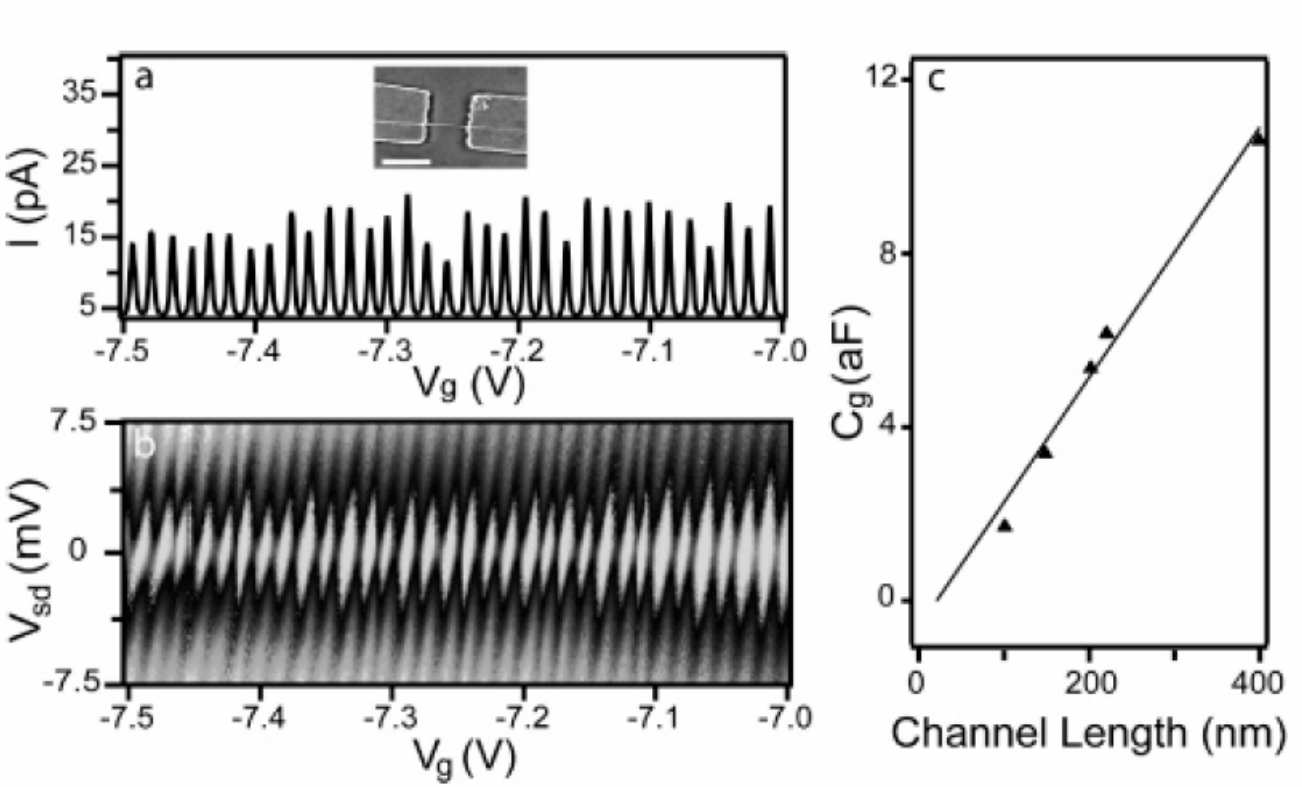




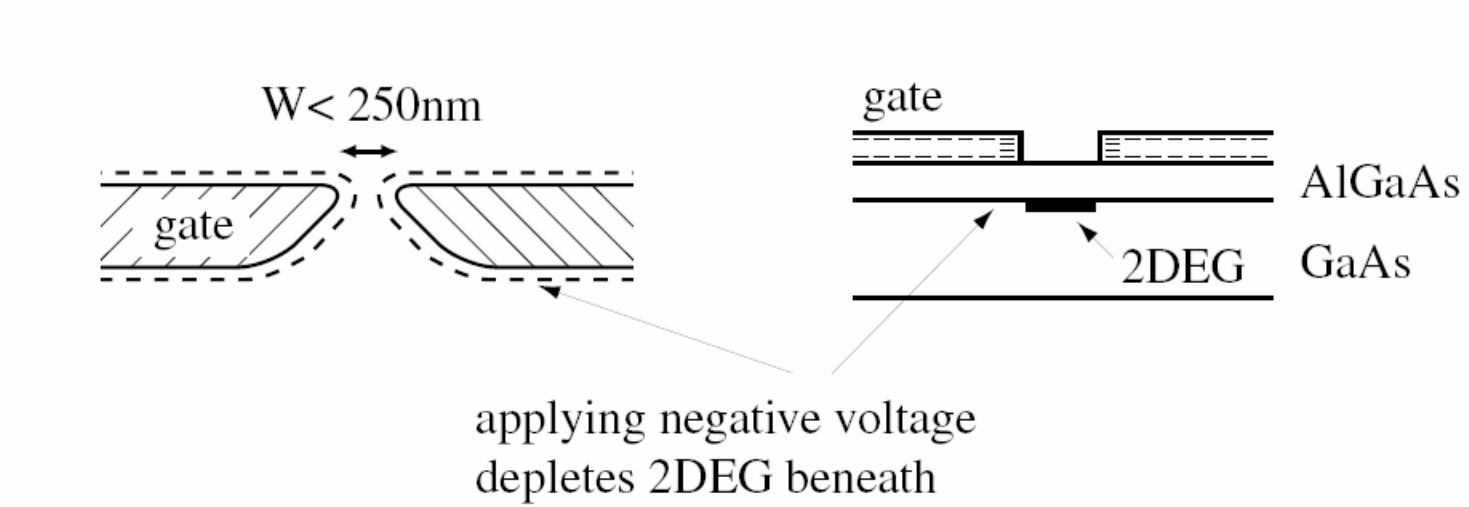


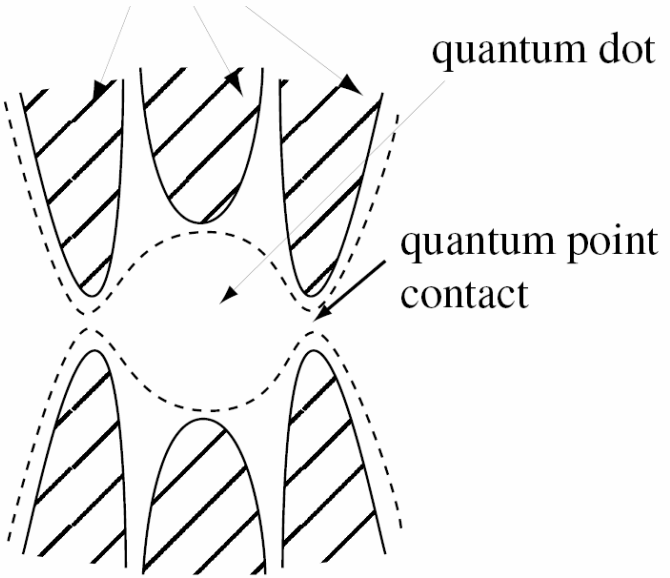
images from Gurevich *et al.*, APL **76**, 384 (2000).

Tunnel barriers formed by Schottky barriers at the contacts



Formation of quantum dots in 2DEG

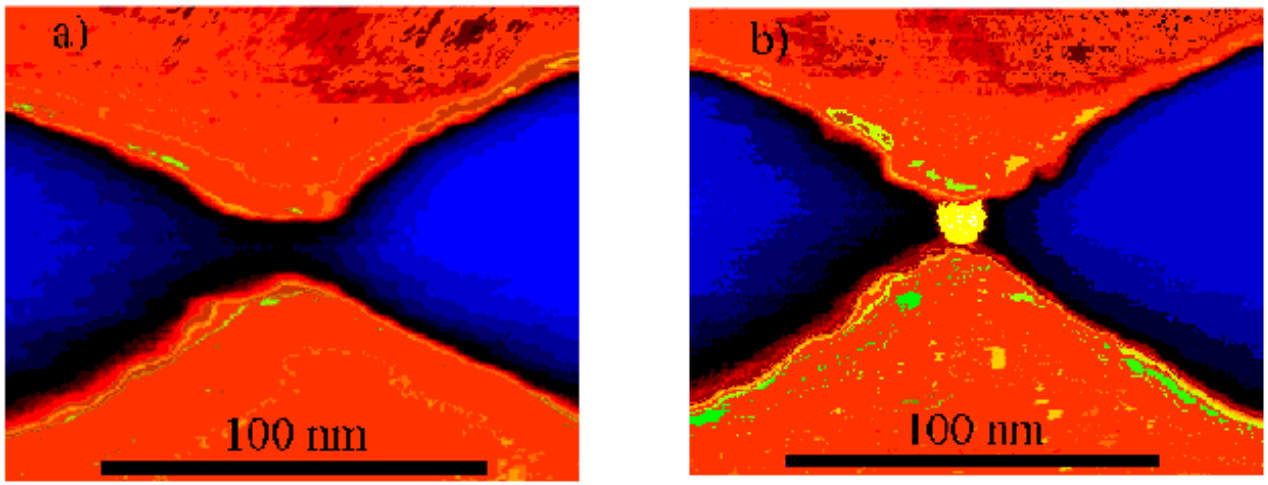




Dots formed by depletion gates

Trapped nanoparticles

images from Dekker, Delft



One approach: use chemical fabrication to make nanoparticles for use as SET islands.

Trap particles between lithographically created electrodes.

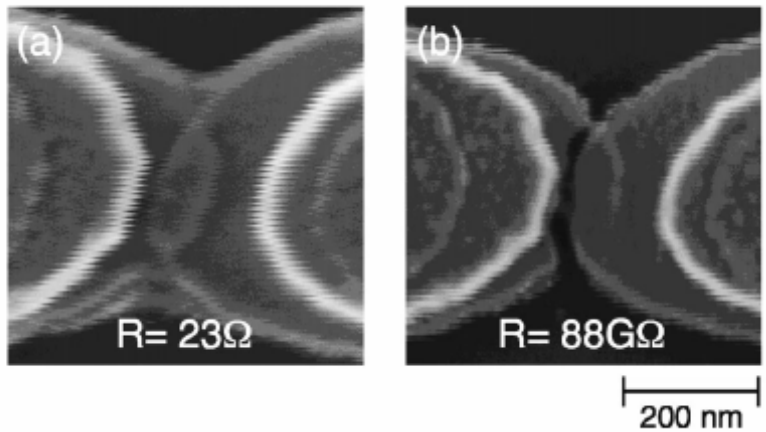
Electrostatic trapping in above – nanoparticle drawn to region of high local electric field as source/drain are biased.

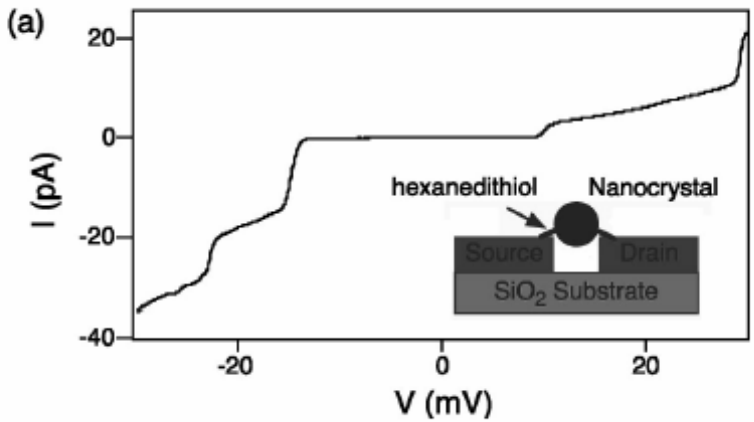
Trapped nanoparticles

images from Park *et al.*, APL 75, 301 (1999).

Alternative:

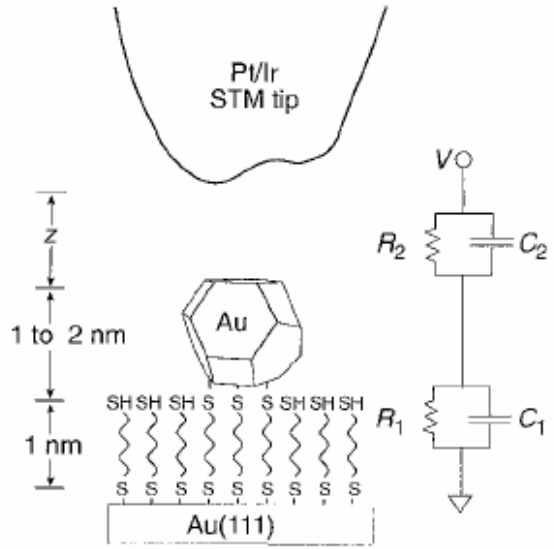
- Start with continuous metal electrodes on top of insulated metallic substrate, to be used as a gate.
- Dust surface to decorate with nanoparticles, such as chemically synthesized CdSe nanocrystals.
- Break into separate source-drain electrodes by "electromigration", and sometimes nanocrystal ends up ideally positioned to act as island.

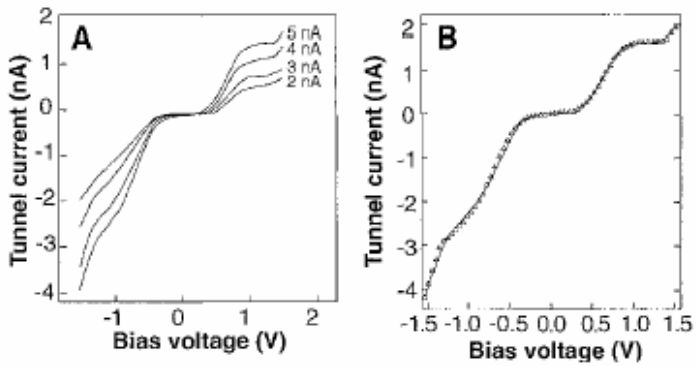




Nanoparticles on surfaces

- Can decorate surface with tethered nanoparticles, in this case Au colloid.
- Insulating layer = self-assembled monolayer of thiol-terminated alkane chains.
- Scanned probe microscope tip as drain electrode: Coulomb staircase.





images from Andres *et al.*, Science **272**, 1323 (1996).

Clear technological challenges:

- Reliable fabrication of sub-10 nm structures with little or no variation for room temperature Coulomb blockade physics.
- Tuning of “environmental characteristics” such as stray capacitance.
- Reliable (self-controlling?) tunnel junctions.
- Control of single electronic offset charges: individual charged defects can have effects identical to random offset voltages on gates!

Incentives:

- Dense integration.
- Possible ultralow power operation
- Ultimate limits of switching technology.

Technology possibilities

Voltage-based SET logic:

- Very similar to typical CMOS logic: high voltage = logic high; low voltage = logic low.
- Nonmonotonic drain current as function of gate voltage opens up designs not possible with regular MOSFET devices.

Charge based applications

- Nonvolatile memory
- Electrometry
- Metrology standards

SET logic:

- High scalability even on an atomic scale.

- Low power consumption (power consumption roughly proportional to the electron number transferred from voltage source to ground).

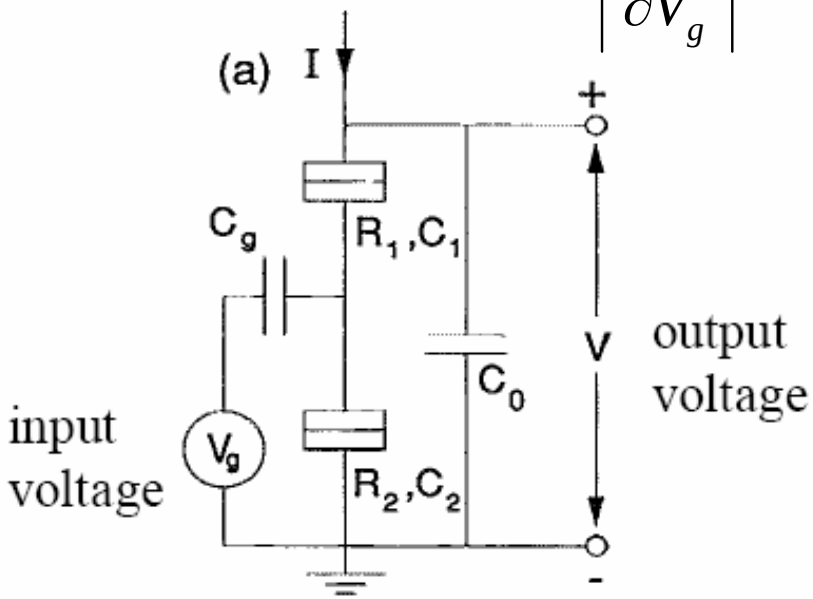
- Circuit designers can treat SET-based logic gates like conventional logic gates. (Waser, p425-441.)

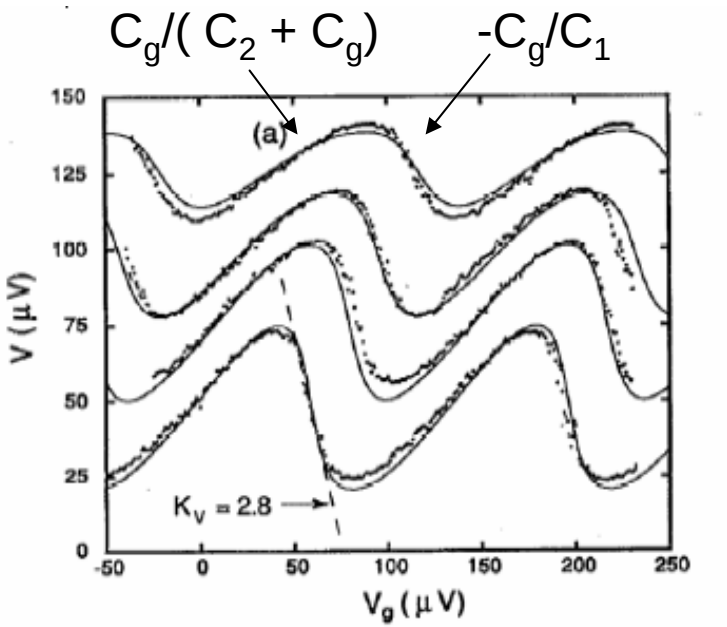
- SET characteristics (oscillatory response to V_G) mean that one SET can sometimes replace more than one regular MOSFET.

SET logic:

It is possible, with SETs, to achieve *voltage gain*. That is, the output voltage modulation of a circuit can be greater than the input voltage modulation:

$$K_V \equiv \left| \frac{\partial V_{out}}{\partial V_g} \right|$$

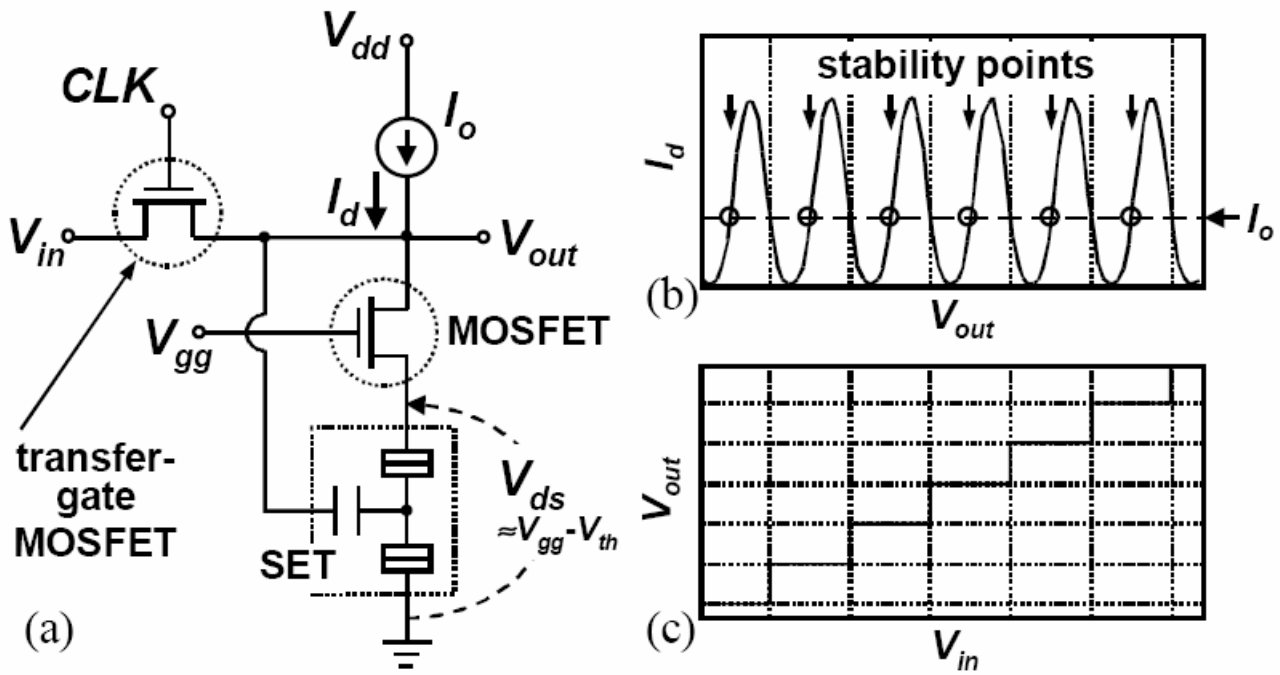




$K_V>1$, when $C_g>C_1$

Zimmerli *et al.*, APL **61**, 2616 (1992).

Multiple-valued logic



Inokawa, IEDM, 147, (2001)

SET logic:

Problems:

• For acceptable device performance,
either temperatures must be very low, or devices must be extremely small….

• “Off”-state leakage leads to power consumption problems comparable to highly-scaled CMOS.

• Background charges are also a serious problem.

• K_V normally < 1

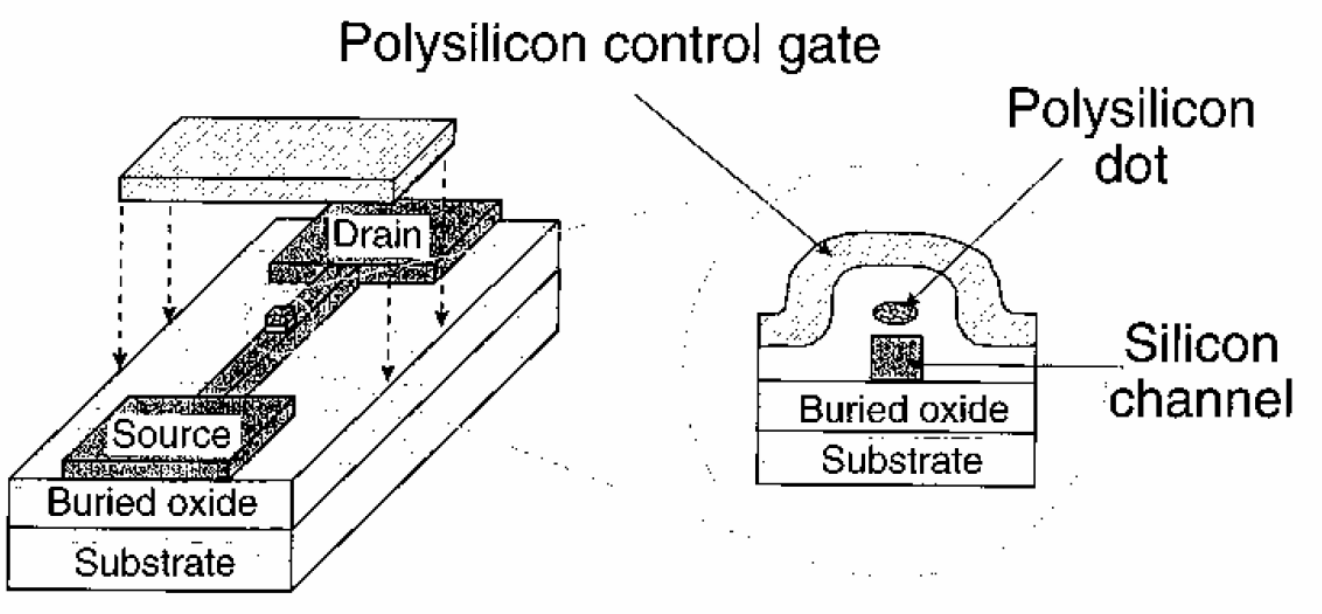
Prognosis:

Single electron logic devices are unlikely to be the technology that replaces CMOS at the few nm scale, unless there is a major breakthrough in fabrication, performace, or architectures.

SEDs more likely to find applications in niche areas:

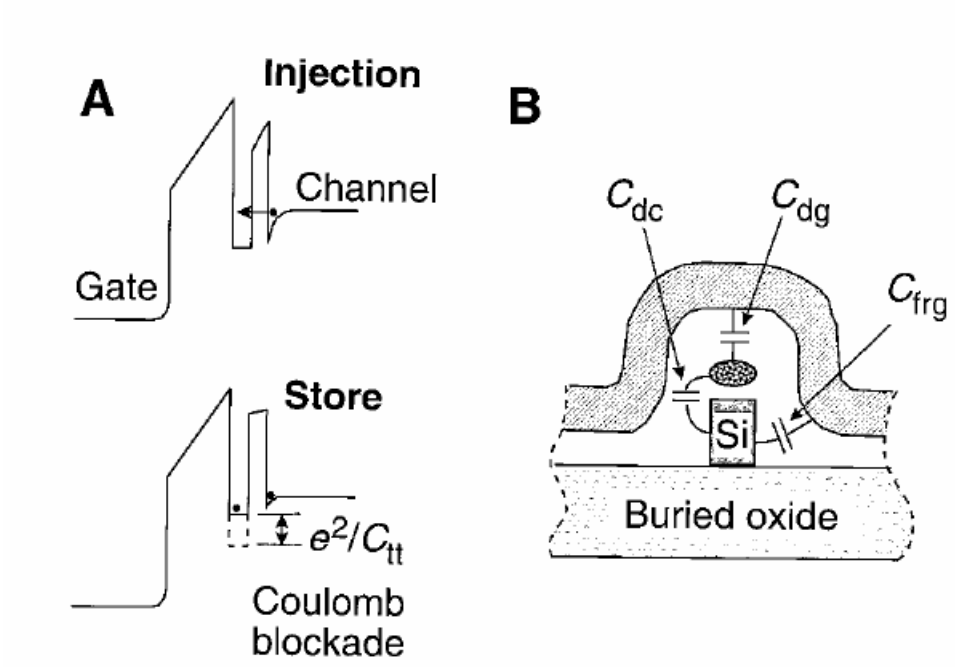
- Nonvolatile memory
- Electrometry
- Metrology standards

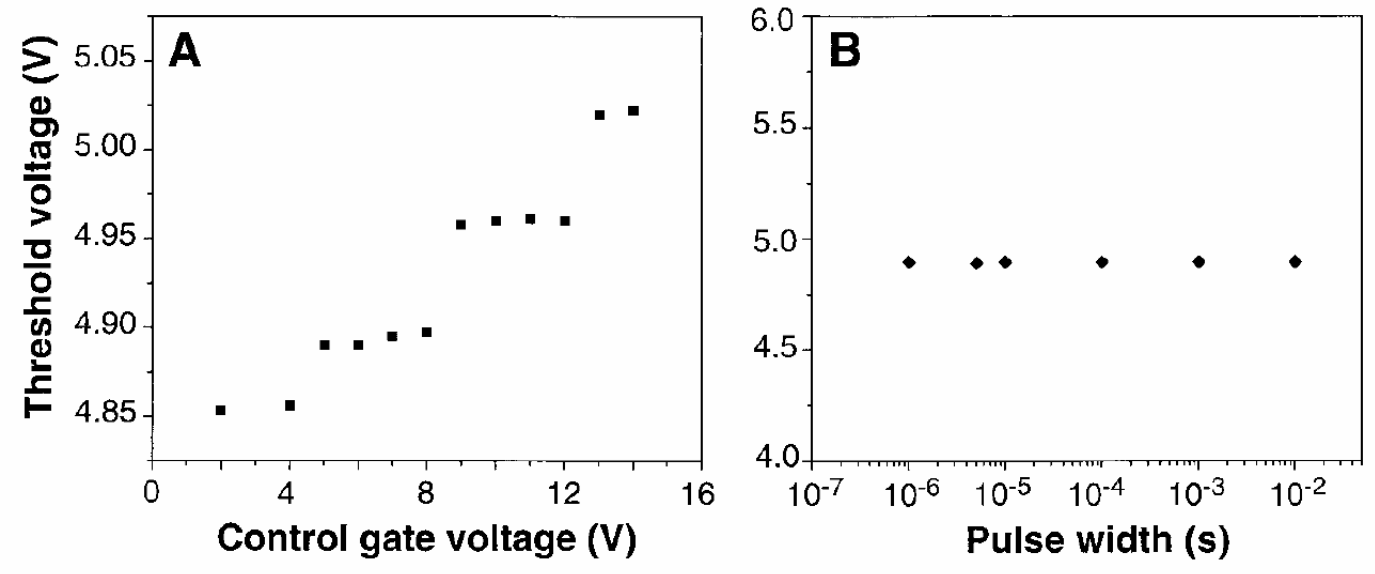
Single electron memory



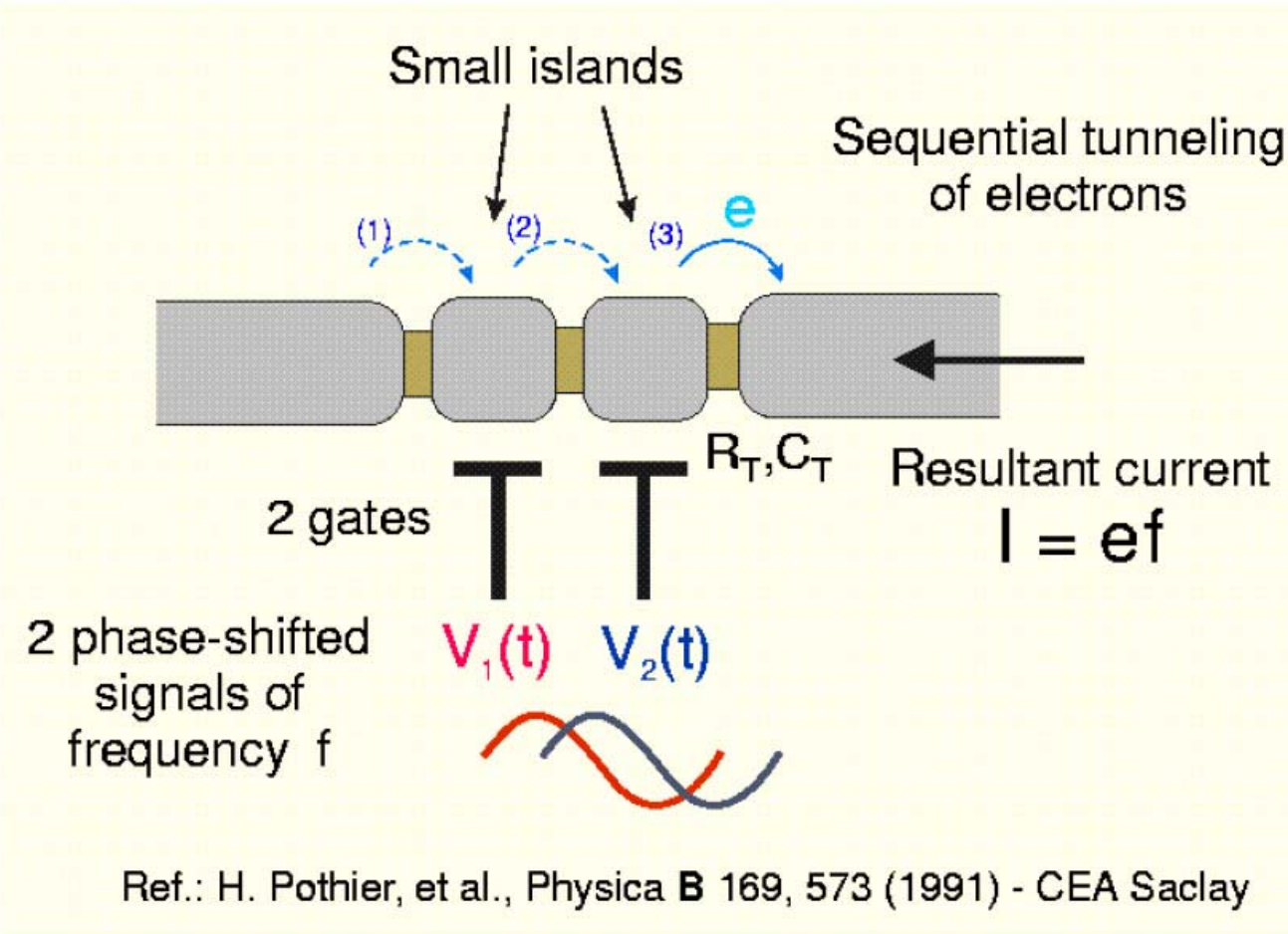
Single electron memory

- Discrete charge states.
- Self limited process.



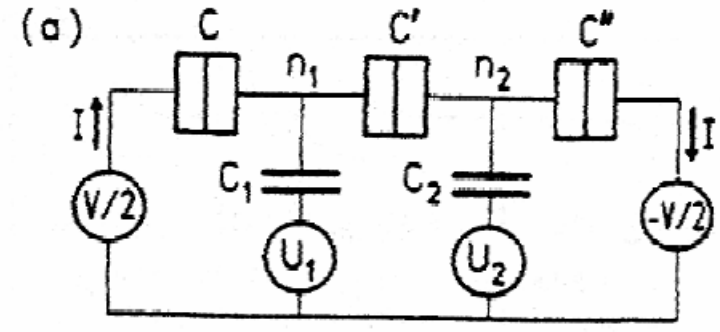


Current standard: SET pump



Current standard: SET pump

Cycling voltages around one of the “triple points” in the diagram at the lower right will transfer a *single electron* through the pump, right to left. (Thus a unidirectional current from left to right….)



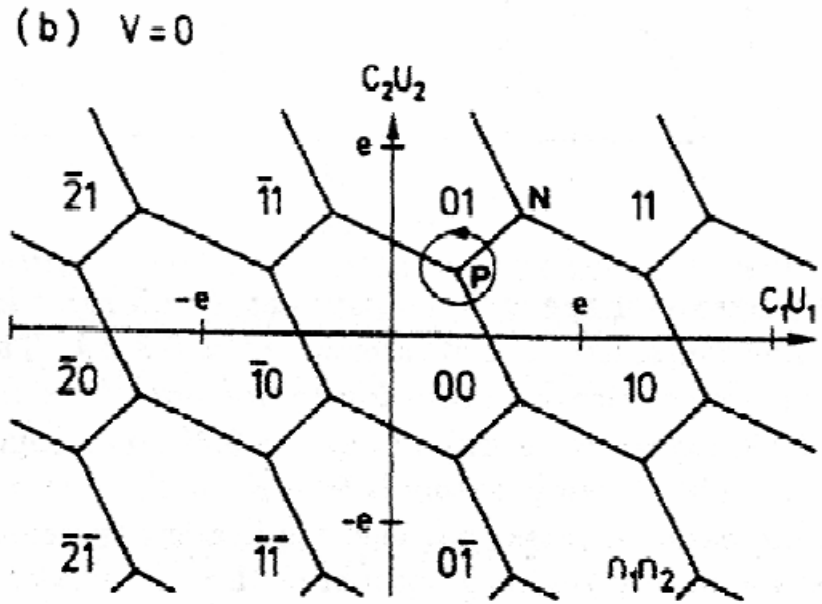


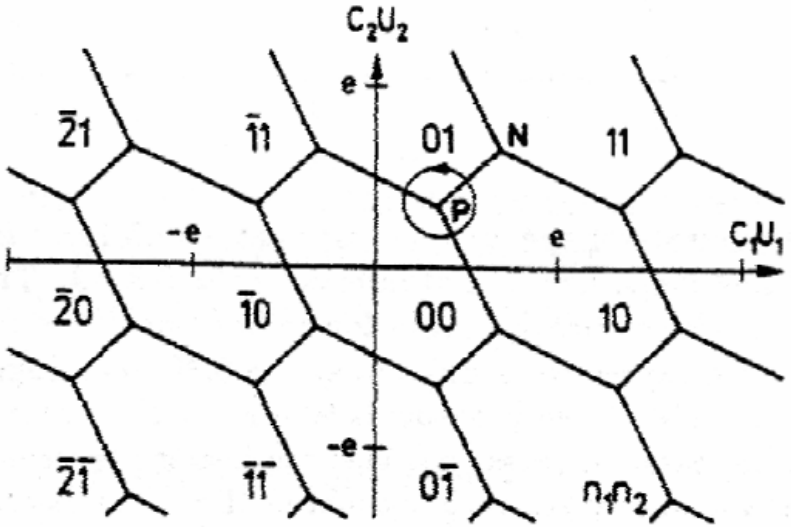
image from Esteve

Current standard: SET pump

Actual experimental data on 2-gate pump agrees with this.

Current is nonzero only in vicinity of “triple points”. Three junction two island pump errors in experiment: ~ 1%.

Error sources:
- thermal hopping
- “missed” tunneling events
- cotunneling



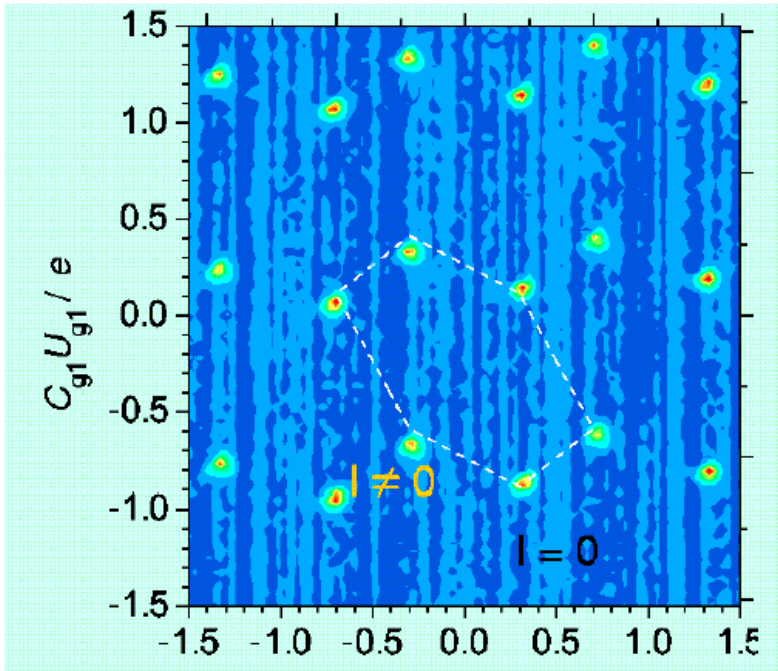


image from Zorin presentation, PTB

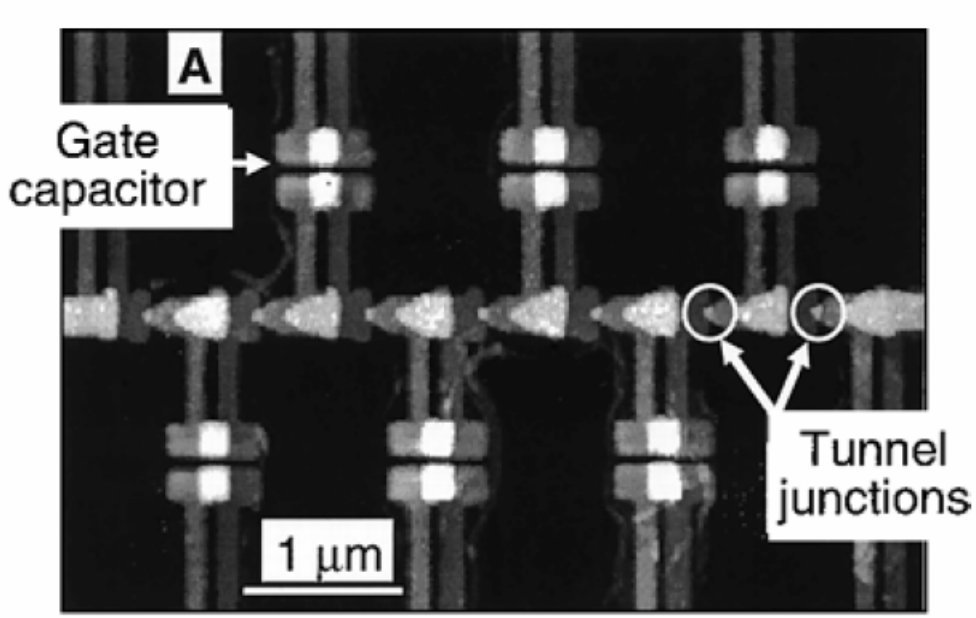
Current standard: SET pump

One approach to dealing with these errors: more junctions!

State-of-the-art: NIST seven-junction six-gate pump.

Really designed for low frequency work - electron counting rather than current standard.

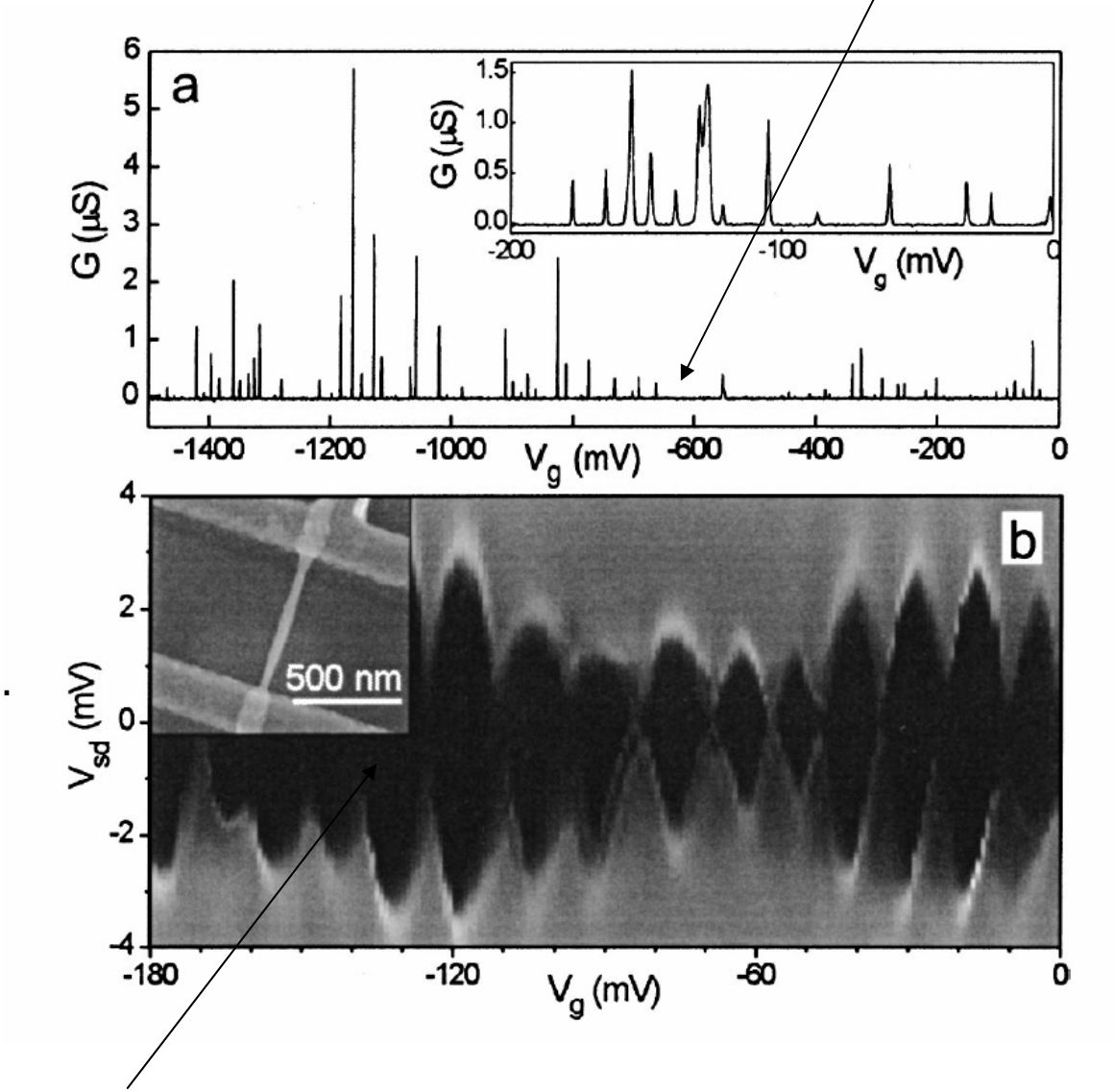
Errors with this set up: ~ 1.5×10^{-8}.



M.W. Keller *et al.*, Science **285**, 1706 (1999)

Missing peaks

Randomly formed multiple islands



No control over whether an electron can be added to a particular island.

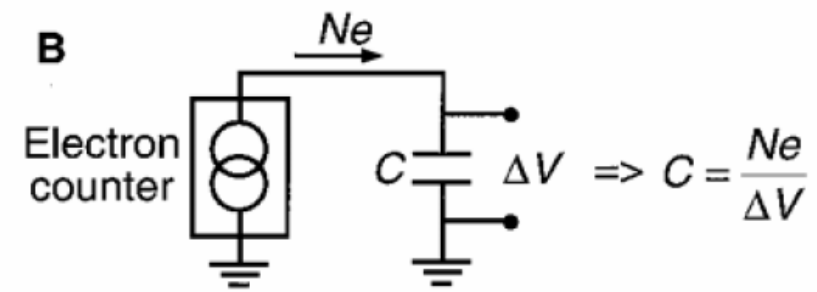
Non closed CB diamonds

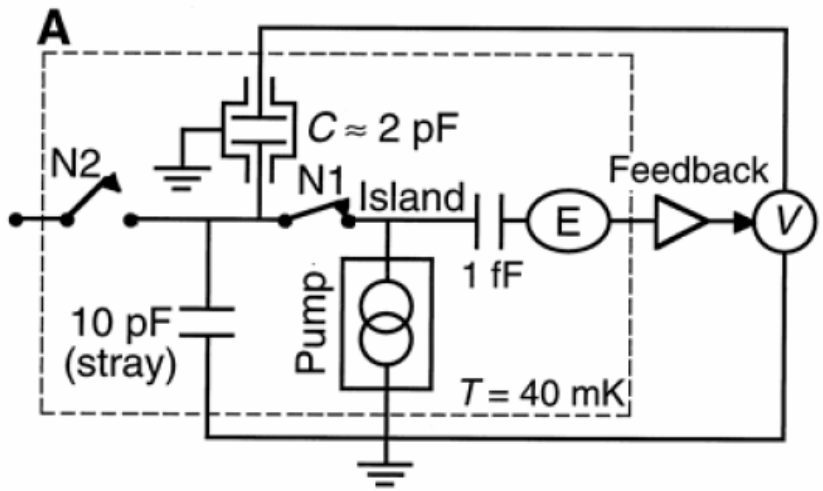
Capacitance standard

Even slow pumping of electrons can be very useful.

Capacitance standard:

- Make a capacitor.
- Pump a precisely known number of electrons onto the capacitor (*e.g*. with the 7-junction pump).
- Measure the capacitor voltage precisely.
- $Q = CV$ gives the capacitance.





M.W. Keller *et al.*, Science **285**, 1706 (1999)

Electrometry

Current flow through SET can be modulated between maximum and minimum values by moving a *single electron* off and on the gate:

One possible generalization: have the island be a moveable probe!

$$\frac{G}{G_{\max}} \approx \cosh^{-2}\left[\frac{e(C_g / C_{eq})\cdot(V_g^0 - V_g)}{2.5k_BT}\right]$$

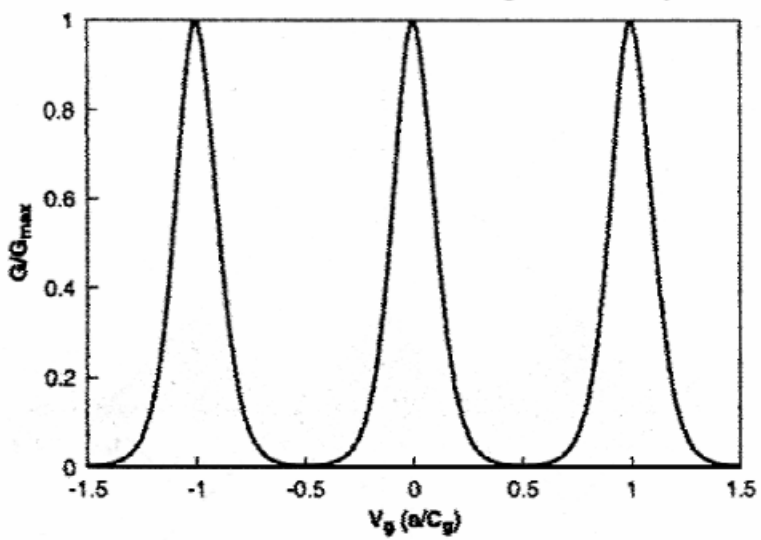
As the island capacitively couples to test objects, its polarization charge Q_p changes.

This shifts the G vs. V_G plot at right.

From our SET analysis,

$$V_0' \equiv V_0 + Q_p / C_g$$

image from Ferry



Electrometry

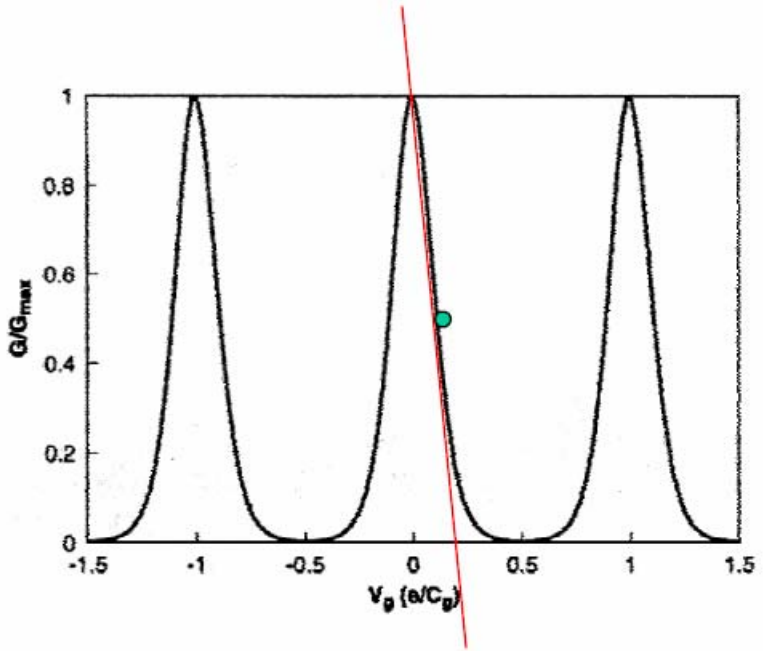
Basic idea:

Bias gate voltage to point where G vs. V_G is most rapidly varying.

Apply a small source-drain voltage to measure G.

Then change the charge distribution near the island.

Small changes in V_0 lead to large changes in measured source-drain current.



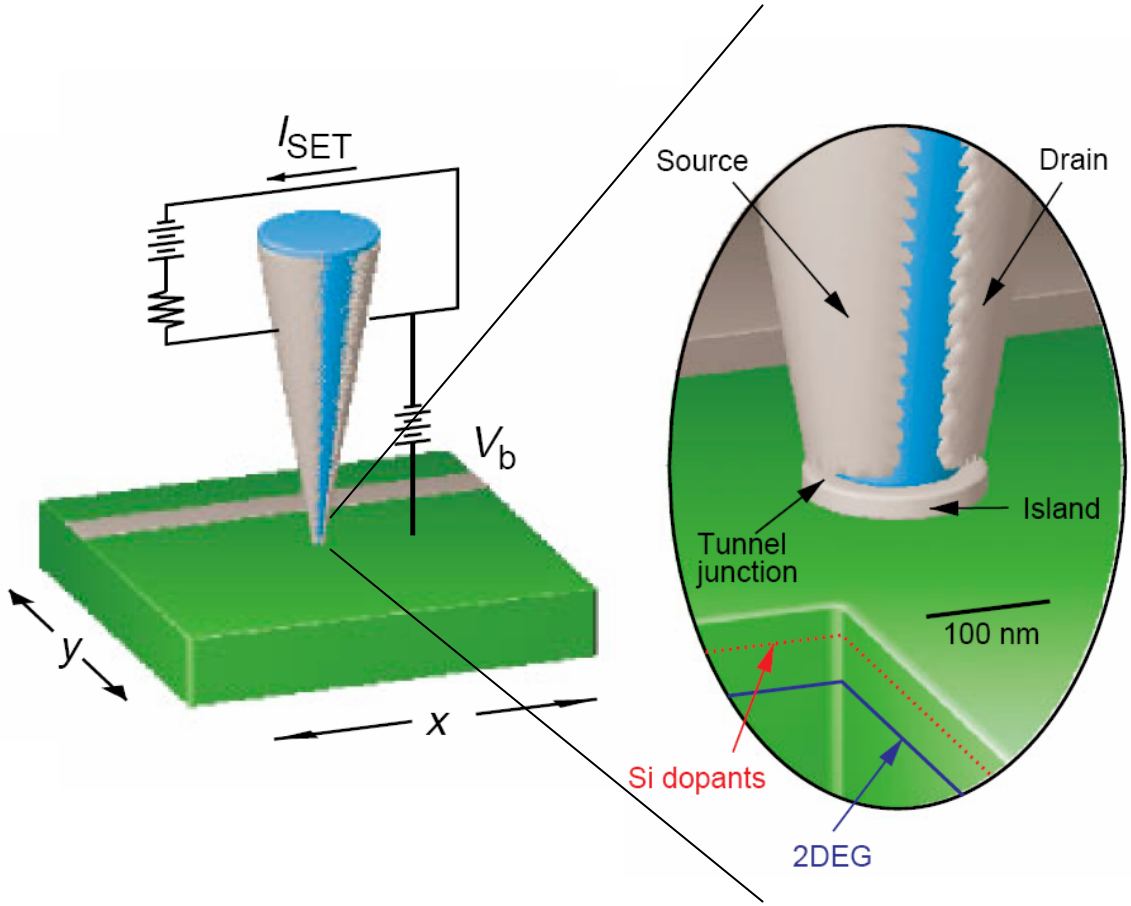
Sensitivity limits possible: $< 10^{-5}\ e/\mathrm{Hz}^{1/2}$

In another word, potential >GHz bandwidth for single electron detection.

Scanning SET electrometer

One adaptation of this is to place the island on a movable tip, and scan it over a surface.

Result: the SET scanning electrometer (SETSE).



Yoo, Science, **276**, 579 (1997)

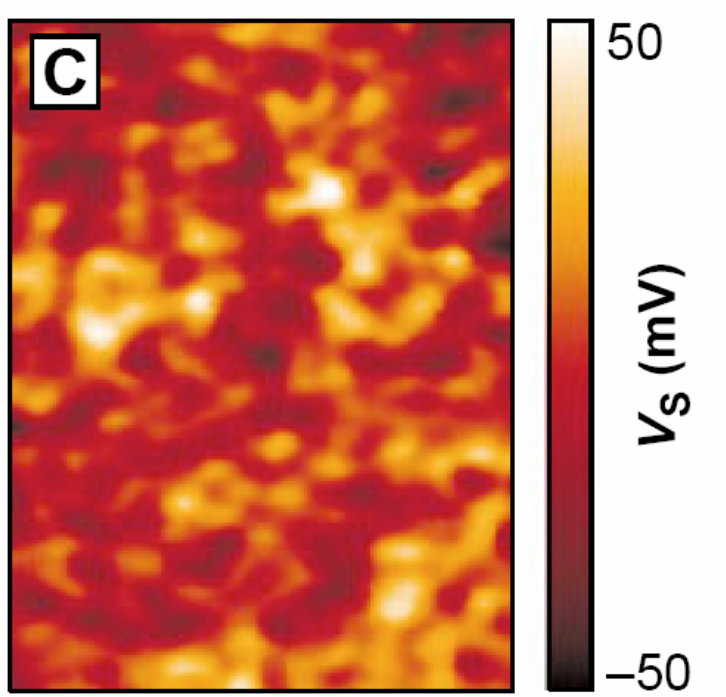
Scanning SET electrometer

Individual charged Si dopant atoms

SETSE is easily sensitive enough to see surface charge fluctuations caused by individual dopant atoms in semiconductor.

Problems:

- slow
- fragile
- requires quite low *T*.



Yoo, Science, **276**, 579 (1997)

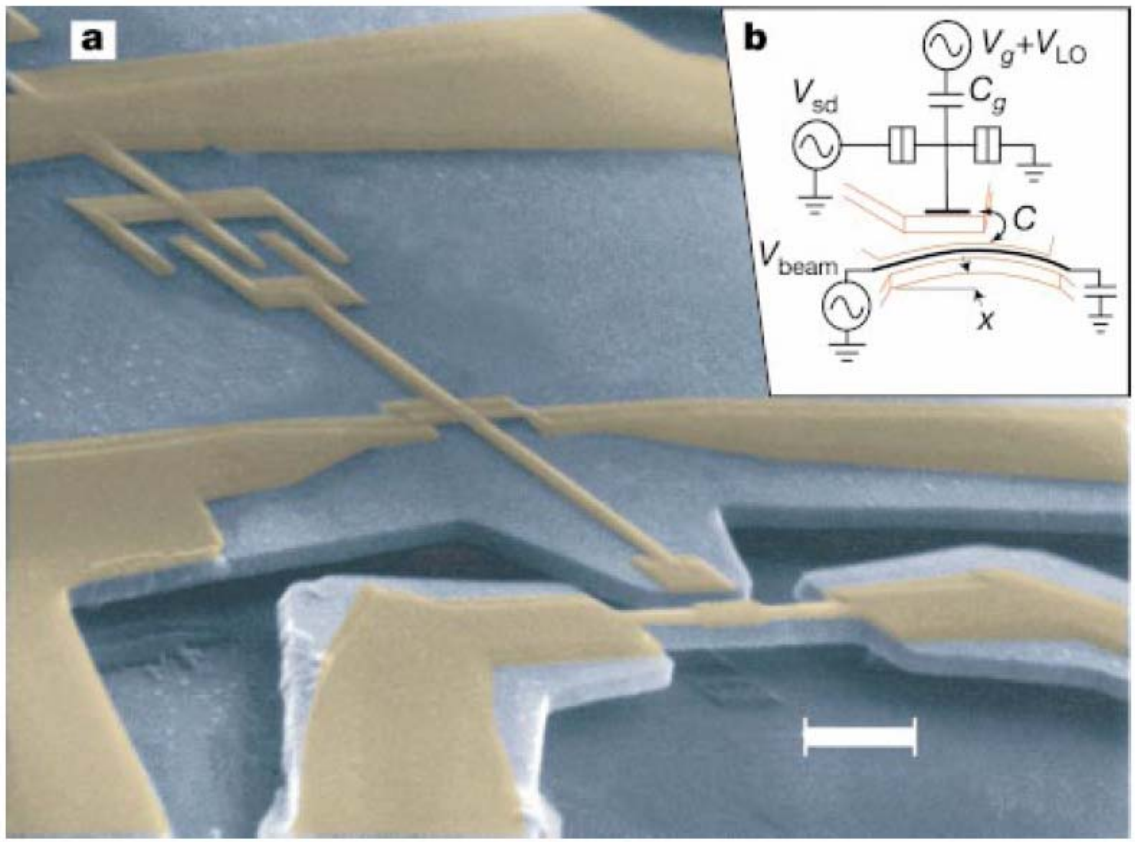
SET as displacement meter

G sensitive to $C_g V_g$, C_g determined by spacing between the SET island and device under test.

Sensitivity of

$$2 \times 10^{-15}\,\mathrm{m}/\sqrt{\mathrm{Hz}}$$

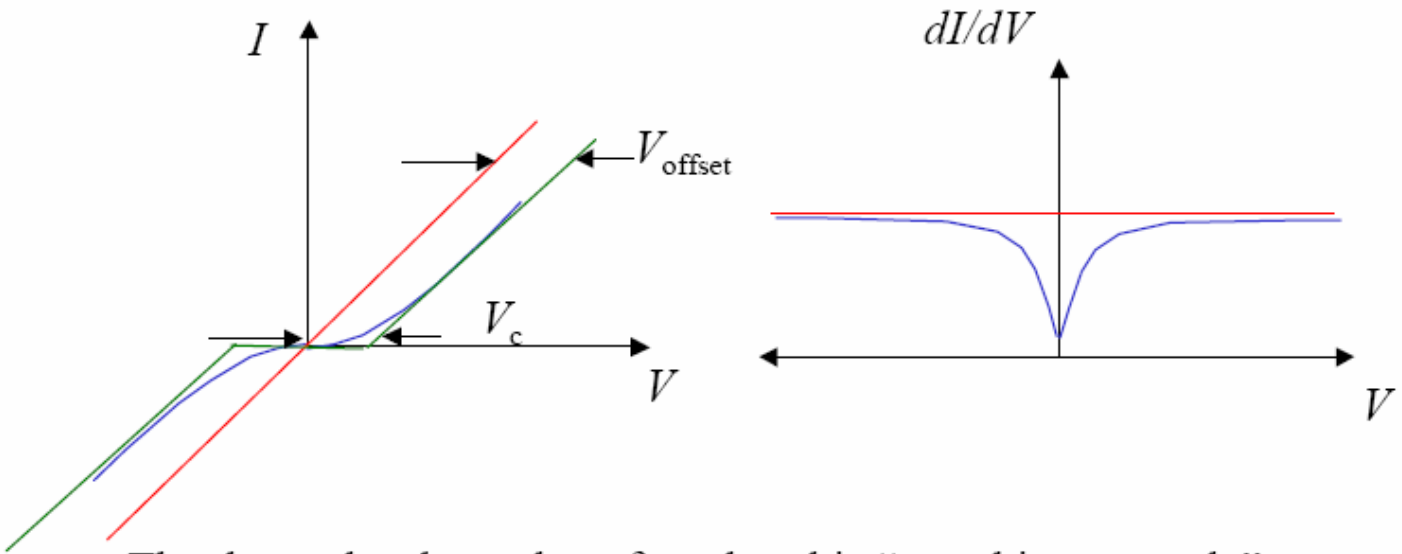
has been obtained.



Knobel, Nature, **424**, 291 (2003)

Coulomb blockade thermometry

Remember that a single junction (or for that matter, an array of junctions), when voltage biased, leads to an IV curve that looks like:



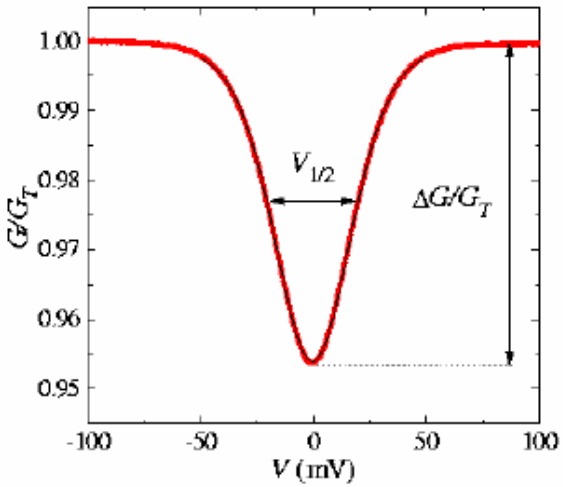
The theory has been done for what this "zero-bias anomaly" looks like as a function of temperature for a 1d array of tunnel junctions.

Coulomb blockade thermometry

$$G/G_T = 1 - (\varepsilon_c/k_BT)g(eV/Nk_BT)$$ N, # of junctions

$V_{1/2} = 5.439Nk_BT/e$ **primary thermometer** Calibration not needed.

$\Delta G/G_T = \varepsilon_c/6k_BT$ **secondary thermometer** Need calibration to determine E_c, the charging energy.



Normalised conductance, G/G_T, of a CBT sensor against bias voltage V. The theoretical curve is shown as a black line.

$$g(x) = [x\ \sinh(x) - 4\ \sinh^2(x/2)]/8\ \sinh^4(x/2)$$

Pekola, PRL, 73, 2903

Coulomb blockade thermometry

- Can improve reliability by having parallel 1d arrays.
- 2d arrays also work, with essentially identical function for ZBA width (though high temperature corrections are different).
- Work from 30 K down to < 20 mK, with basically no *B* dependence and comparatively low power dissipation!

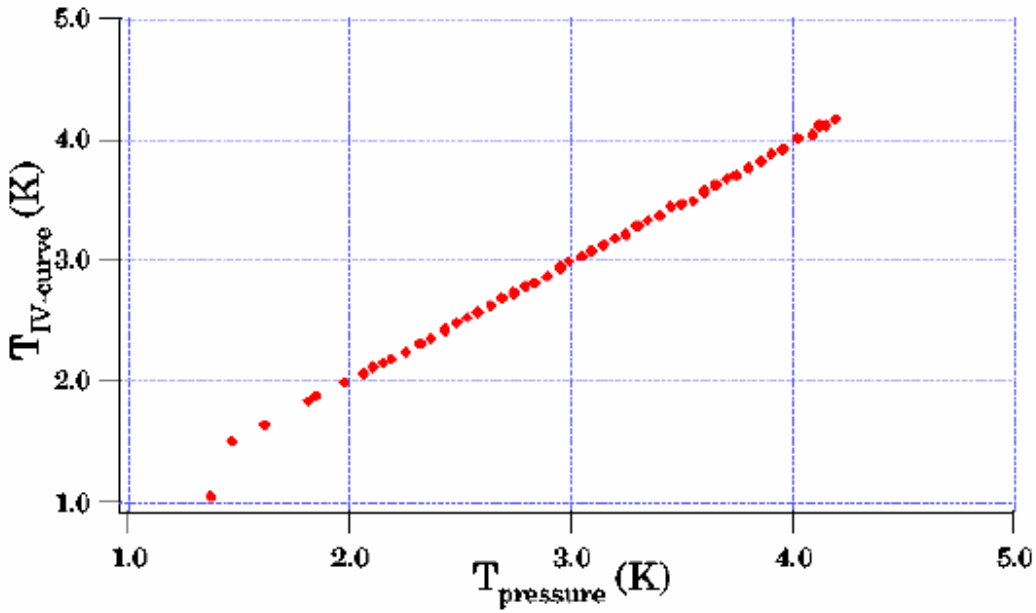


image from Bergsten *et al.*, Chalmers, Sweden