Carbon Nanotube Field Effect Transistors

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New Devices

Device Scaling:

→ reaching fundamental physical limitations
(tunneling, leakage current, hi power consumption)

→ can not shrink devices much more

→ same technologies but new material

- Carbon Nanotubes (CNT)
- Organic Molecules

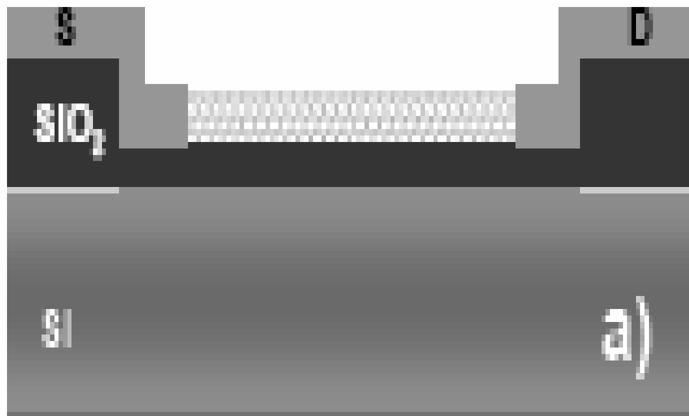
Single-Walled CNT

Single atomic layer of carbon's graphite structure

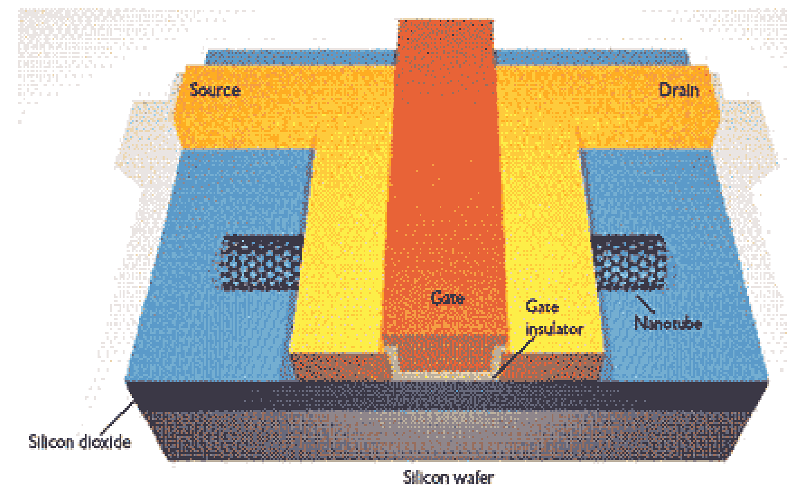
- 1D system: carriers propagate forward or backward
- no small angle scattering of electrons or holes by defects or phonons
- ~ no backscattering → lower resistivity
- ballistic characteristic in ~ 100nm
- no need to use SiO_2 as gate insulating film
- good control over the critical dimension: diameter
- high chemical stability and robustness

SW-CNT FET

source/drain: metal or electrostatically “doped” CNT
carrier transport region: SW-CNT



(Javey, 2003)



(Avouris,)

SW-CNT FET Operation

- Initially assumed that gate voltage modified the nanotube conductance.
- Now we know it is the Schottky Barrier (SB) at contacts that play a central role in the switching characteristic
- When SB is large enough to block current, switching occurs by modulation of contact resistance
- For small SB, conventional channel limited FET (depends on channel conductance)

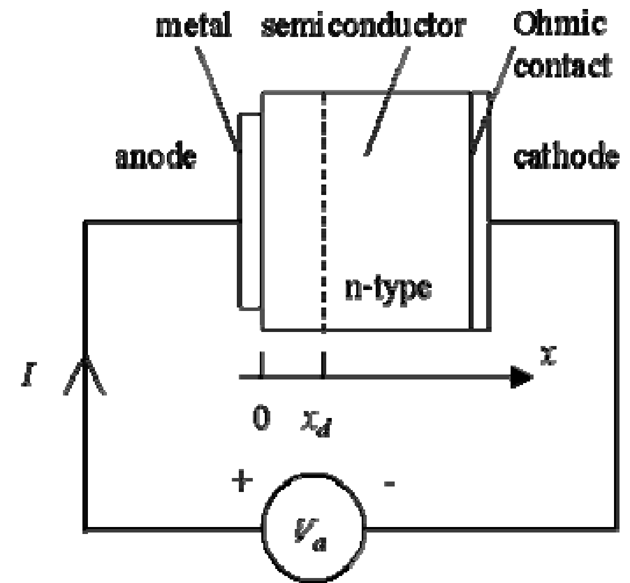
Metal-Semiconductor Junction

Ohmic Contact:

No potential difference between metal and semiconductor

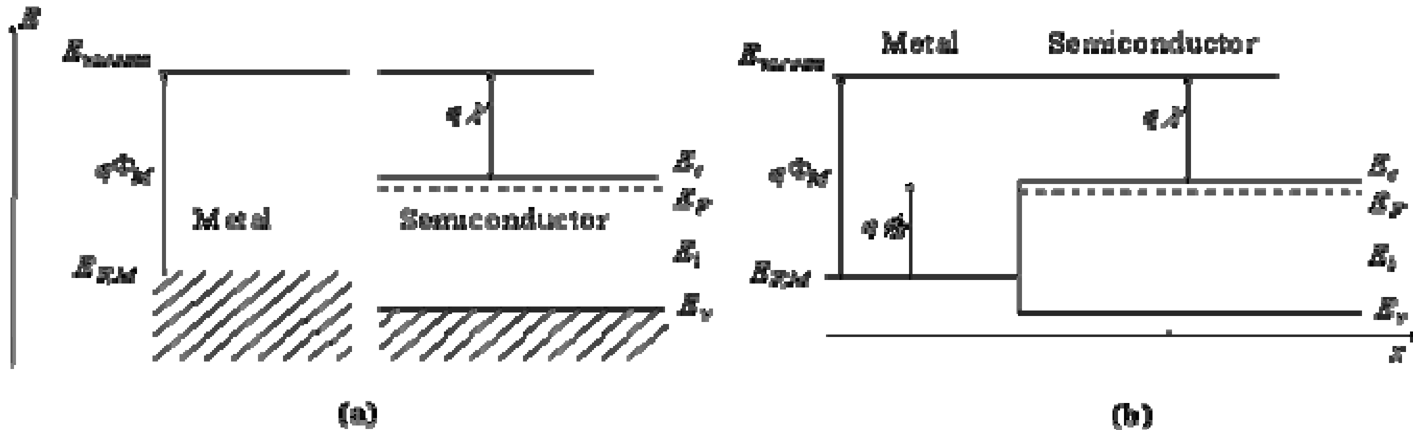
Schottky Diode:

Potential barrier between metal and semiconductor



Zeghbroeck, 2004

Schottky Diode



Zeghbroeck, 2004

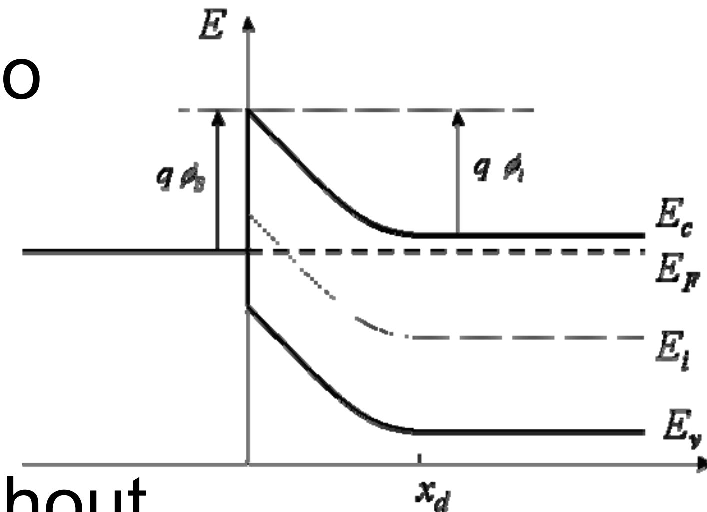
$$\phi_B = \phi_M - \chi$$

$$\phi_B = \frac{E_g}{q} + \chi - \phi_M$$

Potential Barrier: Difference between Fermi energy of metal and the band edge with the majority carriers

Thermal Equilibrium

- Electrons diffuse from n-type to metal
- Electrons drift from metal to n-type
- Constant Fermi energy throughout the device



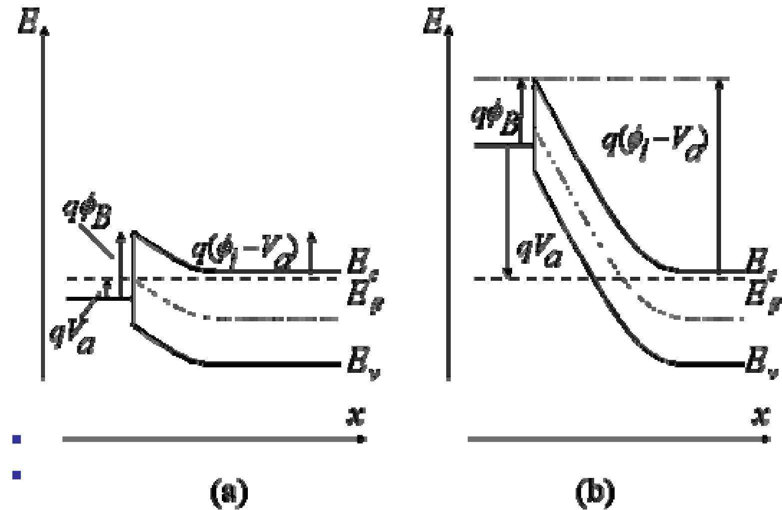
Zeghbroeck, 2004

Forward & Reverse Bias

Positive voltage on metal:

Current through device

(Forward Bias)



Negative voltage on metal:

~ No current through device

(Reverse Bias)

Zeghbroeck, 2004

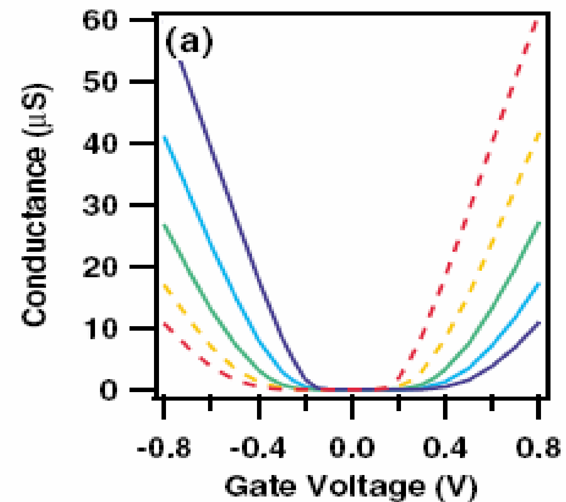
Schottky Diode Current

- Diffusion:
  carriers move from hi concentration to low
- Tunneling:
  electron waves penetrate the barrier
  depends exponentially on the barrier height
- Thermionic Emission:
  energetic carriers cross the barrier

Schottky Barrier & CNT-FET

- ON current depends on SB
- SB is sensitive to metal work function
- Metal work function is sensitive to absorbed gases, such as O2

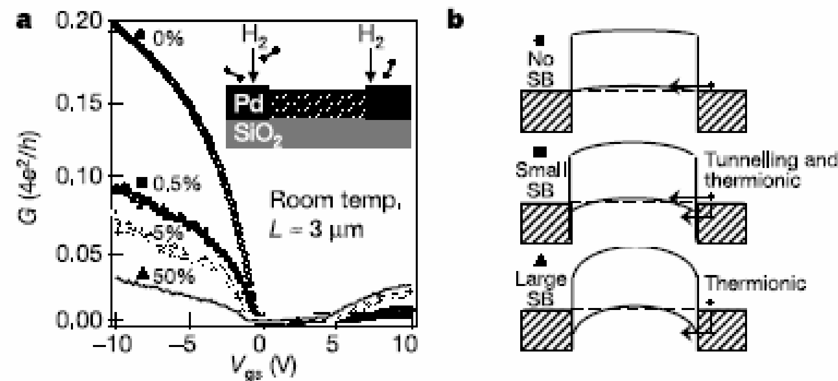
- Increasing work function reduces SB for p-type
- Decreasing work function reduces SB for n-type



(Heinze, 2002)

Schottky Barrier & CNT-FET

- exposure of Pd to molecular hydrogen reduces its work function at room temperature
- experiment results:
  - higher SB for holes: decreased p-channel conductance
  - lower SB for electrons: increased n-channel conductance



(Javey, 2003)

CNT-FET Devices

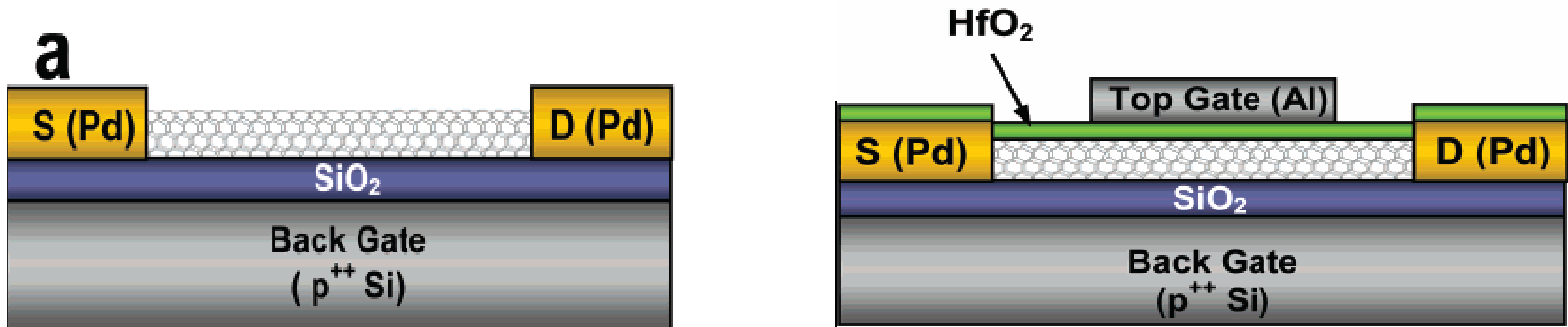
- MetalSD-FET

  metal electrodes as Source/Drain (S/D)
- DopedSD-FET

  electrostatically “doped” CNT as S/D

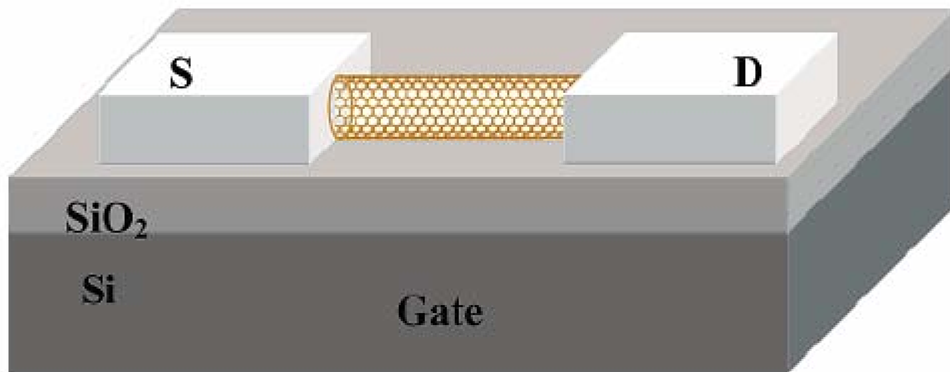
  channel: CNT below top gate region

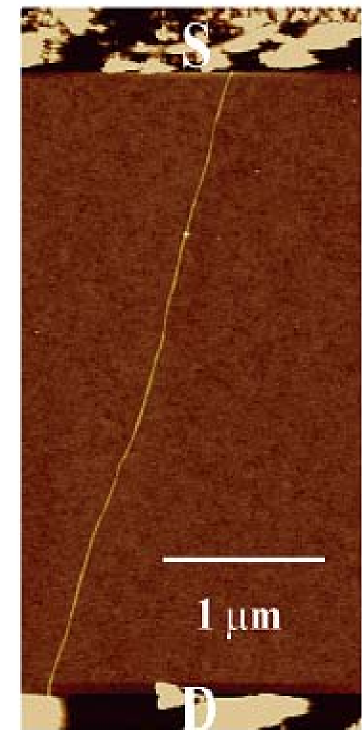
  S/D electrodes: CNT outside top gate region



(Javey, 2004)

Complementary CNT-FET



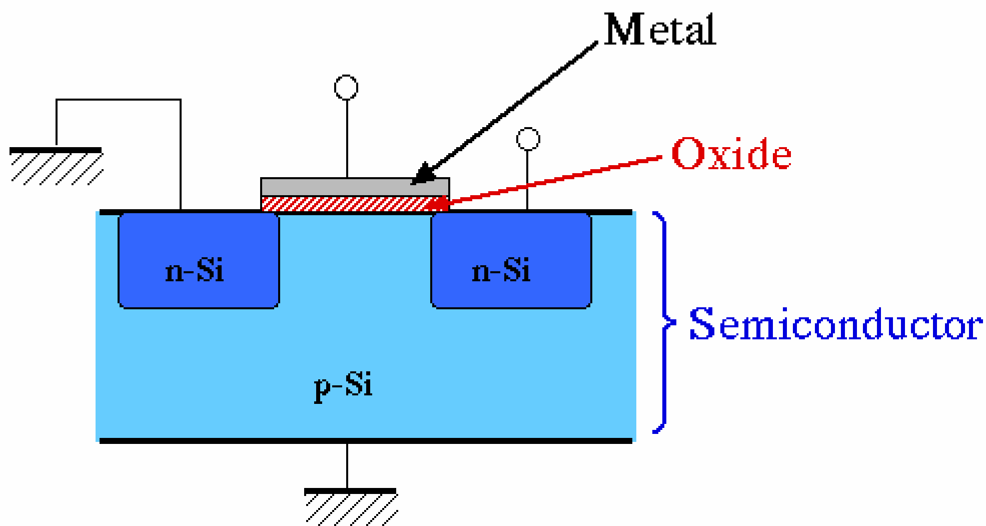


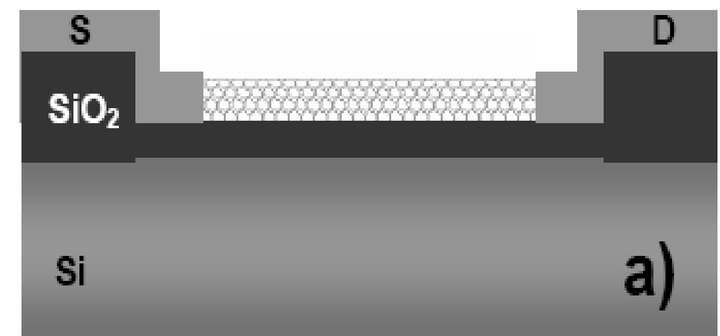
Traditional CMOS

- CMOS circuits utilize 2 types of MOSFET devices to create circuits
- n-channel (n-FET) and p-channel (p-FET) transistors are the foundation of analog and digital circuits
- In order to replace the current CMOS technology, CNT-FETS must offer a comparable option to each of the MOS types

Simplest Design

- The simplest case for creating a CNT-FET is to use the whole nanotube as a channel with a Source and Drain contact





Javey, 2003

C1

Operation of a MOSFET

- Source and drain are created in a substrate that has the opposite doping profile (no channel for charge to flow)
- Gate (Metal or Poly-Silicon) controls the formation of the channel
- Above a certain voltage, a channel of charge carriers is created and charge can flow

Similarities in operation

- The operation of a CNT-FET can be modeled on the operation of a MOSFET
- The SWCNT behaves as the channel for the charge carriers
- The gate voltage controls whether the channel conducts
- The function of the source and drain (for charge carriers) is also the same

Differences

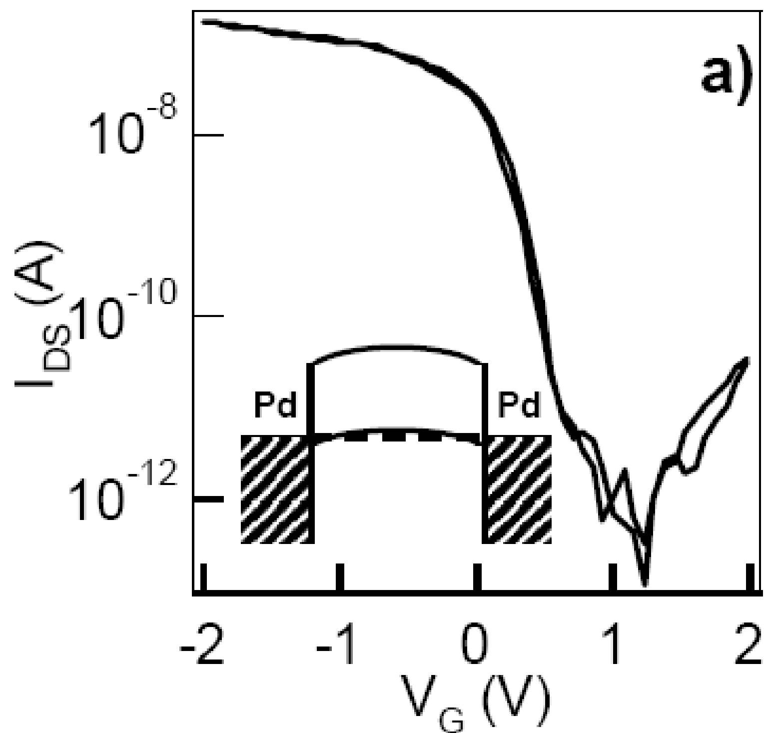
- The Source and Drain (S/D) contacts are formed using metals instead of heavily doped Si
- In a simple CNT-FET, no doping is needed to create a n-type or p-type FET
- The type of CNT-FET depends on the band-gap of the CNT and the work function of the metal used as the S/D contact

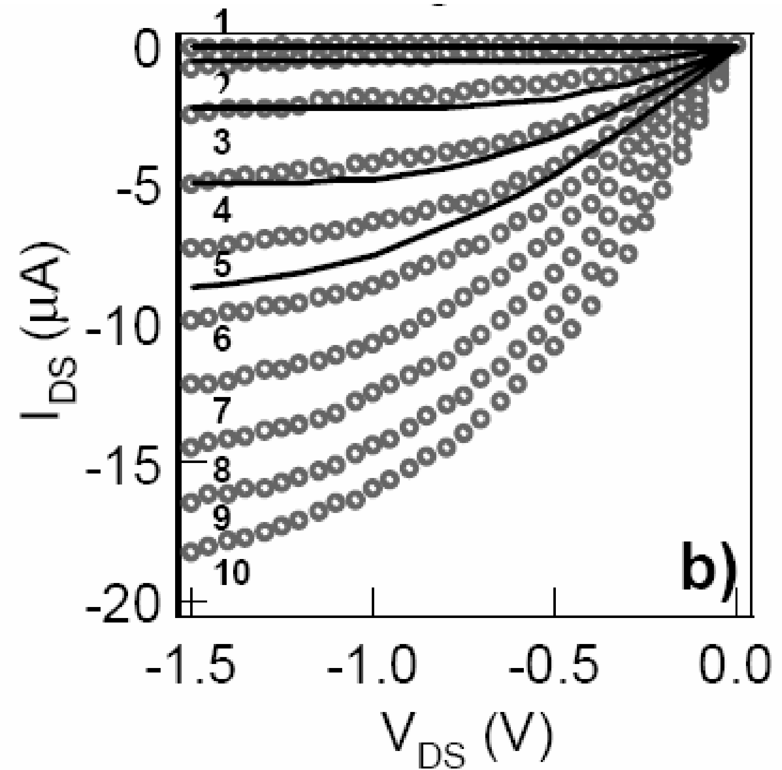
S/D Contacts (PMOS)

- The best case scenario is an Ohmic contact between the S/D and the CNT (zero or negative Schottky barrier height)
- In order to form a good Ohmic contact, the work function of the metal must be higher than the work function of the CNT
- The flow of holes in the channel can be controlled by the gate voltage

I-V curve of p-FET

- The I-V response the p-(CNT)-FET is similar to the response of a PMOS (Pd contacts



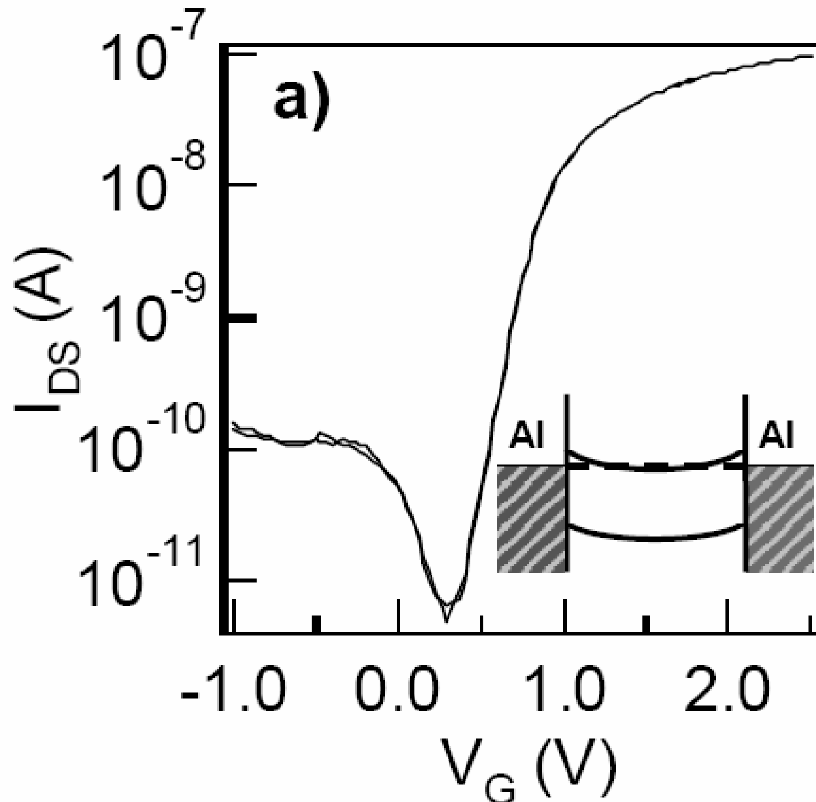


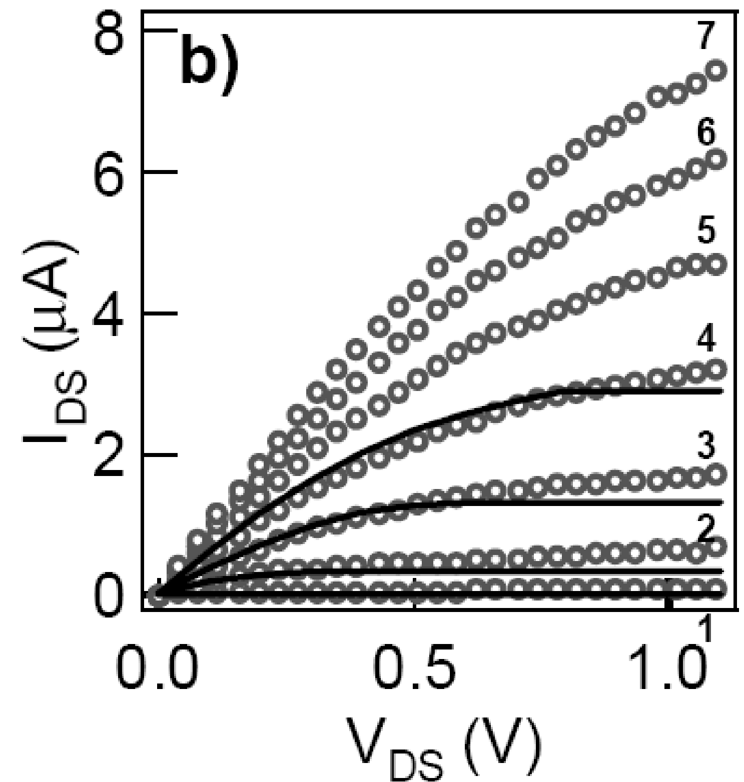
Analysis of I-V curves

- From the I-V curve of the p-FET, the following physical properties of the transistor were obtained:
  - Gon ~ 0.1-0.2 x $4e^2/h$ (Ron ~ 50 kOhms)
  - Gon/Goff ~ 10^5
  - μ_p ~ 3400 $cm^2/V*s$ - μ_p ~ 8000 $cm^2/V*s$ (depending on the height of the SBs at the interface)
  - Saturation current can be up to 20 μA
  - Subthreshold swing (S) = 100-150mv/decade

I-V Curve of n-FET

- An n-FET is created with a CNT of 2-3nm diameter and Al contacts





Analysis of n-FET I-V curve

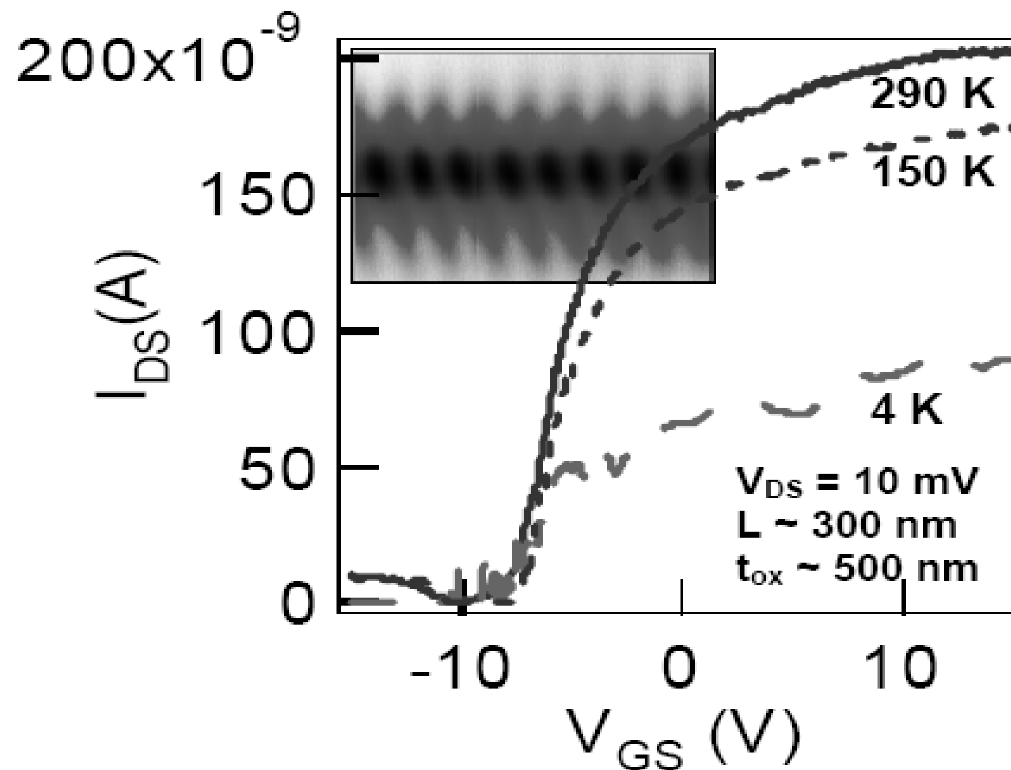
- From the I-V characteristics of the n-FET, the following properties were observed:
  - Gon ~ 0.05 x $4e^2/h$ (Ron ~ 100 kOhms)
  - Ion/Ioff ~ 10^4
  - μ_n ~ 3750 $cm^2/V*s$
  - Saturation current can be up to 10 μA
  - Subthreshold swing (S) = 150mv/decade

Comparison of n-FET and p-FET

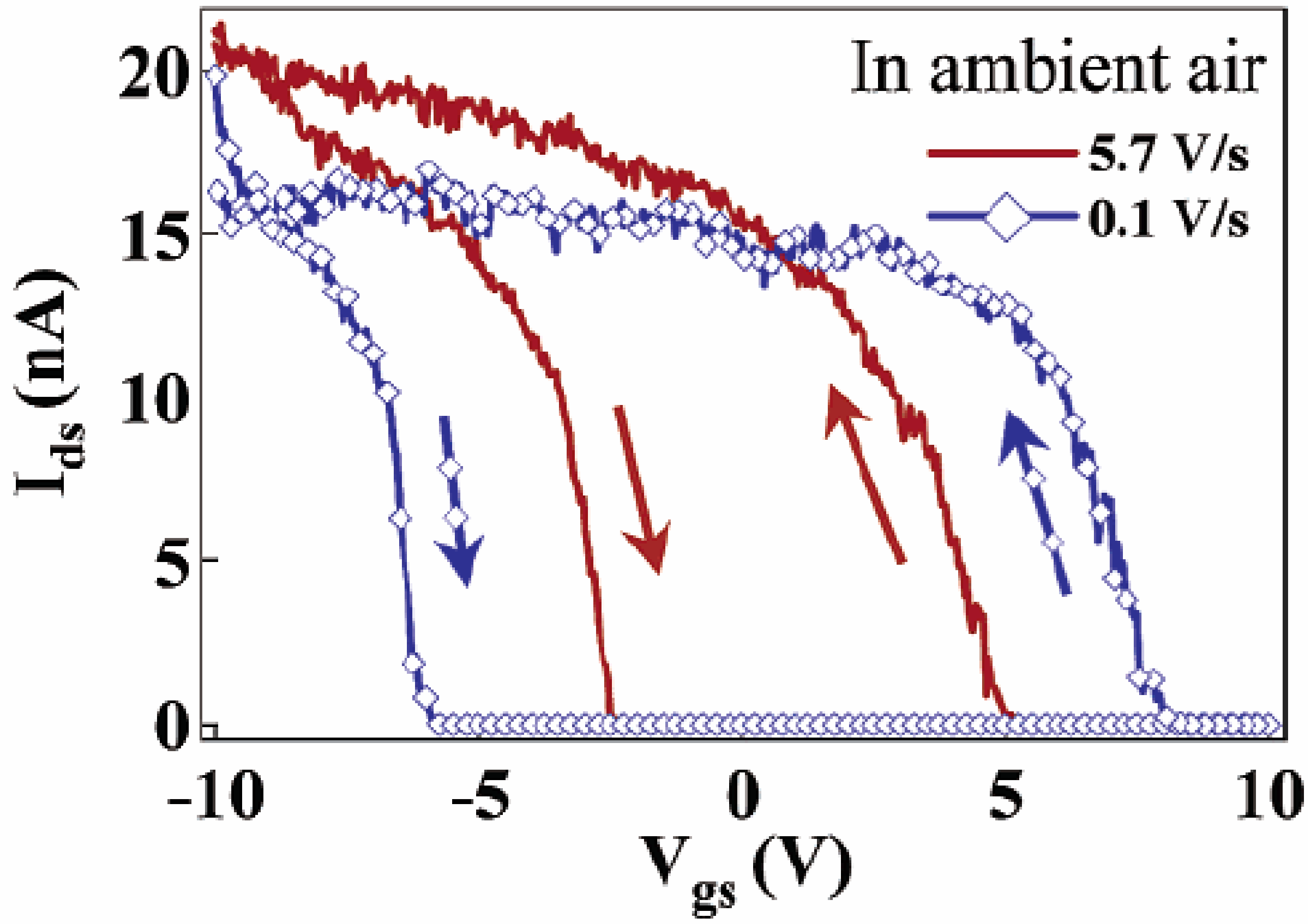
- Palladium (Pd) is the best contact metal found for p-FETS (no SB at the interface)
- Aluminum is used to create near Ohmic contacts with the SNT in n-FET
- Small SBs exist at the interface between Al and CNT
- Overall performance of p-FET is better than n-FETS

Ambient Factors

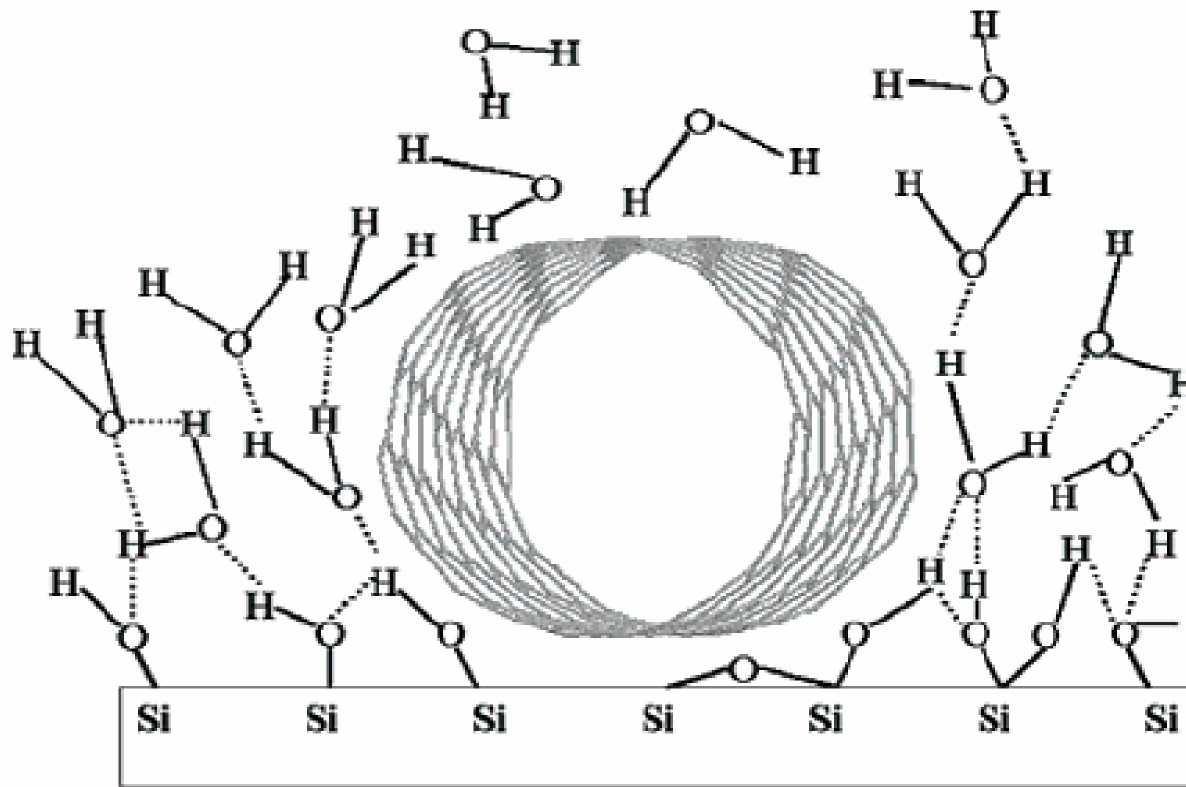
- The performance of CNT-FET also depends on the ambient temperature



I-V Hysteresis

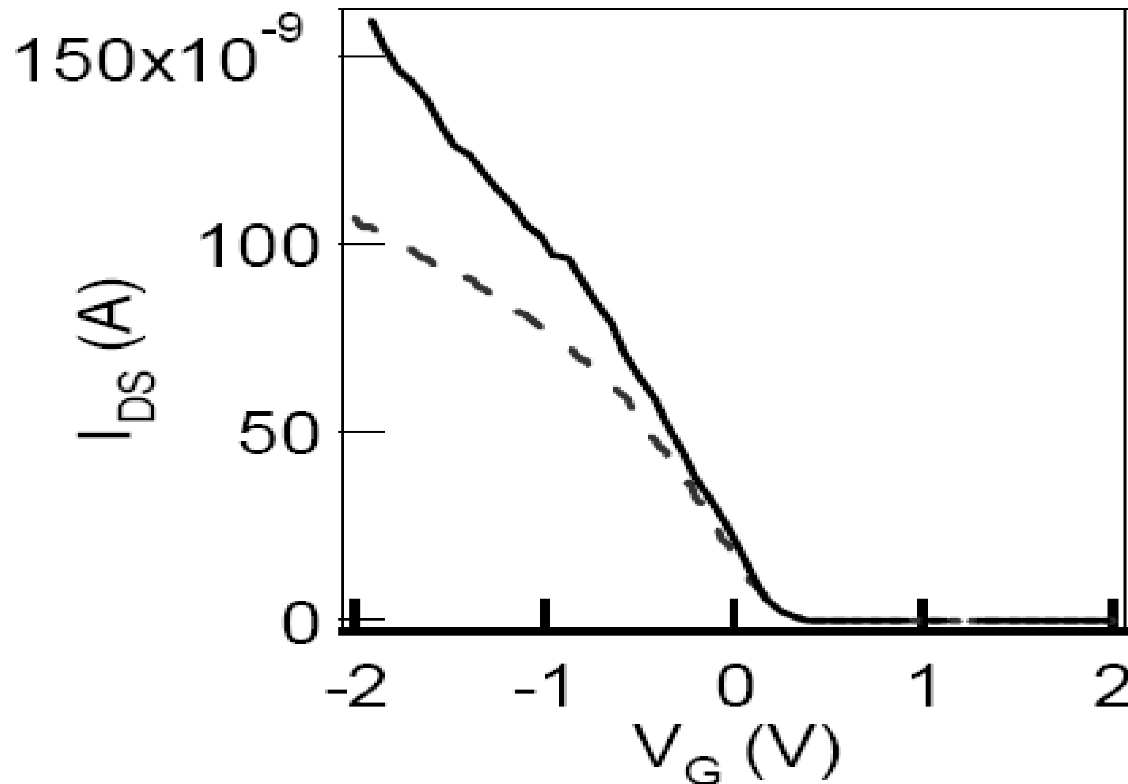


Possible Explanation



Solution

- A possible solution is to use PMMA passivation

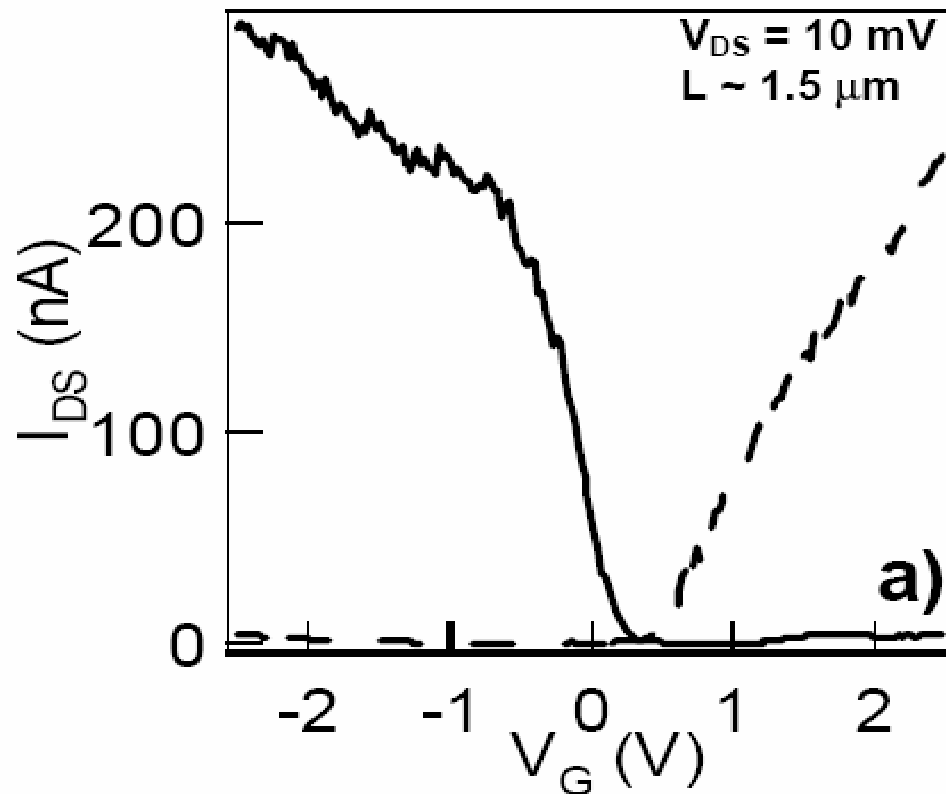


Threshold Voltage

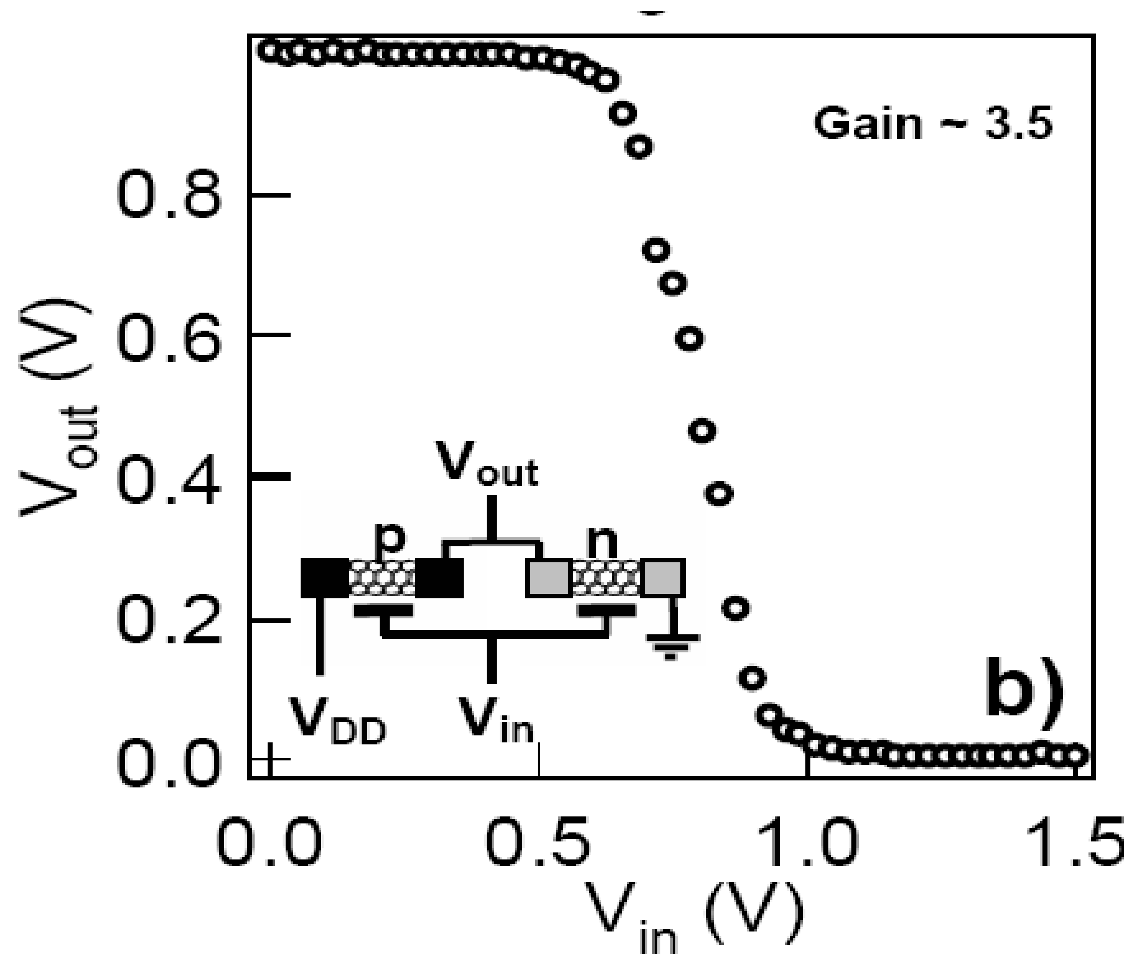
- For p-FET
  - Vth ~ 0.6V
- For n-FET
  - Vth ~ 0.3V
- The Vth can be reduced further with better gate materials
- Slight variations in Vth are present due to the variation in the diameter of the CNTs

Fabrication

- Fabrication of both n and p type CNT-FETs is possible on the same chip



Applications to logic circuits

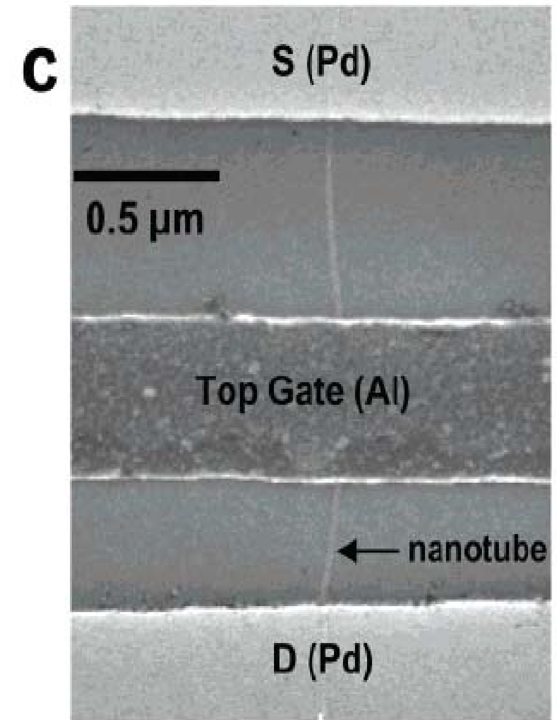


DopedSD-FET Fabrication

- form metalSD-FETs on SiO_2/p^+ Si subtrate
- 100nm SiO2 cover most areas of substrate
- 10nm SiO2 locally under channel region (grown by dry oxidation)
- Atomic Layer Deposition of 8nm HfO_2 film using alkylamid/150 °C
  - anneal at 180 °C for 2 hours after deposition
    → no unintentional p-doping of nanotubes
  - less degradation in Pd-SWNT contacts compared to $ZrCl_4$ ALD at 300 °C
- form top gate (Al)

DopedSD-FET Size

- SEM image of device
- total tube length ~2 μm
- top-gated section length ~ 0.5 μm
- tube diameter ~ 2.3nm



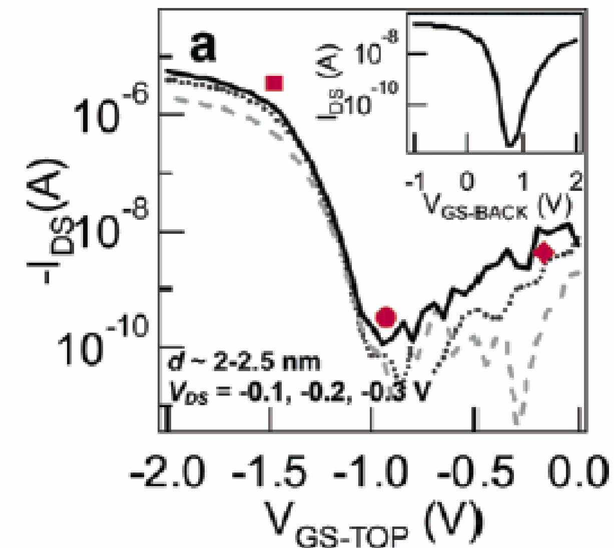
(Javey, 2004)

Electrical Properties

- tube diameter d~2.3±0.2nm
- g_m~20 μS (5000 S/m, normalized to 2d)
- I_{on_sat} ~15 μA & G_{on} ~ $0.1 \times 4e^2/h$

→ 5 times higher than Si p-MOSFET

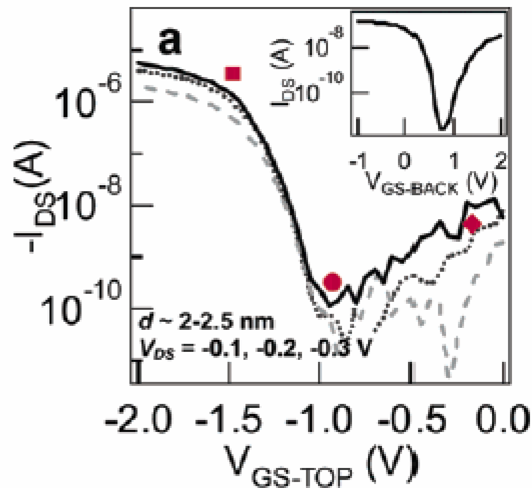
→ 3 times higher than DopedSD-FET with Mo electrodes

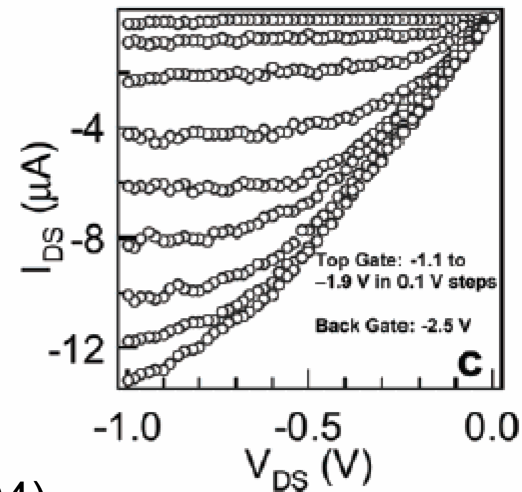


(Javey, 2004)

Electrical Properties

- subthreshold swing ~ 80mV/decade
- Bias-independent I_{min}
- $I_{on}/ I_{min} > 10^4$





(Javey, 2004)

Electrical Properties

Ambipolar Conduction:

- higher gate voltages
- electrons tunnel in the direction of drain to source
- increases off current

(Javey, 2004)

Electrical Properties

- comparable p-channel ON states for Pd MetalSD-FET and DopedSD-FET:

  I_{on} ~15-20 μA , G_{on} ~ $0.1x4e^2/h$

  → high-k deposition does not degrade ON state
- channel transmission = $L_{mfp}/(L_{mfp}+L)$ ~0.1

  relatively long tubes → nonballistic channel

  L: 3 μm→ Ron: 200k (nonballistic)

  L: 300nm→ Ron: 10kΩ (~ballistic)

Future Improvements:

Shrink channel length in top-gated & S/D tube segments

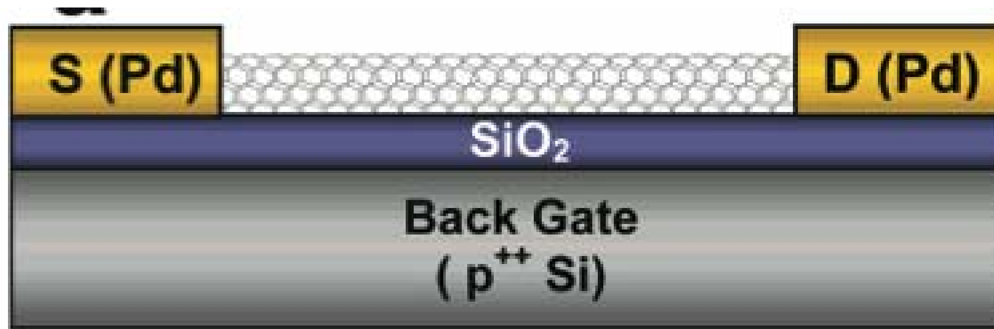
Require novel lithography and self-aligned processes

Properties of different CNT-FET device geometries

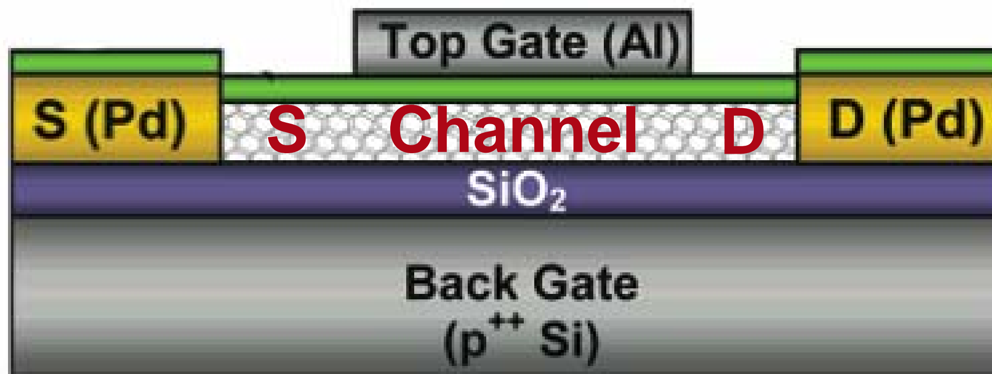
- Two geometries
  - *MetalSD-FET's*
  - *DopedSD-FET's*
- Comparison of critical device properties
  - I_{min}
  - *N-channel leakage current*

Reminder of device geometries

MetalSD-FET



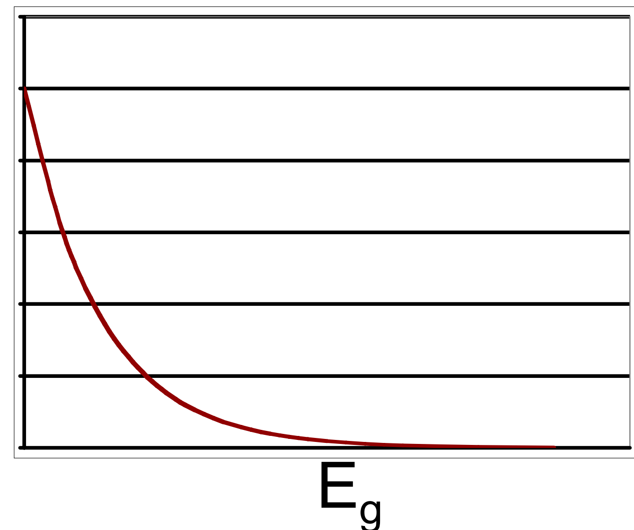
DopedSD-FET



MetalSD-FET: thick gate oxide

- SiO_2 (t_{ox}) ~ 67nm
- N-channel leakage
  - *Negligible*
- I_{min}
  - *determined by thermal activation over the full band gap of the tube*
  - $I_{ON}/I_{OFF} \sim 10^6$, $d>3$ nm $= E_g<0.4$ eV

$$I_{MIN} \propto \exp\left(-\frac{E_g}{k_B T}\right)$$



MetalSD-FET: thin gate oxide

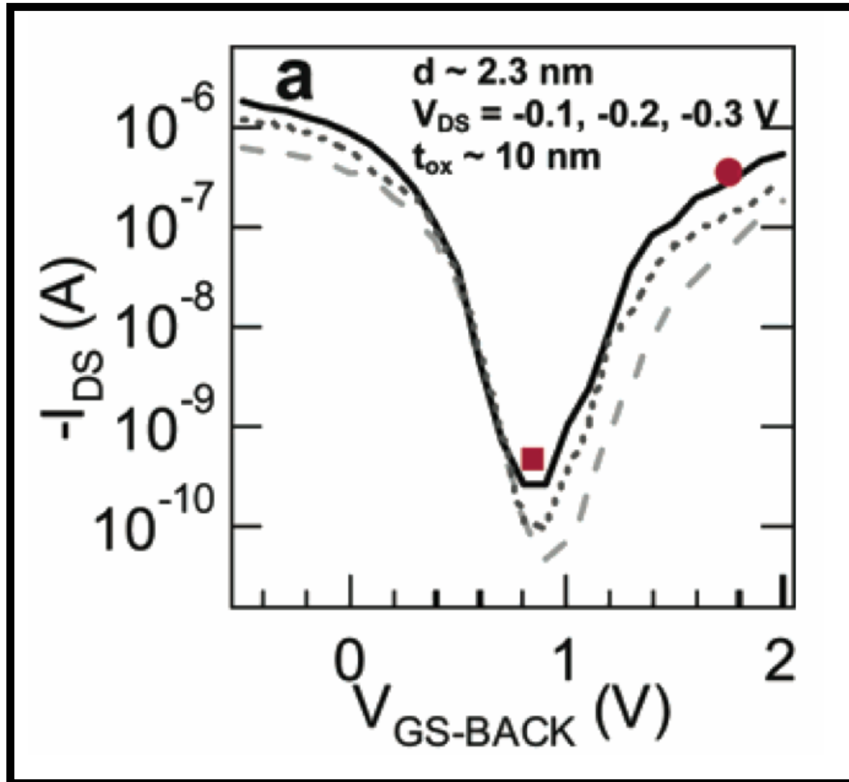
- What happens when keep scaling down FET?
- SiO_2 (t_{OX}) ~ 10nm
- N-channel leakage
  - *High*
  - *Ambipolar conductance*
  - *Due to thin SB (width SB ~ t_{OX})*
  - *Therefore tunneling through SB to conduction band of CNT*

MetalSD-FET: thin gate oxide

- I_{min}
  - *Higher for thinner gate oxides*
  - *Higher V_{DS} = higher I_{Min}*
  - *As scale MetalSD-FET*
    - *Unacceptable off-state current for useful operating voltages*

$$I_{MIN} \propto \exp\left(-\frac{(E_g - e|V_{DS}|)}{k_B T}\right)$$

MetalSD-FET: thin gate oxide

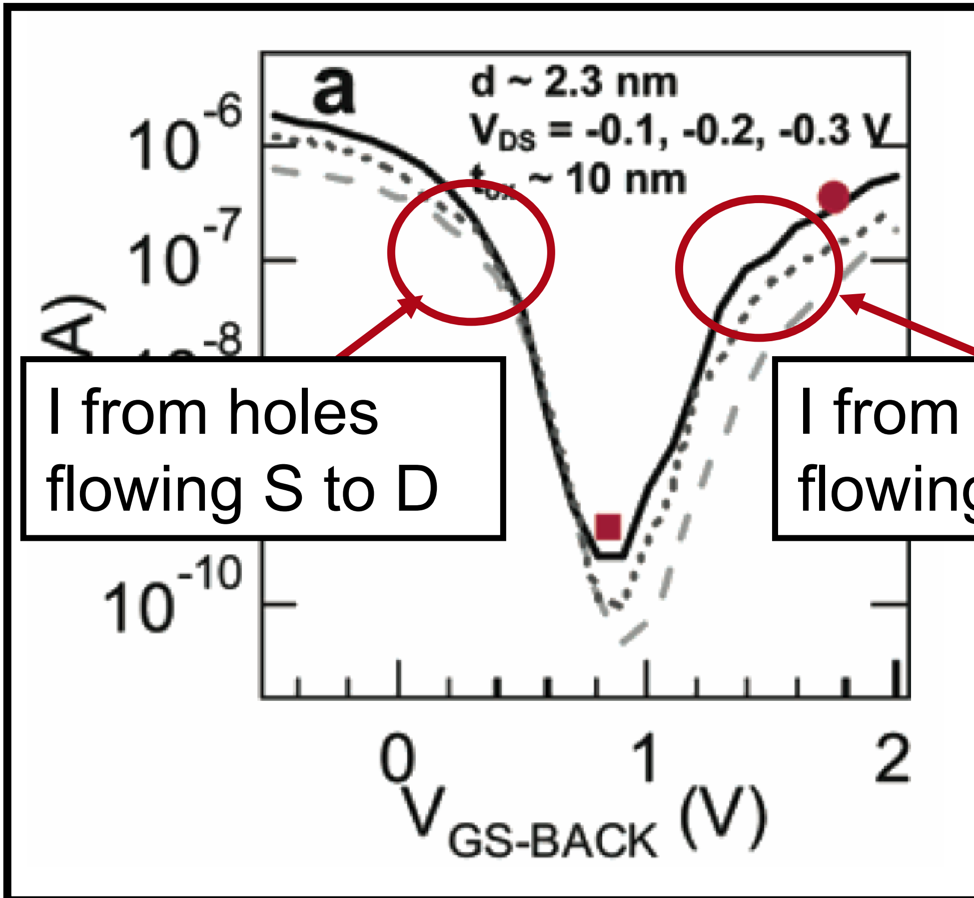


d~2.3 nm
SiO_2~10nm

Notice
1. Ambipolar

Current always flow from source to drain

MetalSD-FET: thin gate oxide



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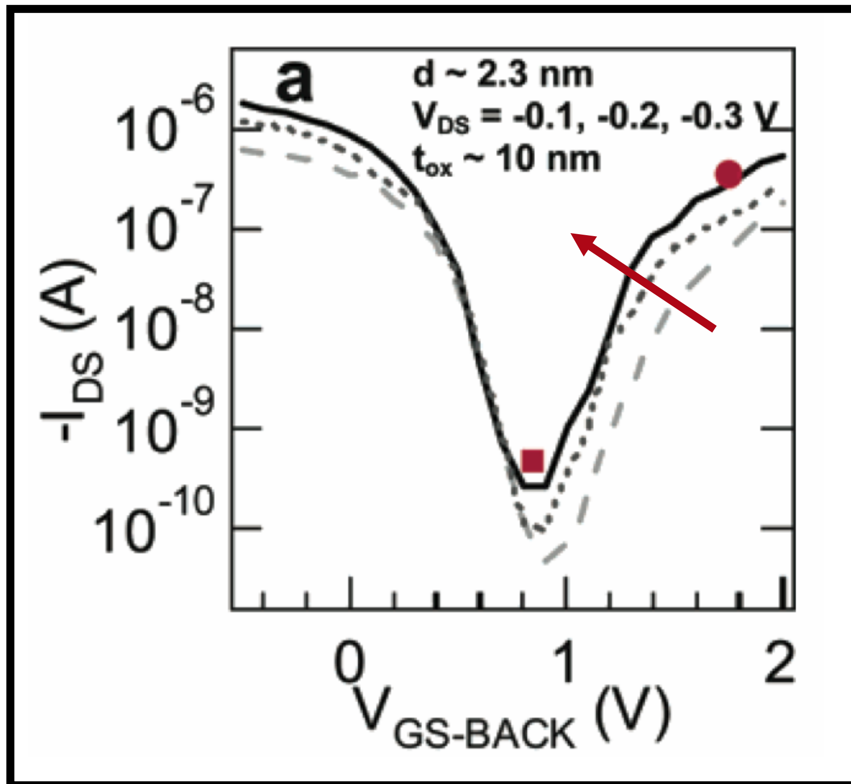
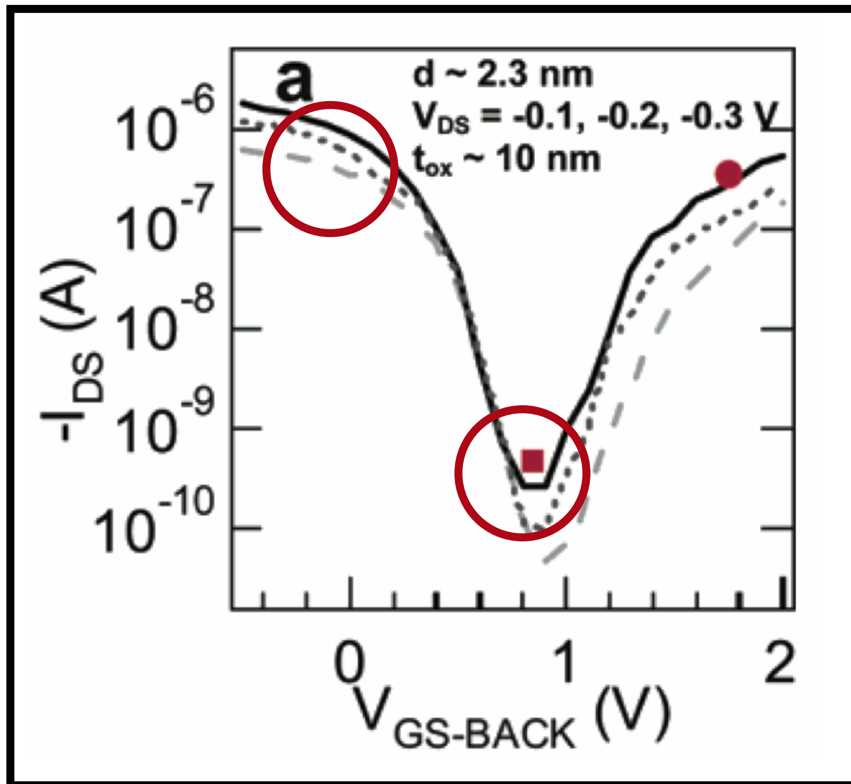


Notice

1. Ambipolar
2. Increasing I_{min} with increasing V_{DS}

Increasing bias voltage

MetalSD-FET: thin gate oxide



Notice

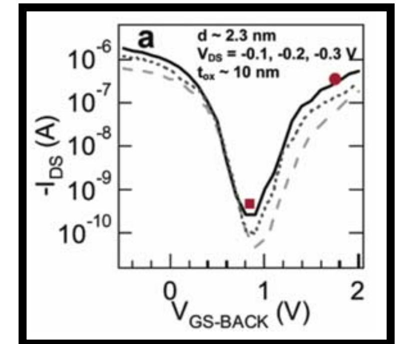
1. Ambipolar
2. Increasing I_{min} with increasing V_{DS}
3. I_{ON}/I_{OFF}

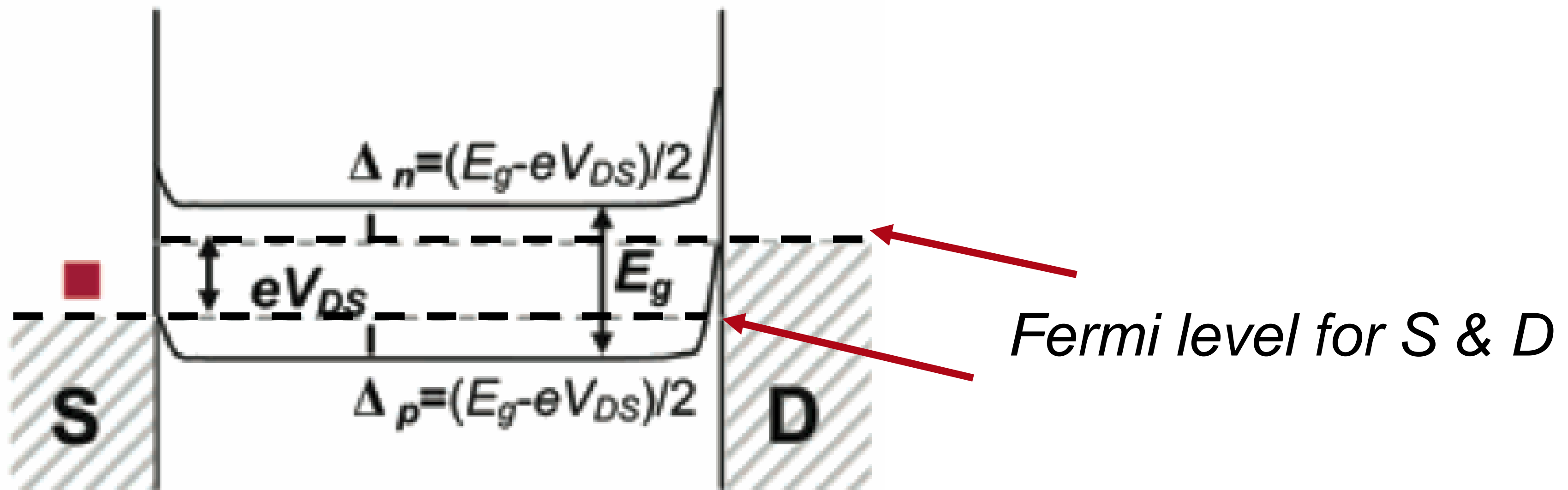
$I_{ON}/I_{OFF} \sim 10^3$

as compared to 10^6 for thick t_{OX}

MetalSD-FET: thin gate oxide

- Band diagram description
- V_{DS} & eV_{DS} constant
- Barrier to holes (Δ_p) = Barrier for e's (Δ_e)
  - $\Delta_p = \Delta_e (E_g - e|V_{DS}|)/2$





Fermi level for S & D

MetalSD-FET: thin gate oxide

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- V_{DS} & eV_{DS} constant
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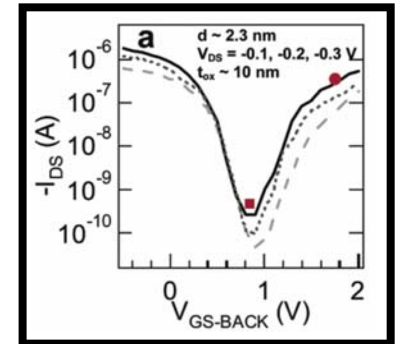


E_C

E_V

S

D

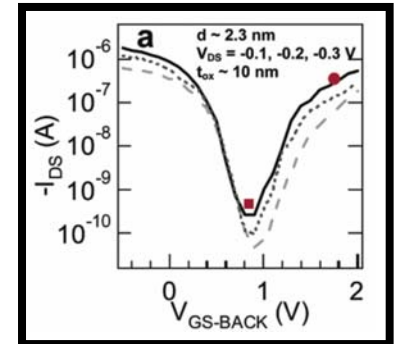
Barrier for electron tunneling

Fermi level for S & D

Barrier for hole tunneling

MetalSD-FET: thin gate oxide

- Fermi levels of source and drain remain constant
- Increase gate voltage
- E_V and E_C shift down
- Barrier larger for holes/smaller for electrons
- Electron tunneling produces current



eV_{DS}

Fermi level for S & D

E_C

E_g

S

D

E_V

MetalSD-FET: thin gate oxide

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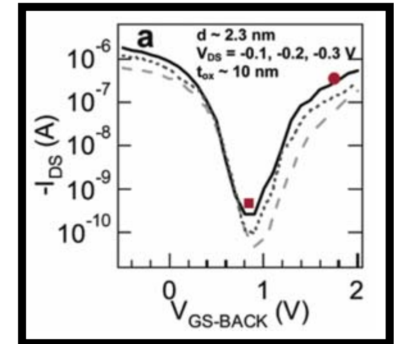


Barrier for electron tunneling

Barrier for hole tunneling

eV_{DS}

Fermi level for S & D

E_C

E_g

E_V

S

D

DopedSD-FET

- Advantages over scaled down MetalSD-FET's
  - Doped semiconductor S/D like traditional MOSFET
    - MetalSD-FET uses SB
  - Better ambipolar conductance behavior
  - Lower I_{min}
  - I_{ON}/I_{Min} ~10^5

DopedSD-FET device properties

- N-channel leakage current low
  - *High gate voltage for $I_{N\text{-}channel}$ compared to I_{ON}*
- I_{min}

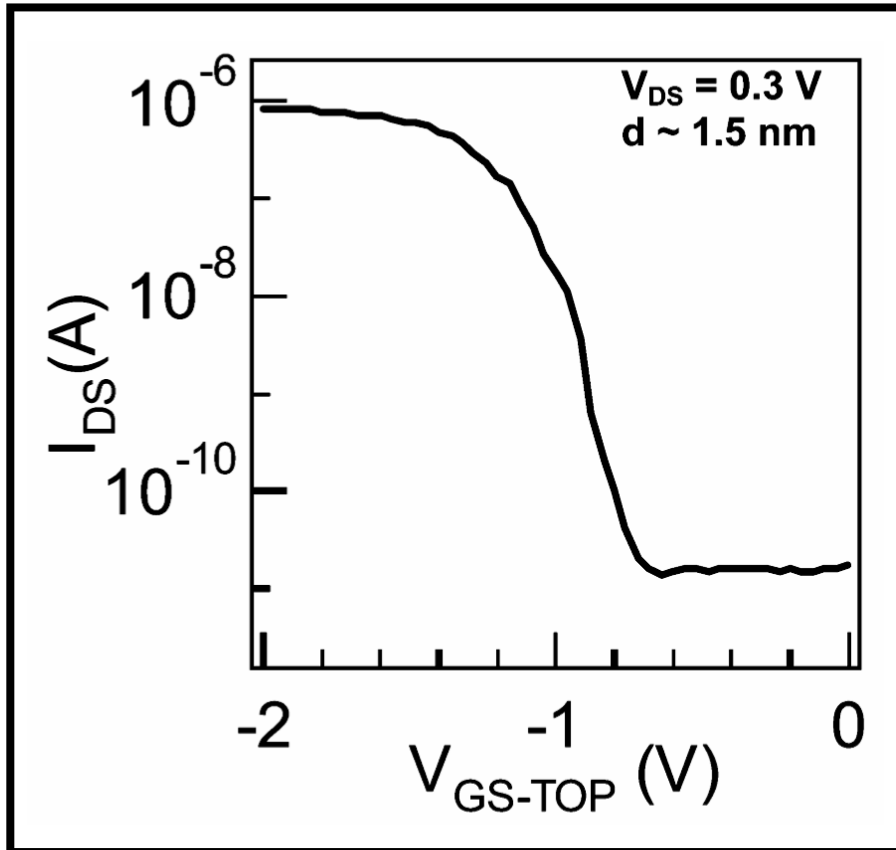
$$I_{MIN} \propto \exp\left(-\frac{(E_g - E_d)}{k_B T}\right)$$

E_d - energy spacing from E_V to E_F in p-doped SD

- E_d is the energy spacing from E_V to E_F in p-doped SD
- E_d is set by back-fate electrostatic doping
  - Ex: $V_{GS\text{-}Back}$ ~ -2V gives E_d ~ 0.2eV\
- I_{Min} no longer sensitive to V_{DS}

DopedSD-FET device properties

- Example of transfer characteristics of dopedSD - FET



Notice

1. No ambipolar behavior
2. Low off state current
3. $I_{ON}/I_{Min} \sim 10^5$

Excellent off states for DopedSD-FET with small d SWNT but at expense of lower I_{ON}

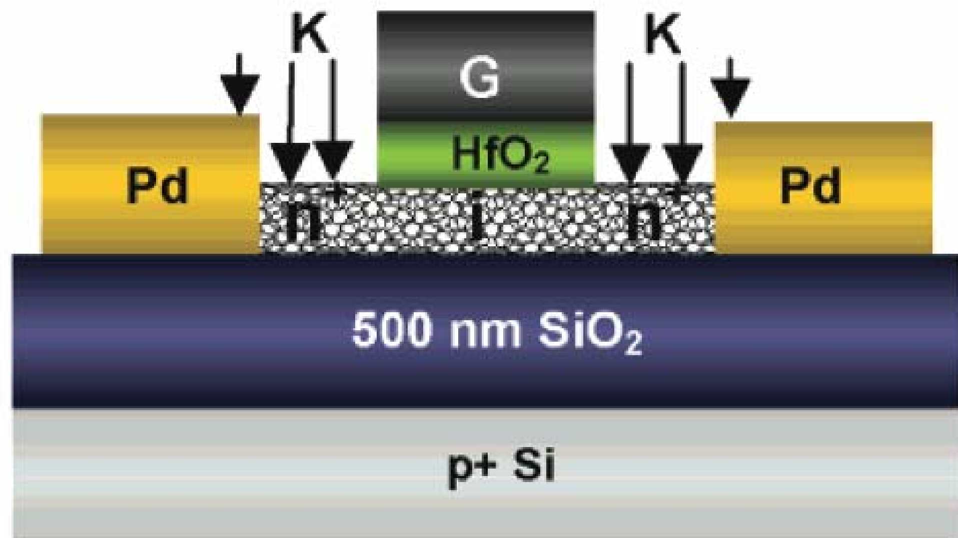
Summary

- Can create FET from SWNT by using schottky barriers
  - *MetalSD-FET*
- However, as scale down MetalSD-FET device properties become less desirable
  - I_{Min} *increases*
  - *Ambipolar behavior*
- By using a back-gate to create SD from SWNT itself, improve device performance at smaller dimensions

Chemically doped SWNT-FET

- Chemically dope SWNT to create SD as opposed to electrostatically doping
  - *Dope source and drain regions with potassium*
  - *Currently exposure to air reverses doping process due to reactivity of K*

Javey A, Tu R, Farmer DB, et al. NANO LETTERS 2005

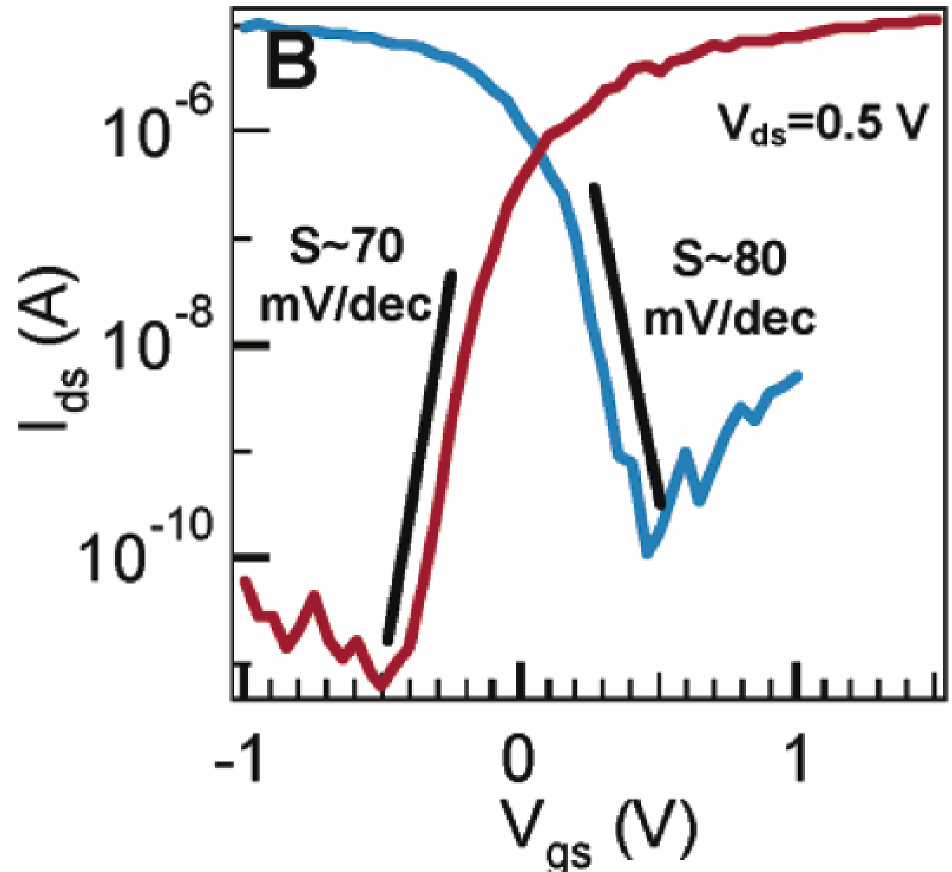


Chemically doped SWNT-FET

- N-type SWNT-FET
- For SWNT ~ 1.6nm & E_g~0.55eV
  - *Subthreshold swing ~ 70mV/decade*
  - *Small ambipolar behavior*
  - *I_{ON}/I_{OFF} ~ 10^6 @ V_{DS} ~ 0.5V*
  - *High on currents*

Blue = before doping

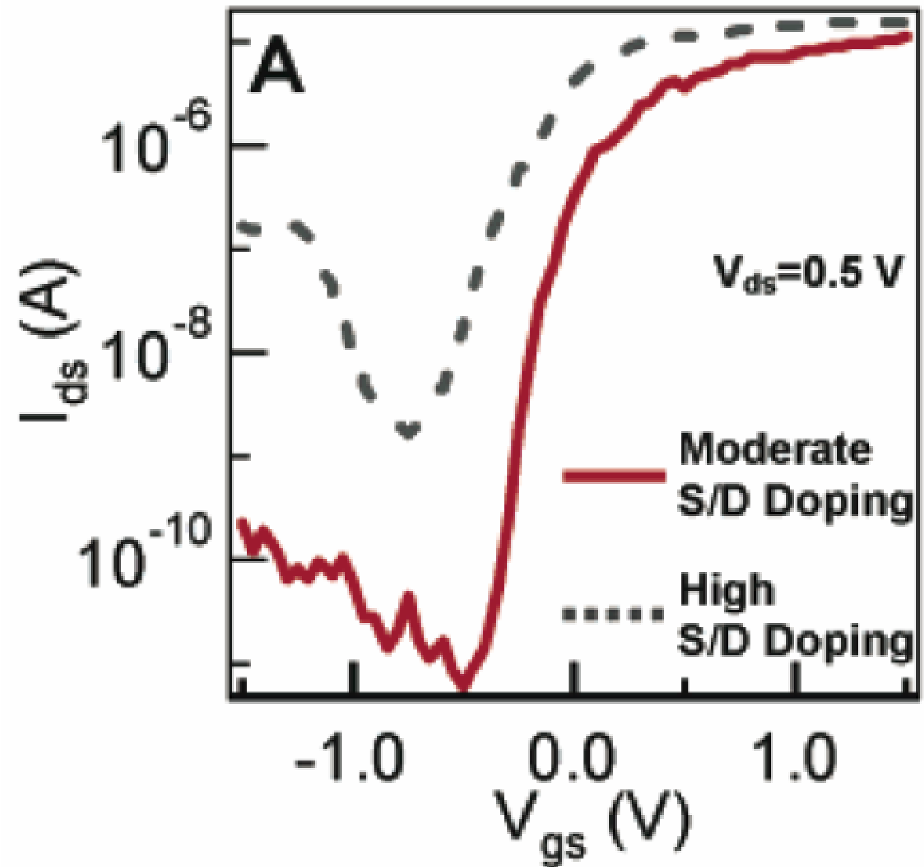
Red = after doping



Javey A, Tu R, Farmer DB, et al. NANO LETTERS 2005

Chemically doped SWNT-FET

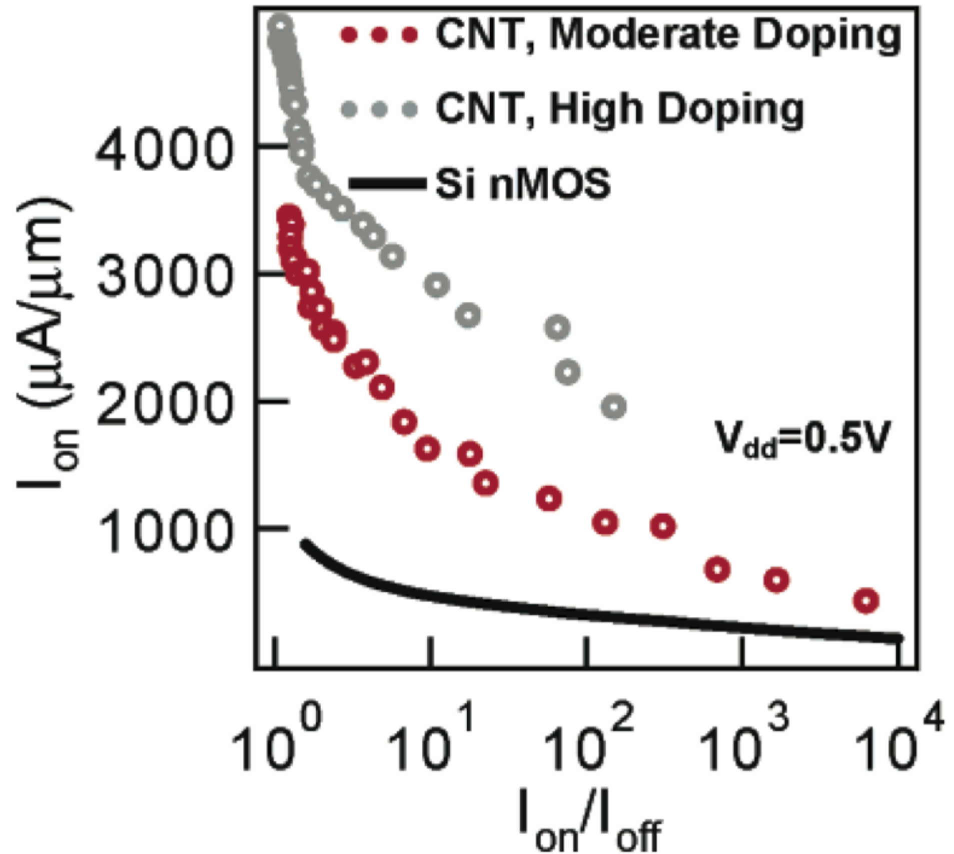
- Effects of doping
- Increased doping
  - *I_{ON} increased*
  - *Larger ambipolar p-channel conduction*
  - *I_{Min} increased*



Javey A, Tu R, Farmer DB, et al. NANO LETTERS 2005

Chemically doped SWNT-FET

- Comparison of n-type SWNT-FET with Si nMOS
- *SWNT-FET*
  - *Compare at power supply voltage of* $V_{dd}=V_{DS}=V_{gs}(on) - V_{gs}(off)=0.5V$
  - I_{ON} *per unit width*
- Si nMOS
  - *Same power supply*
  - *Same* I_{ON}/I_{OFF} *ratios as SWNT*
- For all I_{ON}/I_{OFF} ratios SWNT-FET has a higher on current



Javey A, Tu R, Farmer DB, et al. NANO LETTERS 2005

Optimization of SB-CNT FET

- Two important figures of merit: subthreshold current, I_{on}/ I_{off} ratio
- using thin high-k material as gate dielectric

  → increase coupling between gate and CNT

  → increase I_{on} , increase I_{off} (ambipolar behavior)
- Double Gate (DG) structure → suppress ambipolar

n-type device: 1st gate controls electron injection at source

2nd gate reduces hole injection at drain

Single Gate Structure

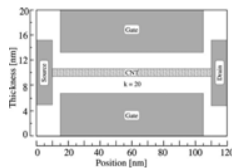
Ambipolar Behavior

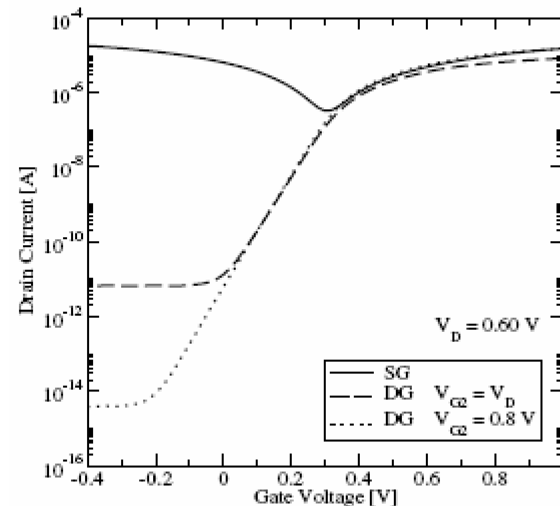
Positive $V_d > V_g$

→ suppresses SB at drain contact

→ increases hole injection

→ increases current in off regime (no saturation)



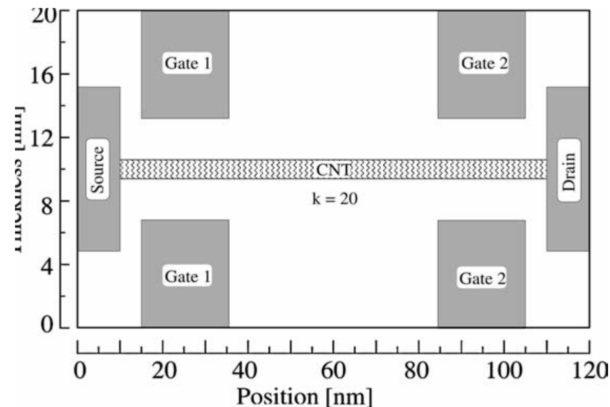


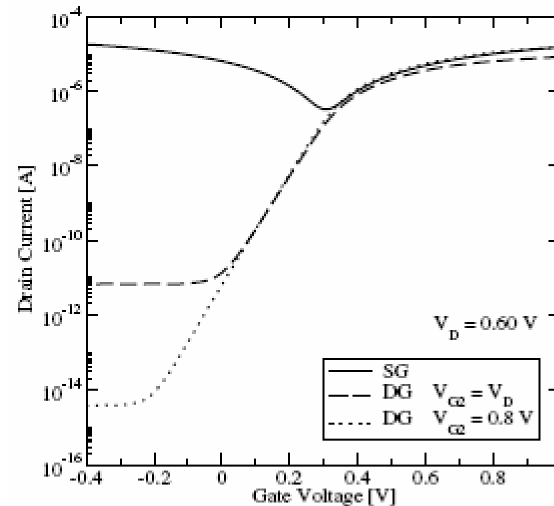
(Pourfath, 2005)

Double Gate Structure

first gate controls carrier injection at source (I_{on})

second gate controls carrier injection at drain (I_{off})

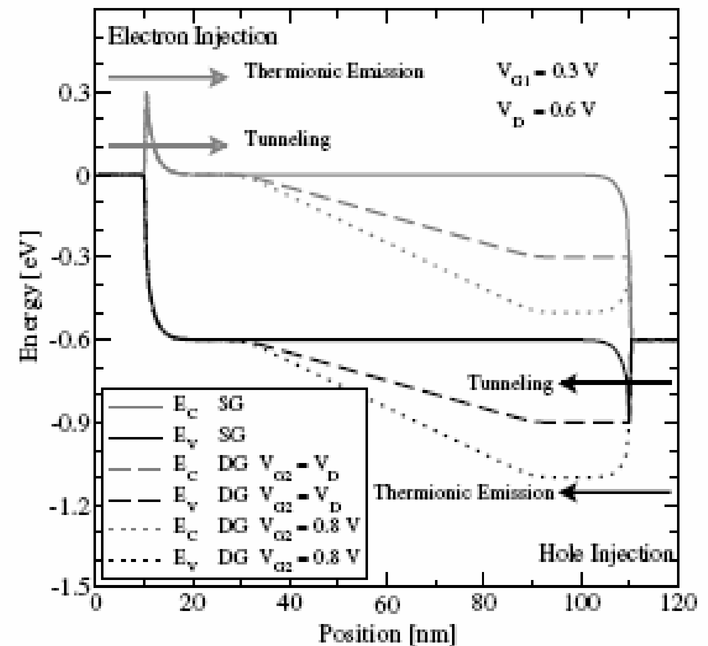




(Pourfath, 2005)

Double Gate Structure

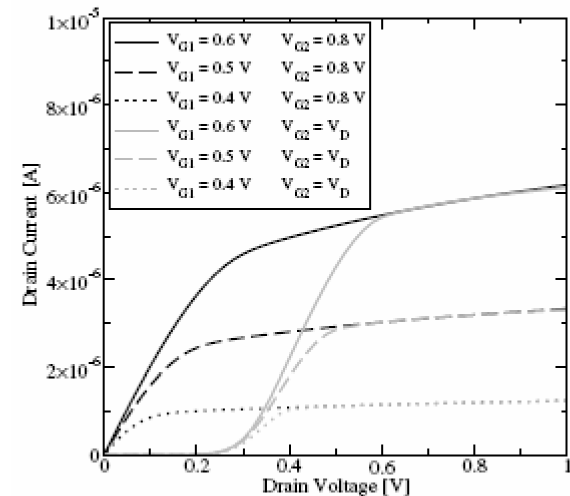
- $V_{g2}=V_d$ → flat band edge near drain (D)
  → suppressed tunneling effect of holes near D
  → only some thermionic emission current
- $V_{g2}>V_d$ → thermionic emission of holes at D decrease exp.



(Pourfath, 2005)

Double Gate Structure

- $V_{g2} = V_d$
  I_d doesn't increase until $V_d = V_{g1}$
  injected carriers at 'S' see thick barrier near 'D' until $V_d > V_{g1}$
- $V_{g2} > V_d$
  injected carriers at 'S' see thin barrier even at low V_d while holes at 'D' see thick barrier



(Pourfath, 2005)

Double Gate Overview

- 1st gate controls carrier injection at source contact (I_{on})
- 2nd gate controls carrier injection at drain contact (I_{off})
- Minimum I_{off} is limited by thermionic emission over SB
- $V_{g2} \geq V_d$

  $V_{g2} = V_d$:

  ✓ avoids parasitic cap between 2nd gate & drain

  ✓ no separate voltage source needed

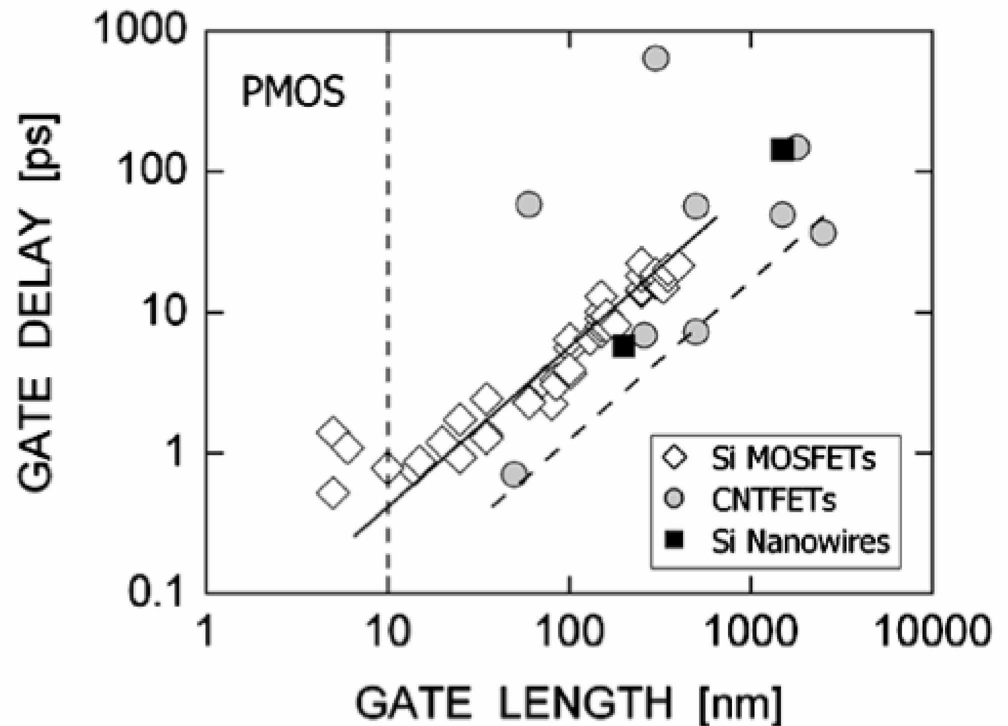
  ✓ more feasible fabrication

Benchmarking nanotechnology

- Chau R, Datta S, Doczy M, et al. IEEE Transactions On Nanotechnology, 2005
- Comparing PMOS transistors
  - *CNT-FET's*
  - *Si nanowire FET's*
  - *Nonplanar Si devices*
- Metrics
  - *Speed - CV/I vs L_g*
  - *Switching energy - CV/I * CV^2 vs L_g*
  - *Scalability - transistor subthreshold slope vs L_g*
  - *Off- state leakage - CV/I vs I_{ON}/I_{OFF}*

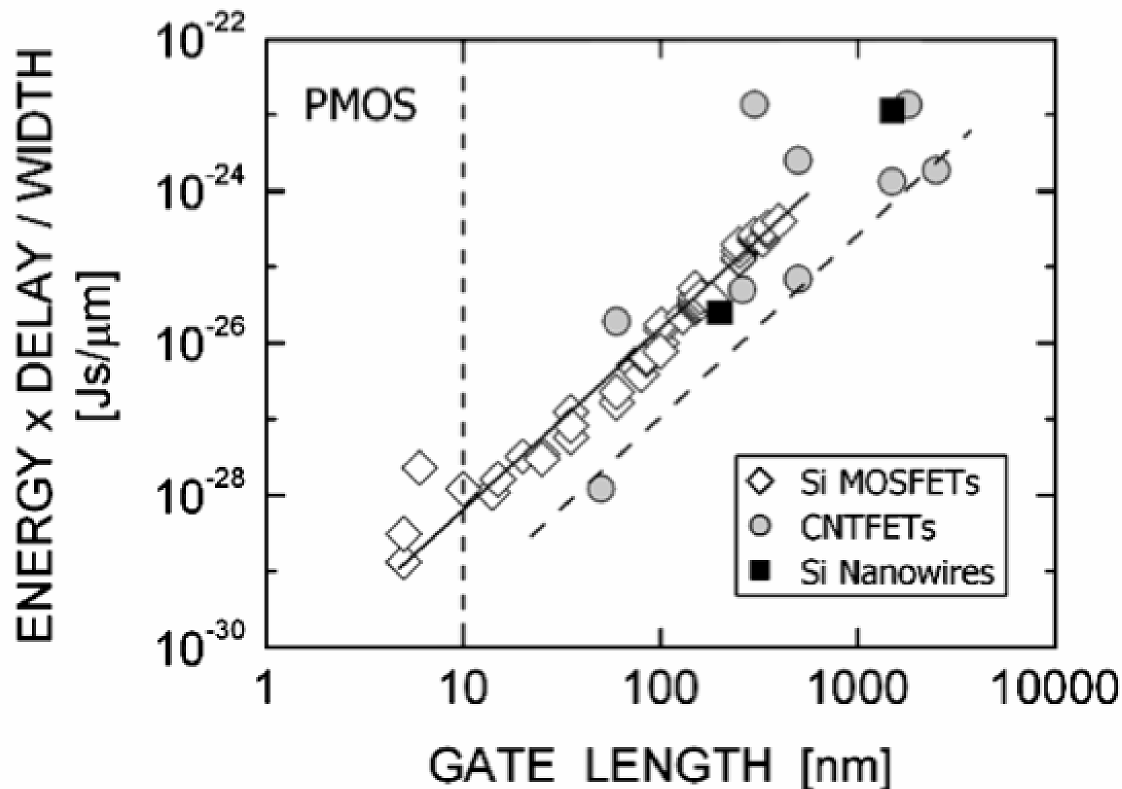
Intrinsic device speed

- CNT-FET's show CV/I improvement over Si-FET's
  - *Due to better mobility*
  - *Estimated CNT mobility at least 20 times higher than Si*
- Si NW FET's show similar data to Si FET's
- CNT and Si NW FET's have not been scaled below L_g=50nm



Switching energy

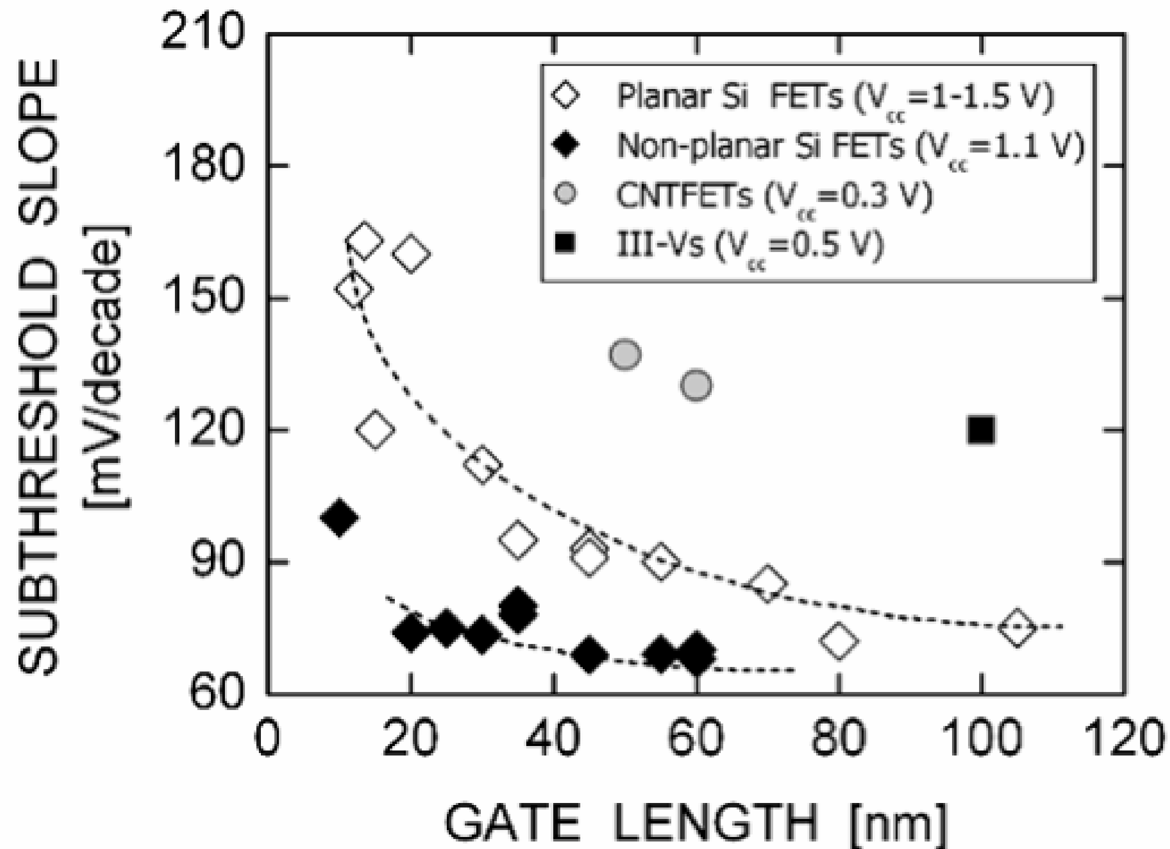
- CNT-FET's show better characteristics than Si-FET's
  - *Due to higher effective motilities*



Scalability

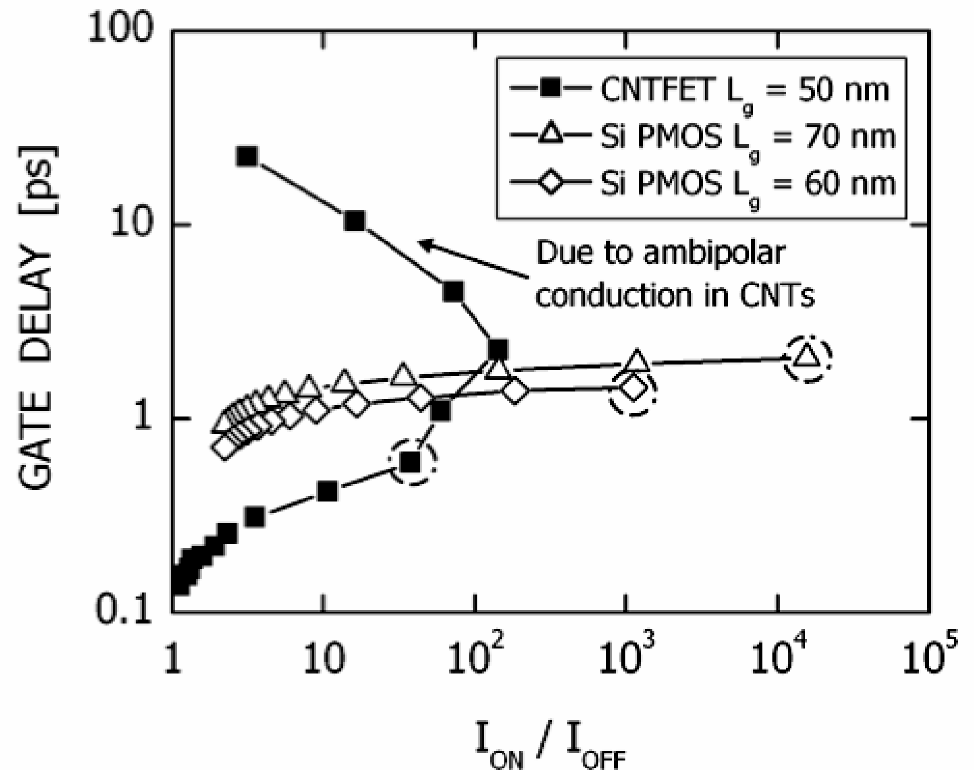
- Novel nanoelectronic devices have not been well demonstrated below L_g~50nm
- Are they scalable?
  - Subthreshold slope

Planar Si-FET	✗
Non-planar Si-FET	✓
CNT-FET	✗



Gate Delay

- Si & CNT devices
  - *CV/I Improves with reducing I_{ON}/I_{OFF}*
- *CNT show better CV/I values for a given I_{ON}/I_{OFF}*
  - *Due to higher mobility*
  - *I_{ON}/I_{OFF} limited by ambipolar behavior*



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- Unless otherwise noted all references came from
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- Javey A, Tu R, Farmer DB, et al. High Performance n-Type Carbon Nanotube Field-Effect Transistors with Chemically Doped Contacts NANO LETTERS 5 (2): 345-348 FEB 2005

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