characterized by a single exponent $\mu = 0$ governing both the frequency and temperature dependences[2,22,23]. Bosonic theory can be therefore of relevance in electron systems, but it requires the fermionic degrees of freedom to be bound in collective bosonic degrees of freedom at low energy.

In the copper oxides, it appears that the quantum criticality has to do with the restoration of the Fermi-liquid state in the overdoped regime characterized by a large Fermi surface. This implies that fermionic fluctuations play a central role in the quantum critical state, and their role has not yet been clarified theoretically. The absence of a single master curve for all values of ω/T is at variance with notions of quantum critical behaviour, and its understanding may require concepts beyond the standard model of quantum criticality. We close with the speculation that the presence of bosonic fluctuations and fermionic fluctuations in the copper oxides is pivotal in understanding the quantum critical behaviour near optimal doping of the copper oxides. □

Methods

Kubo formula

The Kubo formalism establishes the relation between optical conductivity and current–current correlation function:

$$\sigma(i\omega_n, T) = \frac{Ne^2}{m\omega_n} + \frac{1}{\omega_n}\int_0^{L_T} d\tau\ e^{i\omega_n\tau}\langle \mathbf{j}(\tau)\mathbf{j}(0)\rangle$$

The first term, corresponding to perfect conductivity, is only relevant in the superconducting state, $\mathbf{j}(\tau)$ is the current operator at (imaginary) time τ, while in the path integral formalism $L_T = \hbar/k_B T$ is the compactification radius of the imaginary time. The angle brackets mean a trace over the thermal distribution at finite temperatures. The integration is over a finite segment of imaginary time, resulting in the optical conductivity at the Matsubara frequencies $i\omega_n = 2\pi i n/L_T$ along the imaginary axis of the complex frequency plane. The conductivity at real frequency ω follows from analytical continuation.

Experimental determination of the optical conductivity

The most direct experimental technique, which provides the optical conductivity and its phase, is spectroscopic ellipsometry. Another popular approach is the measurement of the reflectivity amplitude over a wide frequency region. Kramers–Kronig relations then provide the phase of the reflectivity at each frequency, from which (with the help of Fresnel equations) the real and imaginary part of the dielectric function, $\epsilon(\omega)$, is calculated. We used reflectivity for $50\,\mathrm{cm}^{-1} < \omega/2\pi c < 6,000\,\mathrm{cm}^{-1}$, and ellipsometry for $1,500\,\mathrm{cm}^{-1} < \omega/2\pi c < 36,000\,\mathrm{cm}^{-1}$. This combination allows a very accurate determination of $\epsilon(\omega)$ in the entire frequency range of the reflectivity and ellipsometry spectra. Owing to the off-normal angle of incidence used with ellipsometry, the *ab*-plane pseudo-dielectric function had to be corrected for the *c*-axis admixture. We used previously published[24] *c*-axis optical constants of the same compound. The data files were generously supplied to us by S. Tajima. The effect of this correction on the pseudo-dielectric function turns out to be almost negligible, in accordance with Aspnes[25].

The optical conductivity, $\sigma(\omega)$, is obtained using the relation $\epsilon(\omega) = \epsilon_\infty + 4\pi i\sigma(\omega)/\omega$, where ϵ_∞ represents the screening by interband transitions. In the copper oxide materials $\epsilon_\infty = 4.5 \pm 0.5$. For $\omega/2\pi c = 5{,}000\,\mathrm{cm}^{-1}$ an uncertainty of 0.5 of ϵ_∞ propagates to an error of 2° of the phase of $\sigma(\omega)$. This accuracy improves for lower frequencies.

Frequency dependent scattering rate

For an isotropic Fermi liquid, the energy dependent scattering rate of the quasi-particles can be readily obtained from the optical data, using the relation $1/\tau(\omega) = \mathrm{Re}\{\omega_p^2/4\pi\sigma(\omega)\}$. In spite of the fact that the notion of a quasi-particle in the spirit of Landau's Fermi liquid is far from being established for the copper oxides, during the past 15 years it has become a rather common practice to represent infrared data of these materials as $1/\tau(\omega)$. The dynamical mass is defined as $m^*(\omega)/m = \mathrm{Im}\{\omega_p^2/4\pi\omega\sigma(\omega)\}$. To obtain absolute numbers for $1/\tau(\omega)$ and $m^*(\omega)/m$ from the experimental optical conductivity, a value of the plasma frequency, ω_p, must be adopted. With our value of ω_p the dynamical mass converges to 1 for $\omega \to \infty$. Sometimes the renormalized scattering rate, $\tau^*(\omega)^{-1} = \tau(\omega)^{-1}m/m^*(\omega) = \omega\sigma_1(\omega)/\sigma_2(\omega)$, is reported instead of $\tau(\omega)$. If the frequency dependence of the conductivity is a power law, $\sigma(\omega) = (-i\omega)^{\gamma-2}$, then $1/\tau^*(\omega) = -\omega\mathrm{cotan}(\pi\gamma/2)$, which is a linear function of frequency[18]. The value of the slope reveals the exponent, and corresponds to the phase of the conductivity displayed in Figs 3 and 4.

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High-performance thin-film transistors using semiconductor nanowires and nanoribbons

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Thin-film transistors (TFTs) are the fundamental building blocks for the rapidly growing field of macroelectronics[1,2]. The use of plastic substrates is also increasing in importance owing to their light weight, flexibility, shock resistance and low cost[3,4]. Current polycrystalline-Si TFT technology is difficult to implement on plastics because of the high process temperatures required[1,2]. Amorphous-Si and organic semiconductor[5,6] TFTs, which can be

processed at lower temperatures, but are limited by poor carrier mobility. As a result, applications that require even modest computation, control or communication functions on plastics cannot be addressed by existing TFT technology. Alternative semiconductor materials[7,8] that could form TFTs with performance comparable to or better than polycrystalline or single-crystal Si, and which can be processed at low temperatures over large-area plastic substrates, should not only improve the existing technologies, but also enable new applications in flexible, wearable and disposable electronics. Here we report the fabrication of TFTs using oriented Si nanowire thin films or CdS nanoribbons as semiconducting channels. We show that high-performance TFTs can be produced on various substrates, including plastics, using a low-temperature assembly process. Our approach is general to a broad range of materials including high-mobility materials (such as InAs or InP).

Individual semiconductor nanowires (NWs)[9,10] and single-walled carbon nanotubes[11–13] have been used for nanoscale field-effect transistors (FETs) with performance comparable to or exceeding that of the single-crystal materials. In particular, carrier mobility values of 300 $cm^2 V^{-1} s^{-1}$ have been demonstrated for p-type Si NWs[9], 2,000–4,000 $cm^2 V^{-1} s^{-1}$ for n-type InP NWs[10] and up to 20,000 $cm^2 V^{-1} s^{-1}$ for single-walled carbon nanotubes[13]. These nanoFETs promise to push Moore's law to the limit with unprecedented performance[10].

Here we take nanomaterial-enabled electronics in a new direction: we exploit nanomaterials not for the next generation of nanoelectronics, but for high-performance macroelectronics. In short, we assemble NWs into oriented NW thin films to yield a novel electronic substrate; this substrate is processed using standard methods to produce NW-TFTs with conducting channels formed by multiple parallel single-crystal NW paths. In such NW-TFTs, charges travel from source to drain within single crystals, thus ensuring high carrier mobility.

Figure 1a illustrates our NW-TFT fabrication process. We synthesized p-type Si-NWs with controlled diameters using a previously reported approach[14]. NWs have a core–shell structure, with a single-crystal core surrounded by an amorphous silicon oxide shell of 1–3 nm thickness (Supplementary Fig. S1). The NWs were then dispersed into solution, and assembled onto the surface of the chosen substrate using a flow-directed alignment method[15] to produce an oriented NW thin film. An optical micrograph (Fig. 1b) of the NW thin film shows that the film consists of a monolayer of NWs oriented in parallel with an average NW spacing of 500–1,000 nm. The NW spacing is controlled by varying the NW solution concentration and flow time. Other approaches (for example, a Langmuir–Blodgett film) may also be used to obtain nearly close-packed NW thin films[16,17]. Oriented-NW deposition can readily be achieved over a 4-inch wafer and potentially at larger scales (Supplementary Fig. S2). The NW thin film was then processed using standard lithography followed by metallization to define source and drain electrodes and yield TFTs (Fig. 1c, d). For initial study, the TFTs had a simple back-gated device configuration on a silicon substrate (Fig. 1c inset), where underlying silicon was used as the back gate, 100-nm-thick silicon nitride (SiN_x) as the gate dielectric, and Ti/Au film as the source and drain electrodes.

Drain current (I_{DS}) versus drain–source voltage (V_{DS}) relations (Fig. 2a) at various gate voltages (V_{GS}) for a NW-TFT show typical accumulation mode p-channel transistor behaviour[18], as I_{DS} increases linearly with V_{DS} at low V_{DS}, and saturates at higher V_{DS}. Upon application of negative V_{GS}, I_{DS} increases as the majority carrier (hole) density increases in the channel. Applying a positive V_{GS} depletes holes in the channel and turns the device off. The plot of $-I_{DS}$ versus V_{GS} (Fig. 2b) at a constant $V_{DS} = -1$ V shows little current when the V_{GS} is more positive than a threshold voltage (V_{th}), and I_{DS} increases nearly linearly when the V_{GS} increases in the negative direction. Extrapolation of the linear region results in a V_{th} of 0.45 V.

For macroelectronic applications, a number of key transistor parameters, including transconductance, mobility, on/off ratio, threshold voltage, and subthreshold swing, dictate TFT performance[18]. High transconductance is a critical measure of transistor

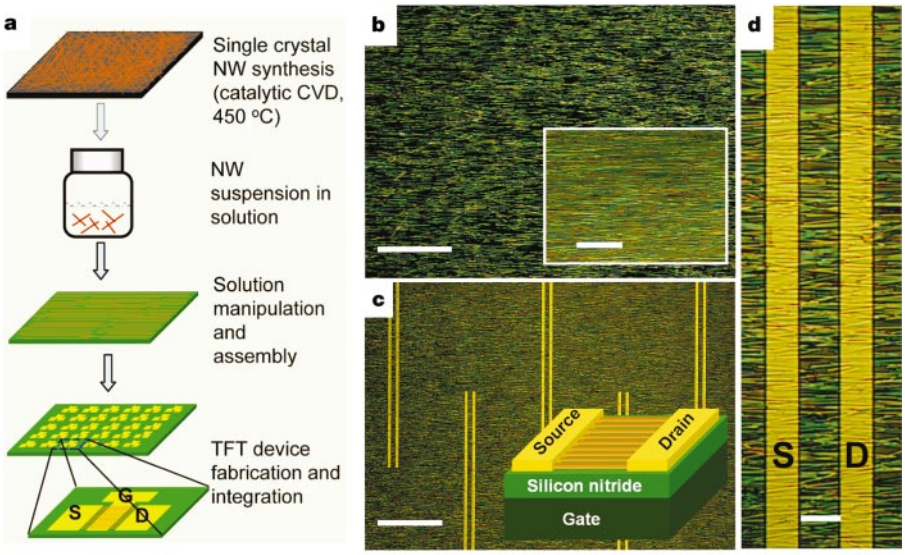

Figure 1 Nanowire TFT fabrication. **a**, Diagrams illustrating the NW-TFT fabrication process. In our approach, high-quality single-crystal NW materials are synthesized at high temperature using a catalytic chemical vapour deposition processes, and are then harvested and dispersed in a solution and aligned on the desired substrate to form a densely-packed oriented NW thin film that is further processed via standard methods to form TFTs with the conducting channel parallel to the wire axis. **b**, Optical micrograph of flow aligned NW thin film. Scale bar, 80 μm. Inset, a picture at higher magnification. Scale bar, 20 μm. The micrographs show that the NW thin film is nearly a monolayer of NWs, but occasionally a few NWs cross over each other. The average space between parallel NW arrays is estimated to be ~540 nm. **c**, Optical micrograph of NW-TFTs fabricated on NW thin films. The whole substrate is covered with a NW thin film, and each pair of metal (Ti/Au) electrodes (yellow) corresponds to source–drain electrodes for a NW-TFT. Scale bar, 100 μm. Inset, a schematic view of the NW-TFT configuration. **d**, Optical micrograph of a NW-TFT, where parallel arrays of NW are clearly seen to bridge the full distance from the source to the drain electrodes. Scale bar, 5 μm.

performance, and determines voltage gains of transistor-based devices including amplifiers and logic circuits. The slope in the linear region of $-I_{DS}$ versus V_{GS} gives a transconductance $g_m = dI_{DS}/dV_{GS} \approx 11\,\mu S$ at $V_{DS} = -1\,V$. Assuming the effective channel width equals the NW diameter (d) multiplied by the number (N) of NWs, $W_{eff} = Nd = 1.8\,\mu m$, we obtain a normalized transconductance of $\sim 6\,\mu S\,\mu m^{-1}$; this is significantly better than that of organic[6], amorphous (a)-Si ($<0.01\,\mu S\,\mu m^{-1}$)[1], and p-channel polycrystalline (poly)-Si TFTs (~ 0.2–$0.8\,\mu S\,\mu m^{-1}$)[19], and is comparable to that of single-crystal p-channel silicon-on-insulator (SOI) MOSFETs (~ 5–$12\,\mu S\,\mu m^{-1}$)[20]. A normalized transconductance of $\sim 0.09\,\mu S\,\mu m^{-1}$ is calculated if the physical channel width of the device is used, which is still significantly better than a-Si TFTs, and nearly comparable to poly-Si TFTs. The value can be further increased with improved assembly approach[16,17]. For a fair comparison, all the transconductance values have been scaled to devices with the same dimension according to a scaling law[18]. We note that the transconductance can further be improved using thinner dielectrics of higher dielectric constant[12].

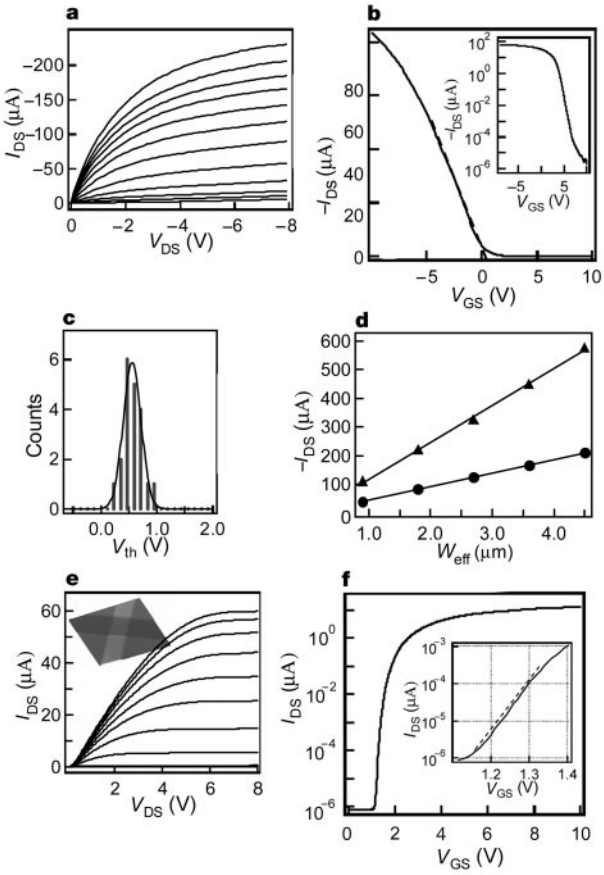

Figure 2 p-channel Si NW-TFT and n-channel CdS nanoribbon TFT. **a**, Drain current (I_{DS}) versus drain–source voltage (V_{DS}) (I_{DS}–V_{DS}) at increasing gate voltages (V_{GS}) in steps of 1 V starting from the top at $V_{GS} = -10$V. The TFT consists of 91 20-nm-diameter NWs in parallel with a 5-μm channel length. **b**, $-I_{DS}$ versus V_{GS} at $V_{DS} = -1$ V. Linear extrapolation results in a threshold voltage (V_{th}) of ~0.45 V. Inset, $-I_{DS}$ versus V_{GS} at $V_{DS} = -1$ V on an exponential scale, highlighting the on-off ratio of nearly 10^8, and the subthreshold swing of about 600 mV per decade. The linear plot data (main panel) were collected at a V_{GS} sweep rate of 500 mV s^{-1}, and the exponential plot data (inset) were collected at a V_{GS} sweep rate of 15 mV s^{-1} to minimize capacitive charging currents at the higher gate voltages. The apparent threshold voltage in the inset is shifted to 3.5 V due to a hysteresis effect (Supplementary Fig. S5). **c**, Histogram of threshold voltage (V_{th}) distribution from 20 NW-TFT devices shows high device-to-device reproducibility and a tight distribution. Gaussian fitting (curve) shows a standard deviation of only 0.22 V. The threshold voltage value was derived from linear extrapolation of the I_{DS}–V_{GS} relation at $V_{DS} = -1$ V. The I_{DS}–V_{GS} relation for all the devices was taken under exactly the same conditions, with a V_{GS} sweep rate of 500 mV s^{-1}. **d**, Linear-scale relation for the drain current when the device is turned on ($V_{GS} = -10$ V). The circles and triangles represent the on-state current as a function of effective channel width measured at $V_{DS} = -1$ V and -8 V, respectively. The effective channel width corresponds to the product of the average diameters of the NWs and the number of the NWs in the channel. **e**, I_{DS}–V_{DS} at variable gate voltages (V_{GS}) starting from top at $V_{GS} = +10$ V decreasing in steps of 1 V. The TFT consists of a nanoribbon of 0.7-μm width and 4.3-μm channel length. Inset, a 3D atomic force microscope topographic image of a nanoribbon TFT. **f**, I_{DS}–V_{GS} relation at $V_{DS} = 1$ V on an exponential scale shows an on-off ratio greater than 10^7. Inset, a zoomed-in plot in the subthreshold region that highlights a subthreshold swing as small as 70 mV per decade.

To estimate the carrier mobility, the device was modelled using standard MOSFET equations. In the low-bias linear region of the I_{DS}–V_{DS} curves, the hole mobility μ_h can be deduced from $G_{DS} = I_{DS}/V_{DS} = \mu_h C_G (V_{GS} - V_{th} - V_{DS}/2)/L^2$, where C_G is the gate capacitance and L is the channel length. Using a calculated C_G (see Methods), we deduced $\mu_h \approx 119\,cm^2\,V^{-1}\,s^{-1}$, which is significantly larger than those of organic, a-Si TFTs ($<1\,cm^2\,V^{-1}\,s^{-1}$) and comparable to the best reported values for p-type poly-Si TFTs ($\sim 120\,cm^2\,V^{-1}\,s^{-1}$)[2] and that of p-type SOI MOSFETs ($\sim 180\,cm^2\,V^{-1}\,s^{-1}$)[20]. Additionally, it is possible to further improve the carrier mobility; for example, by decreasing the doping level and/or minimizing the trapping states on the NW surface[1,9].

The curve of $-I_{DS}$ versus V_{GS} on an exponential scale (Fig. 2b inset) shows that I_{DS} decreases exponentially below V_{th} and that the transistor has an on-off current ratio of nearly 10^8. This is, to our knowledge, the largest on-off ratio reported for transistors assembled from chemically synthesized nanomaterials, and is comparable to that of single-crystal silicon devices[18]. The subthreshold swing $S = -dV_{GS}/d\ln|I_{DS}|$ is ~600 mV per decade for this device. In conventional MOSFETs, subthreshold swing depends on the ratio of the gate capacitance to other capacitances such as interface trap state capacitance, and has a theoretical limit of ~60 mV per decade at room temperature[18]. A small subthreshold swing is usually desired for low-threshold-voltage, low-power operation. The subthreshold swing of ~600 mV per decade in our device is significantly better than those of organic[6] or a-Si TFTs[1] that typically range from one to many volts per decade, but is substantially larger than the best values in poly-Si TFTs (~200 mV per decade)[1] and single-crystal silicon devices (~70 mV per decade)[18]. We believe the relatively large subthreshold swing in our device is mainly due to the existence of surface trapping states[1] and a geometric effect (Supplementary Fig. S3b), which can be improved dramatically by passivating the surface (for example, hydrogenation[1,21] or using a core–shell structure[22]) and/or using a top- or surrounding-gated structure with high-k dielectrics[12]. Importantly, a subthreshold swing as small as ~70 mV per decade has been demonstrated using a surrounding conformal electrolyte gate[13] (X.D., C.N. and V.S., unpublished results).

To study the reproducibility and practical viability of this technology, we have performed tests on 20 NW-TFTs. The threshold voltage distribution (Fig. 2c) and gaussian fitting show a standard deviation of only 0.22 V. Considering that the device configuration and fabrication process have not been optimized, such a tight distribution is very encouraging. We note that major device parameters are independent of the number of NWs in the conducting channel except the drain–source on-current, which scales linearly with the effective channel width (Fig. 2d). Reproducible and predictable assembly of NW-TFTs with designed device parameters will be critical for actual circuit design in future applications.

Because the NW synthesis is independent of the device substrate, our process represents a general approach for exploiting a broad range of materials (including III-V and II-VI group semiconduc-

tors[23]) as the TFT channel materials, and thus opens new opportunities not possible with current poly-Si technologies. As an example, we now show that high-performance TFTs can also be readily assembled from CdS nanoribbons. CdS is an excellent material for optical as well as electronic applications owing to its intrinsically low surface trapping states[24], and is one of the earliest materials used for TFTs[25]. Single-crystal CdS nanoribbons (Supplementary Fig. S4) were synthesized using a vacuum-vapour-transport method. These nanoribbons are particularly interesting candidates for assembling TFTs because their unique physical morphology closely resembles that of conventional single-crystal thin film. CdS nanoribbon TFTs with a single-crystal conducting channel (Fig. 2e inset) were fabricated with an approach similar to that described above.

Electrical transport measurements show typical n-channel transistor characteristics, consistent with previous studies on CdS bulk materials and NWs[24]. The I_{DS}–V_{DS} relation at different gate voltages (Fig. 2e) shows a linear region at low V_{DS} and saturates at a higher V_{DS}. The I_{DS}–V_{GS} relation at a V_{DS} of 1 V shows nearly linear behaviour above a threshold V_{GS} of 2.0 V. The slope in the linear region gives a transconductance of ~2.4 μS at $V_{DS} = 1$ V. With the calculated capacitance (see Methods), we deduce electron mobility of ~283 $cm^2 V^{-1} s^{-1}$ using $I_{DS}/V_{DS} = \mu_e C_G (V_{GS} - V_{th} - V_{DS}/2)/L^2$. Importantly, this mobility value matches closely with that of single-crystal CdS material (~300–350 $cm^2 V^{-1} s^{-1}$)[26]. Furthermore, the exponential plot of I_{DS}–V_{GS} gives an on-off ratio $>10^7$ and a subthreshold swing as small as 70 mV per decade (Fig. 2f and inset), approaching the theoretical limit of 60 mV per decade. The high carrier mobility and small subthreshold swing can be largely attributed to excellent crystalline quality (Supplementary Fig. S4), low-surface states in CdS nanoribbons and the absence of geometrical effects like that in Si NW-TFTs.

A unique feature of the NW-TFT concept is that the entire NW-TFT fabrication process was performed essentially at room temperature, except for the NW synthesis step which is separate from the device fabrication. Therefore, the assembly of high-performance NW-TFTs could be readily applied to low-cost glass and plastic substrates. To demonstrate NW-TFTs on plastics, we have adopted a different device configuration (Fig. 3a). In the plastic device, a locally patterned Cr/Au electrode was used as the gate and electron-beam (e-beam)-evaporated aluminium oxide (AlO_x) was used as the gate dielectric (Fig. 3b).

I_{DS}–V_{DS} curves of a NW-TFT on plastic (Fig. 3c) show a similar behaviour to that of devices on SiN_x/Si substrate. The I_{DS}–V_{GS} relation (Fig. 3d) shows a threshold voltage of ~3.0 V, an on-off ratio $>10^5$, and a subthreshold swing of 500–800 mV per decade, which to our knowledge are among the best characteristics reported for TFTs on plastic. The relatively smaller on-off ratio is due to (1) lower on-current resulting from un-optimized local-gate device configuration, and (2) higher off-current limited by gate leakage current caused by the low quality of e-beam-evaporated AlO_x dielectrics; the on-off ratio can be significantly increased with improved device configuration and advanced core–shell NW structure (Supplementary Fig. S3). A major motivation driving the plastic electronic research is mechanical flexibility. Importantly, slight flexing (radius of curvature ~55 mm) of the plastic with a NW-TFT device does not significantly change the device behaviour (black versus red curve in Fig. 3d and inset). The linear region in the I_{DS}–V_{GS} relation gives a transconductance of 0.45 μS at $V_{DS} = -1$ V (Fig. 3d), but it is hard to extract the hole mobility in the device owing to the difficulties in estimating the gate capacitance of the local-gated device configuration. From electrical measurement of a NW-TFT on plastic with an electrolyte gate[13] (X.D., C.N. and V.S., unpublished results), we deduced the hole mobility $\mu_h \approx 123\ cm^2 V^{-1} s^{-1}$, which is in good agreement with the mobility obtained for similar devices on SiN_x/Si substrate with similar NWs.

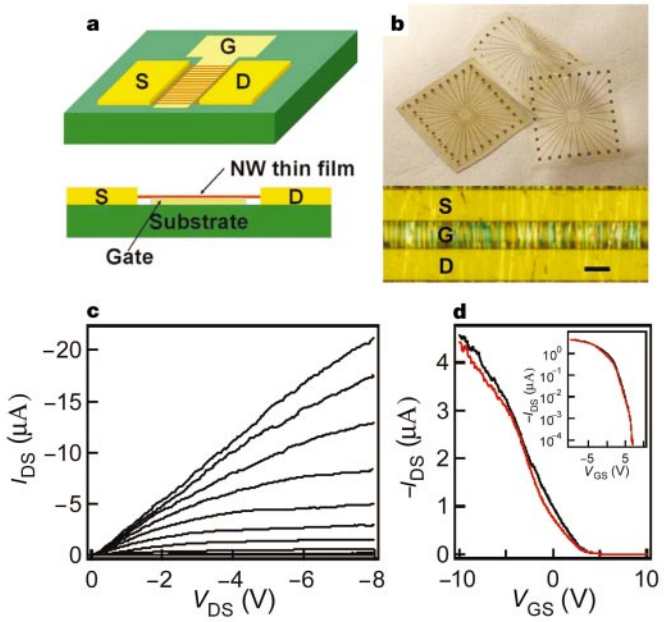

Figure 3 NW-TFTs on plastic. **a**, Diagrams show the device configuration of a locally back-gated NW-TFT on plastic: top, top view; bottom, cross-sectional view. To fabricate the device, a layer of 1–2 μm-thick SU-8 (MicroChem Corp.) photo-resist was first spin cast and cured on a polyetheretherketone (PEEK) sheet (125 μm thick, Goodfellow Inc.) to ensure a microscopically smooth surface. Cr/Au (10/30 nm) strips were then defined as the gate arrays, and a 30-nm layer of aluminium oxide was deposited as gate dielectric using e-beam evaporation. Lastly, the aligned NW thin film was deposited onto the surface, and Ti/Au (60/80 nm) source–drain electrodes were defined to form the TFTs. **b**, Top, a picture of plastic (PEEK) devices with NW-TFTs. The plastic devices show high mechanical flexibility. Bottom, optical micrograph of a locally gated NW-TFT. Scale bar, 5 μm. **c**, I_{DS}–V_{DS} relation at variable V_{GS} starting from the top at $V_{GS} = -8$ V and increasing in steps of 1 V. The TFT consists of 17 NWs of 40-nm diameter in parallel with a 6-μm channel length and 3-μm gate length. **d**, $-I_{DS}$–V_{GS} relation at $V_{DS} = -1$ V. Inset, $-I_{DS}$–V_{GS} relation at $V_{DS} = -1$ V on an exponential scale, which highlights the on-off ratio of more than 10^5 and a subthreshold swing of 500–800 mV per decade. The black and red curves show the transfer characteristics of the same device before and after slight flexing of the plastic substrate (radius of curvature ~55 mm), demonstrating the mechanical flexibility of NW TFTs on plastics.

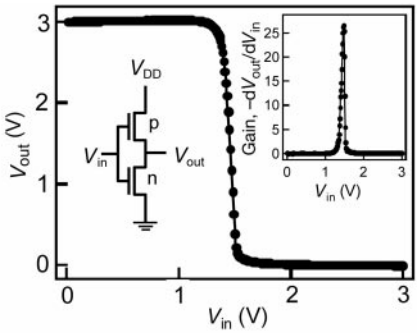

Figure 4 Complementary inverter constructed from NW and nanoribbon TFTs. The output–input (V_{out} versus V_{in}) curve shows a sharp inversion of the output signal. Left inset, the circuit of the complementary inverter formed by connecting a p-channel Si NW-TFT (consisting of 15 NWs in parallel) and an n-channel CdS nanoribbon TFT in series. Right inset, the gain (absolute value of the derivative of V_{out}–V_{in} relation) of the inverter, highlighting a large voltage gain of 27.

The dissociation of semiconductor material growth and device fabrication in our approach allows us to flexibly combine different high-performance semiconductor materials together on a single substrate to achieve (much) improved function and performance, in a way not possible with other technologies. For example, a complementary inverter (a logic NOT gate) was constructed by connecting a p-channel Si NW TFT and an n-channel CdS nanoribbon TFT in series (Fig. 4 left inset)[27]. The output–input (V_{out}–V_{in}) voltage response (Fig. 4) of the inverter shows constant high voltage output with low input. When the input is increased to about 1.5 V, the output quickly turns to 0 V and maintains a low state at higher input voltages. Most significantly, the complementary inverter exhibits a high voltage gain. Differentiation of the measured V_{out}–V_{in} relation reveals a voltage gain as large as 27 (Fig. 4 right inset). Such a large gain demonstrates high performance of our devices, and is critical for interconnection of arrays of logic circuits for macroelectronic applications without the need for signal restoration at each stage.

We have demonstrated an approach to macroelectronics based on solution-assembled NW or nanoribbon thin films. This approach offers a potential technology platform for high-performance TFTs from high-mobility materials (for example, InP or InAs)[10,23], and for novel large-area optoelectronics[24,28] from II-VI and III-V group optically active NW[23] materials on flexible substrates. Significantly, low-cost, low-temperature processes using microcontact[29] or ink-jet printing technology[30] may be employed to produce high-performance flexible macroelectronics. We believe that the present approach will affect existing applications and enable new opportunities in flexible, wearable and disposable electronics. □

Methods

Material syntheses

The p-type Si NWs with controlled diameter of 20 or 40 nm were synthesized by thermal deposition of SiH_4 and B_2H_6 using commercially available mono-dispersed gold colloid particles (British Biocell International Ltd) as the catalysts[14]. The growth was typically carried out in a computer-controlled pilot production scale reactor in a 8-inch tube furnace at a temperature between 420 and 480 °C, a total pressure of 30 torr, and a silane partial pressure of approximately 2 torr, for a period of 40 min. The SiH_4 to B_2H_6 ratio can be varied to control the doping level, and a ratio of ~6,400:1 was used in synthesizing NWs for this study. The doping concentration of the NW was estimated to be $\sim 4 \times 10^{17}$ cm^{-3} from electrical characterizations. This relatively high doping concentration was used to ensure a good contact between NWs and source and drain electrodes without a high-temperature annealing process.

CdS nanoribbons were synthesized using a vacuum vapour transport approach. Specifically, a small amount of CdS powder (~100 mg) was transferred into one end of a vacuum tube and sealed. The vacuum tube was heated such that the end with CdS powder was maintained at 900 °C, while the other end was kept at a temperature ~50 °C lower. Within two hours, most of the CdS was transported to the cooler end and deposited on the tube wall. The resulting materials are predominantly nanoribbons having thicknesses of 30–150 nm, widths of 0.5–5 μm, and lengths of 10–200 μm (Supplementary Fig. S4).

Device fabrication and characterization

The as-made NWs or nanoribbons were dispersed into ethanol solution by ultrasonication, and assembled on to chosen substrate for device fabrication using a fluidic flow alignment aproach[15]. For a global-back-gated device on SiN_x/Si substrate, NWs or nanoribbons were first aligned to the substrate to form a thin film, which is further subjected to photolithography or e-beam lithography to define the source and drain electrode. Source and drain electrodes were metallized with Ti/Au (60/80 nm) film deposited using an e-beam evaporator, without further thermal annealing. Prior to metallization, the native oxide was etched using a dilute (6%) buffered hydrofluoric acid solution. For local-gated devices on plastics, a layer of 1–2-μm-thick SU-8 (MicroChem Corp.) photo-resist was first spin cast and cured on a PEEK sheet (125 μm thick, Goodfellow Inc.) to ensure a microscopically smooth surface. Cr/Au (10/30 nm) strips were then defined as the gate arrays, and a 30-nm layer of aluminium oxide was deposited as gate dielectric using e-beam evaporation. Lastly, the aligned NW thin film was deposited onto the surface, and Ti/Au (60/80 nm) source–drain electrodes were defined to form the TFTs.

All electrical characterizations were carried out in air in a dark box at room temperature. For comparison of device performance with other technology (for example, a-Si, poly-Si and SOI structure), all devices were scaled to have the same dimension where applicable. For a global-back-gated Si NW-TFT (Fig. 2 a–d), the gate capacitance includes the capacitance of the SiN_x dielectric on the substrate and that of the silicon oxide shell. It is, however, nontrivial to calculate these capacitances owing to the complex geometry. The gate capacitance was computed using a 3D finite element package (MetaMesh and HiPhi from Field Precision: http://www.fieldp.com). Results are converged within 1%. Numerical simulation yields a total capacitance of ~28 fF for the device shown Fig. 2a and b. For CdS nanoribbon TFTs (Fig. 2e, f), assuming a parallel plate model, we calculated the gate capacitance to be 2.0 fF using $C_G = \epsilon\epsilon_0 L \cdot W/h$, where ϵ is dielectric constant, L and W are channel length and width, and h is the dielectric thickness.

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