High-Performance Nanowire Electronics and Photonics and Nanoscale Patterning on Flexible Plastic Substrates

MICHAEL C. MCALPINE, ROBIN S. FRIEDMAN, AND CHARLES M. LIEBER

Contributed Paper

The introduction of an ambient-temperature route for integrating high-mobility semiconductors on flexible substrates could enable the development of novel electronic and photonic devices with the potential to impact a broad spectrum of applications. Here we review our recent studies demonstrating that high-quality single-crystal nanowires (NWs) can be assembled onto flexible plastic substrates under ambient conditions to create FETs and light-emitting diodes. We also show that polymer substrates can be patterned through the use of a room temperature nanoimprint lithography technique for the general fabrication of hundred-nanometer scale features, which can be hierarchically patterned to the millimeter scale and integrated with semiconductor NWs to make high-performance FETs. The key to our approach is the separation of the high-temperature synthesis of single-crystal NWs from room temperature solution-based assembly, thus enabling fabrication of single-crystal devices on virtually any substrate. Silicon NW FETs on plastic substrates display mobilities of 200 cm^2-V^{-1}-s^{-1}, rivaling those of single-crystal silicon and exceeding those of state-of-the-art amorphous silicon and organic transistors currently used for flexible electronics. Furthermore, the generality of this bottom-up assembly approach suggests the integration of diverse nanoscale building blocks on a variety of substrates, potentially enabling far-reaching advances in lightweight display, mobile computing, and information storage applications.

Keywords*—Flexible electronics, light-emitting diodes, nanoimprint lithography (NIL), nanoscale patterning, nanowire (NW) transistors, plastic substrates, silicon nanowires (NWs).*

I. INTRODUCTION

Modern microelectronics has been dominated by innovations in "top-down" manufacturing processes, in which wafers of single-crystalline silicon—grown under conditions of high temperature and pressure—are patterned via photolithography into arrays of small, dense integrated transistors [1]. These chips have formed the foundation of an impressive array of computing devices, most notably the personal computer. Equally impressive have been relatively unnoticed innovations in the field of "macroelectronics," defined as electronic systems fabricated over large areas and/or in abundant supply, such as flat-panel displays, smart cards, and wearable displays [2]–[8]. The latter approach has required the integration of inexpensive semiconducting materials onto cheap, lightweight substrates such as glass or conformable plastics, which has motivated research on the synthesis and deposition of new classes of semiconductors on such substrates, as well as methods of finely patterning such substrates. Yet despite over a decade of research, the requirement of high temperature for achieving single-crystal semiconductors has limited the quality of electronics on alternative substrates, as plastics melt well below those temperatures.

For example, amorphous silicon, the active component of transistors in flat-panel displays, can be deposited on glass at relatively low temperatures using vacuum deposition techniques. Yet the low carrier mobility [4], [5], [9] of amorphous silicon restricts its use to pixel-switching elements in these displays, thus requiring peripheral, higher performance electronics made of polycrystalline silicon to drive the switch elements. Polycrystalline silicon has demonstrated carrier mobilities approaching that of single-crystal silicon [10], opening up the possibility of combining pixel elements, display drivers, and more complex electronics on the display substrate. However, the complex processing required to achieve high-quality polycrystalline silicon represents a limitation in the implementation of polysilicon transistors on large-scale glass and plastic substrates [6].

There have also been substantial effort invested in using organic materials as active semiconductor elements [5], [8], as organic semiconductors have the potential for room

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The authors are with the Department of Chemistry and Chemical Biology, and the Division of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138, USA (e-mail: mmcalpine@cml.harvard.edu; robinf@cml.harvard.edu; cml@cml.harvard.edu).

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temperature solution-based processing that can be easily coupled to flexible plastic substrates [11], [12]. Yet, the inherently low carrier mobilities exhibited by organic semiconductors restrict the potential function of these materials and corresponding applications [5], [13]. Overall, these results indicate a dichotomy in the capabilities of current materials—either low performance and broad substrate applicability (organics and amorphous silicon) or high performance and restricted substrate use (polycrystalline silicon)—which, if overcome, could open up exciting opportunities such as the integration of high-performance multifunctional electronics and displays on flexible plastics.

Here we review our recent progress in addressing this general problem, by utilizing a solution-based "bottom-up" assembly of semiconductor nanowires (NWs), akin to the processing for organic semiconductors. NWs are composed of traditional semiconducting materials, but have the morphology of anisotropic wires several nanometers in diameter and tens of micrometers in length [14]. The functional properties of NW building blocks are defined via a high-temperature growth phase and are independent of the ambient solution-based deposition stage. NWs, which exhibit carrier mobilities comparable to those of bulk single-crystal materials [15], [16], have already been demonstrated to be effective materials for the bottom-up assembly of integrated electronic and photonic devices, including nanometer-scale FETs and logic circuits [17], light-emitting diodes [18], and ultrasensitive biological sensors [19]. As our work shows, such high-performance devices can be readily extended to plastic substrates [20].

We also review our approach for patterning nanometer through millimeter scale features on flexible plastic substrates through the use of room temperature nanoimprint lithography (NIL) [21]. The most successful patterning technique used over the past several decades has been photolithography, although developments in this technique that have pushed feature resolution to the 100-nm regime have come at the expense of increasingly complex and costly fabrication equipment [22]. NIL is an interesting alternative approach for nanoscale patterning that is cost-effective, parallel, and scalable [23], and has been shown to be capable of producing sub-100-nm structures on 6-in wafers [24], as well as three-dimensional patterns on conventional inorganic substrates such as silicon [25]. Polymers used for NIL are typically heated above 200 °C, which is above the glass transition temperature, to enable conformable flow during the imprinting step [26]. This heating process represents a limitation for the application of NIL to flexible plastic substrates, since plastics deform at elevated temperatures. Our approach demonstrates that imprint lithography is capable of uniformly patterning flexible, polymeric surfaces in a single room temperature step, making it possible to achieve hundred-nanometer-resolution metal electrodes hierarchically patterned over a large area on plastic substrates. Furthermore, we show that the electrodes patterned by NIL can be naturally combined with NWs to generate high-performance nanoscale transistors, which display single-crystal semiconductor device properties on these flexible substrates.

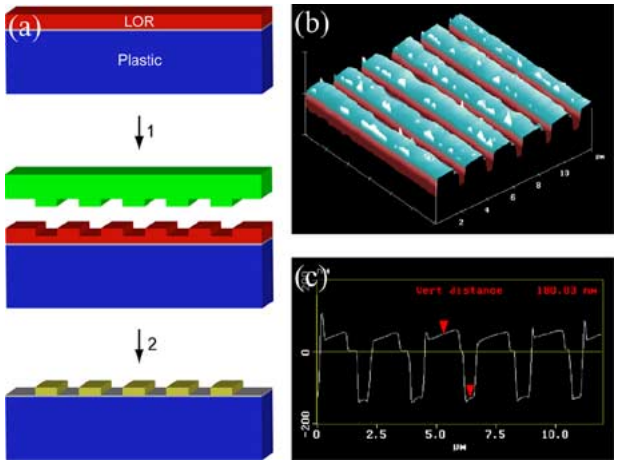

Fig. 1. Schematic of the NIL process on plastic. (a) Plastic substrates (blue) coated with SiO_2 (gray) and LOR (red) were imprinted (1) using a Si/SiO_2 stamp (green). The NIL pattern was transferred to the substrate in successive RIE, metal deposition, and liftoff steps (2). (b) and (c) AFM topographical and line-scan images of the imprinted features, respectively.

II. NIL on Plastics

In NIL [23], [27], a pattern is generated via compression molding of a deformable polymer by a hard inorganic stamp containing nanometer scale features. These features are typically produced using serial electron-beam lithography, but the stamp can be reused many times, making the overall process highly parallel. This relief pattern is subsequently transferred to the underlying substrate by anisotropic reactive ion etching (RIE), followed by material deposition and liftoff of the remaining polymer.

Achieving room-temperature NIL on plastic substrates requires the careful selection of materials used in the process. First, plastic substrates consisted of 100-μm-thick poly(ethylene terephthalate) (Mylar, CP Films, Martinsville, VA) coated with 500-nm SU-8 (MicroChem Corp., Newton, MA) and 50 nm SiO_2 for enhanced planarization of the substrate surface. Second and central to our work is the careful selection of a suitable resist, which must be able to be: 1) reproducibly imprinted at room temperature; 2) removed cleanly from the inorganic stamp; and 3) etched at controlled rates by RIE. Specifically, we have found that liftoff resist (LOR-3A, MicroChem Corp.), as well as epoxy-type resists such as SU-8, function as excellent materials for this purpose. Fig. 1(a) highlights the process. Stamp features consisted of 200 nm wide SiO_2 ridges fabricated on Si/SiO_2 substrates. Atomic force microscopy (AFM) images [Fig. 1(b) and (c)] show that these feature dimensions directly determine the resulting relief topography in the polymer. The resist is imprinted at room temperature using an arbor press at 10 MPa for 10–20 s, and then the imprinted LOR is etched to the SiO_2 layer using anisotropic RIE (CF_4 plasma at 100 W and 100 mtorr), and metal electrodes (10-nm Cr, 50-nm Au) are deposited by thermal evaporation. The polymer and metal are finally lifted off in Remover PG (MicroChem) at 80 °C.

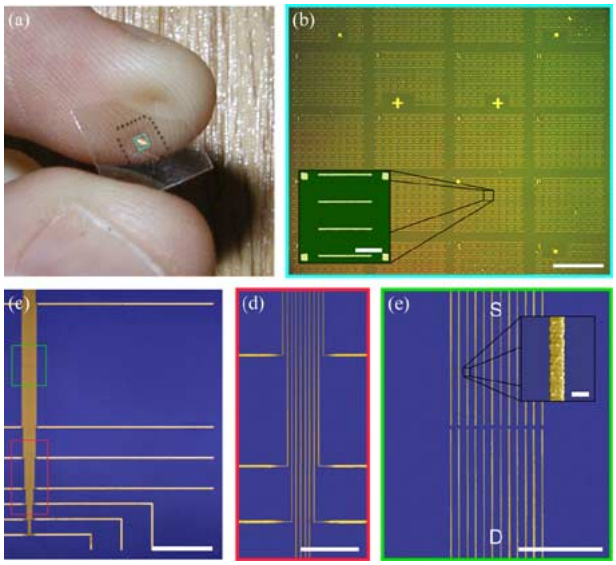

Fig. 2. (a) Digital photograph of an NIL-patterned mylar substrate with the patterned gate array highlighted by the central blue box. (b) Optical image of hierarchically-patterned arrays of gate electrodes; the scale bar is 100 μm. (inset) Scanning electron microscopy (SEM) image of a gate array block, where corner squares are alignment marks. Scale bar is 5 μm. (c) Optical image of S–D array and interconnect wires; the scale bar is 100 μm. (d) Optical image of 200-nm S–D lines and 1-μm interconnect lines from an area highlighted by the red box in (c). Scale bar is 25 μm. (e) Field-emission SEM image of S–D array; scale bar is 20 μm. (inset) SEM image of sub-200-nm-width channel lines; scale bar is 200 nm.

This approach was used to create nanometer-scale metal features over large areas on plastic substrates. In particular, electrodes commonly used for NW and nanotube field-effect devices [20], [28] were fabricated: thin gate level lines, and narrow source–drain level contacts. Figs. 2(a) and (b) show clearly that NIL can readily yield 300-nm-width gate lines in highly regular 135 × 105 μm arrays which are tiled over the plastic substrate to the millimeter scale. In addition, this image highlights micrometer-wide crosses and squares that were patterned simultaneously with the gates electrodes; these latter features can be used to enable subsequent lithographic alignment and device fabrication [29]. Similarly, Figs. 2(c)–(e) show an array of split pair source-drain electrodes and interconnects extending over several hundred micrometers. Larger scale interconnect wires consist of 1-μm-width features, which transition smoothly even at right angles to sub-200-nm-width lines with a 2-μm pitch and a 500-nm source–drain gap between each split electrode pair [Fig. 2(e)]. It should be noted that device applications of such structures are not limited to those mentioned; indeed, this process may have potential in creating floating gates for nonvolatile nanoscale memory applications [30], as well as in addressing problems in directed assembly of nanoscale building block elements [18], [31].

III. High-Performance Devices on Flexible Plastics

As outlined in Fig. 3, semiconductor NWs can be synthesized in single-crystalline form under conditions of high

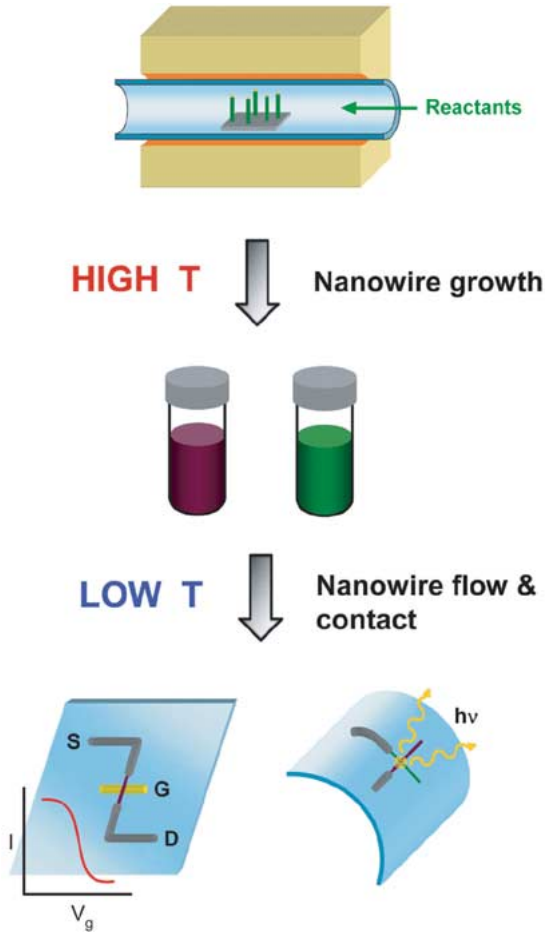

Fig. 3. NW growth and device assembly on glass and plastic substrates. High-quality NWs of desired composition (purple, green) are prepared in a high-temperature process and subsequently dispersed into solution. Room temperature solution-based assembly onto glass and plastic then yields devices with diverse functionalities.

temperature and pressure with precisely controlled structures, chemical compositions, and doping/electronic properties using a gold nanocluster-catalyzed vapor–liquid–solid growth process [14], [15]. Following growth, the NWs can be readily isolated as stable solution suspensions by sonication of the growth substrate in ethanol for 5–10 s [32]. These solutions are subsequently used for deposition and patterning of NW devices. Thus, the growth stage is independent of the fabrication stage of active devices, so there are no thermal or other substrate limitations. We take advantage of these unique features by separating the high-temperature synthesis of single-crystal NWs from ambient solution-based assembly on plastics to enable fabrication of single-crystal-like devices that greatly exceed the characteristics of amorphous silicon and organic materials.

We illustrate this approach with the assembly of 20-nm-diameter p-type silicon NWs—grown from 20-nm gold nanoclusters with $SiH_4 : B_2H_6$ (8000 : 1) as reactants—into FETs [15], [17] on flexible plastic substrates (SiNW/plastic FETs). This process involves: 1) patterning of gate electrodes on plastic with photolithography or NIL and deposition of a 30-nm SiO_2 gate dielectric; 2) fluid-directed assembly [32] of NWs across the gate electrodes; and 3) lithography and

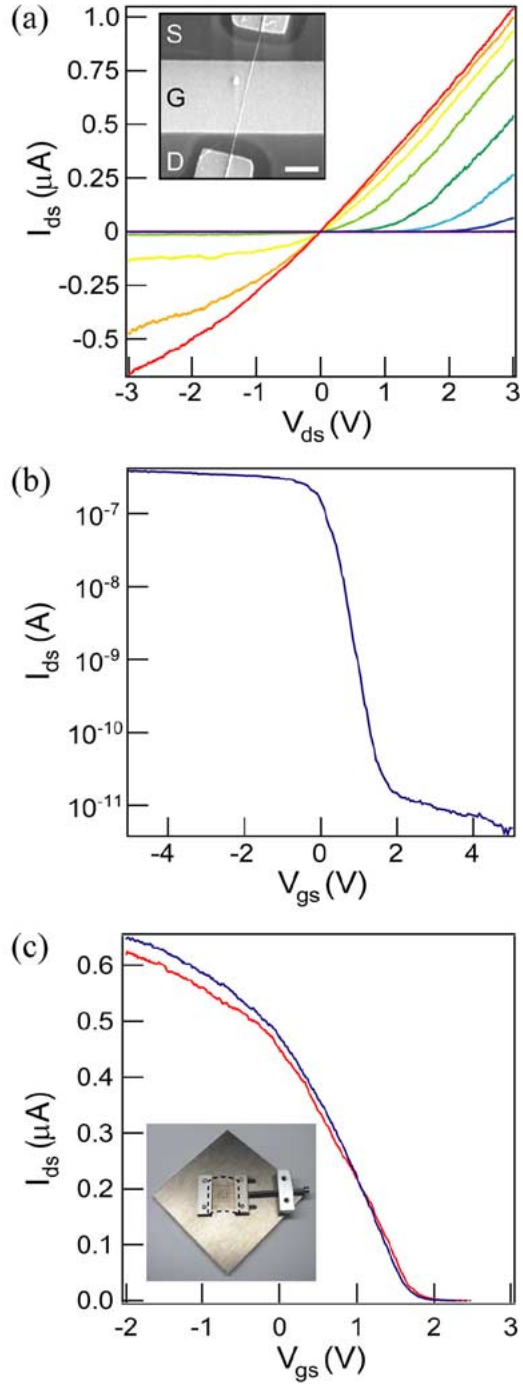

Fig. 4. High-performance p-SiNW devices on plastic. (a) $I_{\rm ds}$ versus $V_{\rm ds}$ curves for a 20-nm SiNW transistor on a mylar substrate, where the red, orange, yellow, . . . blue, and purple curves correspond to $V_{\rm gs} = -5, -4, -3, \ldots 2$, and 3 V, respectively. (inset) SEM image of the NW device. The source (S), drain (D), and gate (G) are labeled. Scale bar is 1 μm. (b) $I_{\rm ds}$ versus $V_{\rm gs}$ ($V_{\rm ds} = 1$ V) for the device shown in (a). (c) Effect of substrate bending on NW device performance. $I_{\rm ds}$ versus $V_{\rm gs}$ for an NW transistor device measured when the substrate was flat (blue curve) and bent to a radius of curvature of 0.3 cm (red curve). (inset) Photograph of the device used for bending the flexible plastic chip and securing it during measurement. The chip is highlighted with a black dashed line.

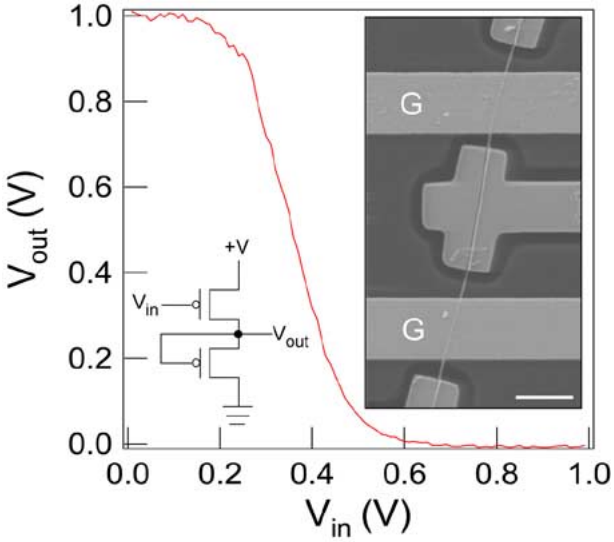

Fig. 5. $V_{\rm out}$ versus $V_{\rm in}$ for an NW inverter assembled from a p-SiNW on plastic. Left inset: Schematic of the device. Right inset: SEM image of the device, in which the NW is oriented in the vertical direction crossing two gates (G). Scale bar is 2 μm.

metallization of 80-nm Pd to form source–drain contacts to the NWs. Due to limitations of the plastic, 80-nm Pd contacts to the NW FETs were not annealed; in other words, the post-NW synthesis processing was performed entirely at room temperature. Despite the lack of an anneal, current versus source–drain voltage curves [$I_{\rm ds}$ versus $V_{\rm ds}$, Fig. 4(a)] show clear current saturation behavior and are linear about the origin, indicating that contacts to NWs on plastic behave in a practical sense as ohmic. Key characteristics of NW FETs were determined from $I_{\rm ds}$ versus $V_{\rm gs}$ data [Fig. 4(b)]. The transconductance has a value of 340 nA-V^{-1}, from which a hole mobility of ~ 200 cm^2-V^{-1}-s^{-1} can be calculated [33]. Notably, this hole mobility value is comparable to that observed in single-crystal p-type silicon at similar doping ratios [34]. In addition, the $I_{\rm ds}$ versus $V_{\rm gs}$ curve shows a threshold voltage of 0.5–1.5 V, an on/off ratio of $\sim 10^5$, and a subthreshold slope 340 mV per decade change in current. Finally, Fig. 4(c) shows that the NW/plastic device experienced less than a 10% drop in on current when the chip was bent to a radius of curvature of 0.3 cm and measured in the bent state. This last point is significant because one of the attractive features of plastic is its flexibility, and the small change in device performance despite a large induced stress highlights the robust nature of our SiNW/plastic transistors.

The values of the mobilities obtained from SiNW/plastic devices are comparable to the highest values reported for p-channel polycrystalline silicon transistors on alternative substrates, 200 cm^2-V^{-1}-s^{-1} on nonalkali glass [10]; and, strikingly, are at least two to three orders of magnitude larger than typical values observed for amorphous silicon and organic transistors on glass and plastic substrates [9], [13]. Furthermore, the threshold voltages and subthreshold swings, which are similar to values reported for polysilicon transistors [35], but lower than amorphous silicon [36]–[39] and organics [40]–[43], suggest advantages for low-power operation. The on/off current ratios of the NW devices reported here are lower than the best amorphous silicon transistor values, 10^6–10^8, on glass and plastic [9], [37], although recent progress on NW devices suggests that similar

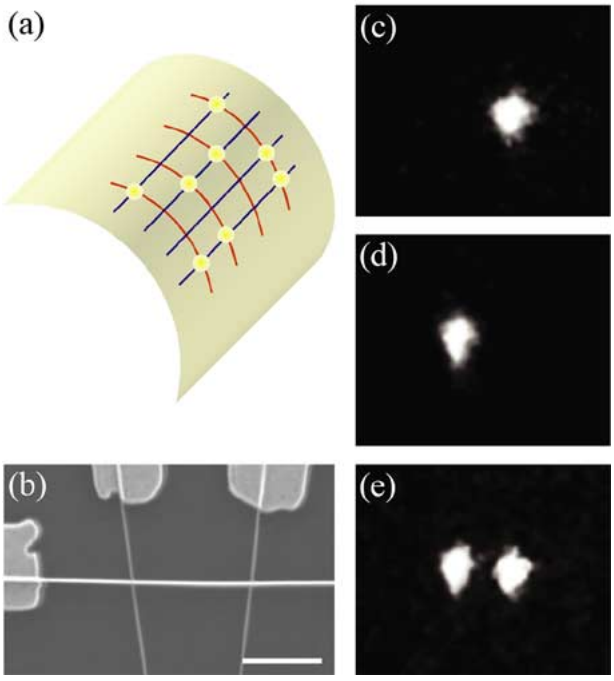

Fig. 6. LED array on plastic. (a) Schematic of a flexible self-emitting display consisting of a crossed-NW LED array on a flexible plastic substrate. (b) SEM image of two p-SiNWs (vertical) crossing an n-type GaN NW to form two LEDs on the plastic substrate. Scale bar is 1 μm. (c)-(e) Electroluminescence (EL) images of localized emission from forward-biased Si-GaN junctions. The junctions can be driven individually (c), (d) or simultaneously (e).

values are possible and that on currents can be significantly increased by, for example, using multiple-NW-based devices [44].

The assembly of high-performance SiNW devices on flexible plastic substrates can also be readily extended to logic structures. A single p-SiNW can be configured as an inverter or logic NOT device (Fig. 5) by defining two FETs on a single NW, in which one FET is the drive transistor and the other functions as an active load [45]. The voltage output $(V_{\rm out})$ versus voltage input $(V_{\rm in})$ of this device shows that the inverter has a dc gain of four. The 1-V operating range of this inverter is significantly lower than the 5–10 V reported for inverters fabricated using organic transistors [46], [47] and thus suggests advantages for low-power logic applications on plastics.

Since NW functionality is determined during the independent growth phase of the process, our general strategy for fabricating high-performance electronic devices on plastic substrates can be readily applied to assemble other functional NWs in addition to Si. For example, assembly of crossed-NW LEDs [18], [48] on plastic substrates could enable flexible self-emitting displays [Fig. 6(a)] similar to organic LEDs [49], [50]. Compared to organic LEDs, NWs have several advantages: 1) they are robust inorganic materials; 2) different materials have a wide range of spectrally pure output colors; and 3) NW transistor drive and LED devices potentially can be integrated together on a single sheet of plastic or glass without the need for polycrystalline silicon. Specifically, crossed-NW UV LEDs from n-type GaN NWs [16], [48] and p-type SiNWs assembled onto plastic show that when either one or both of the p-n diodes of a 1 $\times$ 2 n-GaN/p-Si crossed-NW device [Fig. 6(b)] were forward biased, localized and addressable emission was observed from the junctions [Figs. 6(c)–(e)]. Significantly, these NW-based UV LEDs can maintain their emissive properties upon repeated cycles of bending and unbending of the plastic substrate.

IV. Summary

We have demonstrated NIL of nanometer- through millimeter-scale features on flexible plastic substrates with high uniformity and excellent reproducibility over large areas. Selection of a suitable resist allowed for successful transfer of these features at room temperature. Moreover, we have outlined a broad and rational strategy for the assembly of high-quality single-crystal NWs onto flexible plastic substrates to create high-performance FET and LED devices. By separating the high-temperature synthesis of single-crystal NWs from the ambient-temperature solution-based assembly, we enabled fabrication of single-crystal devices that greatly exceed the characteristics of amorphous silicon and organic materials. Recent studies employing advanced solution-based assembly and patterning techniques have demonstrated control over the hierarchical organization of fully interconnected SiNW FETs to create high-speed integrated logic structures over large areas on glass substrates [44], [51]. Thus, we believe that our development of simple and reproducible high-resolution patterning of plastics using NIL combined with the versatile function of NW building blocks could open up exciting opportunities over many length scales for plastic macroelectronics, photonics, and other areas.

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References

[1] A. C. Bonora, "Silicon wafer process technology: Slicing, etching, polishing," in *Proc. Electrochemical Soc.*, vol. 77–2, 1977, pp. 154–169.

[2] J. M. Xu, "Plastic electronics and future trends in microelectronics," *Synth. Met.*, vol. 115, pp. 1–3, Nov. 2000.

[3] Y. Hamakawa, "From bulk crystalline age to multilayered thin film age—A technological evolution from micro- to macroelectronics," *Sens. Mater.*, vol. 3, no. 1, pp. 9–23, Jan. 1991.

[4] E. Lueder, *Liquid Crystal Displays: Addressing Schemes and Electro-Optical Effects*. Chichester, U.K.: Wiley, 2001.

[5] R. F. Service, "New age semiconductors pick up the pace," *Science*, vol. 287, pp. 415–417, Jan. 2000.

[6] S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," *MRS Bull.*, vol. 27, pp. 881–885, Nov. 2002.

[7] R. L. Wisnieff and J. J. Ritsko, "Electronic displays for information technology," *IBM J. Res. Develop.*, vol. 44, no. 3, pp. 409–422, May 2000.

[8] J. M. Shaw and P. F. Seidler, "Organic electronics: Introduction," *IBM J. Res. Develop.*, vol. 45, no. 1, pp. 3–9, Jan. 2001.

[9] Y. Chen *et al.*, "Electronic paper: Flexible active-matrix electronic ink display," *Nature*, vol. 423, pp. 136–136, May 2003.

[10] A. Hara *et al.*, "High-performance polycrystalline silicon thin film transistors on nonalkali glass produced using continuous wave laser lateral crystallization," *Jpn. J. Appl. Phys.*, pt. 2, vol. 41, no. 3B, pp. L311–L313, Mar. 2002.
[11] J. A. Rogers *et al.*, "Paper-like electronic displays: Large-area rubber-stamped plastic sheets of electronics and microencapsulated electrophoretic inks," *Proc. Nat. Acad. Sci. USA*, vol. 98, no. 9, pp. 4835–4840, Apr. 2001.
[12] H. Sirringhaus *et al.*, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, pp. 2123–2126, Dec. 2000.
[13] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM J. Res. Develop.*, vol. 45, no. 1, pp. 11–27, Jan. 2001.
[14] C. M. Lieber, "Nanoscale science and technology: Building a big future from small things," *MRS Bull.*, vol. 28, pp. 486–491, Jul. 2003.
[15] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowires field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149–152, Jan. 2003.
[16] Y. Huang, X. Duan, Y. Cui, and C. M. Lieber, "Gallium nitride nanowire nanodevices," *Nano Lett.*, vol. 2, no. 2, pp. 101–104, Jan. 2002.
[17] Y. Huang *et al.*, "Logic gates and computation from assembled nanowires building blocks," *Science*, vol. 294, pp. 1313–1317, Nov. 2001.
[18] X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, pp. 66–69, Jan. 2001.
[19] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, pp. 1289–1292, Aug. 2001.
[20] M. C. McAlpine *et al.*, "High-performance nanowires electronics and photonics on glass and plastic substrates," *Nano Lett.*, vol. 3, no. 11, pp. 1531–1535, Oct. 2003.
[21] M. C. McAlpine, R. S. Friedman, and C. M. Lieber, "Nanoimprint lithography for hybrid plastic electronics," *Nano Lett.*, vol. 3, no. 4, pp. 443–445, Mar. 2003.
[22] G. M. Whitesides and J. C. Love, "Nanofabrication: The art of building small," *Sci. Am.*, pp. 38–47, Sep. 2001.
[23] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint lithography with 25-nanometer resolution," *Science*, vol. 272, pp. 85–87, Apr. 1996.
[24] B. Heidari, I. Maximov, and L. Montelius, "Nanoimprint lithography at the 6 in. wafer scale," *J. Vac. Sci. Technol. B*, vol. 18, no. 6, pp. 3557–3560, Nov./Dec. 2000.
[25] M. Li, L. Chen, and S. Y. Chou, "Direct three-dimensional patterning using nanoimprint lithography," *Appl. Phys. Lett.*, vol. 78, no. 21, pp. 3322–3324, May 2001.
[26] T. Borzenko, M. Tormen, G. Schmidt, L. W. Molenkamp, and H. Janssen, "Polymer bonding process for nanolithography," *Appl. Phys. Lett.*, vol. 79, no. 14, pp. 2246–2248, Aug. 2001.
[27] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Nanoimprint lithography," *J. Vac. Sci. Technol. B*, vol. 14, no. 6, pp. 4129–4133, Nov./Dec. 1996.
[28] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, "Carbon nanotube inter- and intramolecular logic gates," *Nano Lett.*, vol. 1, no. 9, pp. 453–456, Sep. 2001.
[29] K. Pfeiffer *et al.*, "Multistep profiles by mix and match of nanoimprint and UV lithography," *Microelectron. Eng.*, vol. 57–58, pp. 381–387, Sep. 2001.
[30] G. Groeseneken, H. E. Maes, J. van Houdt, and J. S. Witters, "Basics of nonvolatile semiconductor memory devices," in *Nonvolatile Semiconductor Memory Technology*, W. D. Brown and J. E. Brewer, Eds. New York: IEEE, 1998, ch. 1.
[31] H. Matsui, P. Porrata, and G. E. Douberly Jr, "Protein tubule immobilization on self-assembled monolayers on Au substrates," *Nano Lett.*, vol. 1, no. 9, pp. 461–464, Aug. 2001.
[32] Y. Huang, X. Duan, Q. Wei, and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science*, vol. 291, pp. 630–633, Jan. 2001.
[33] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multiwall carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 73, no. 17, pp. 2447–2449, Aug. 1998.
[34] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981, ch. 1.
[35] D. P. Gosain, "Excimer laser crystallized poly-Si TFT's on plastic substrates," *Proc. SPIE*, vol. 4426, pp. 394–400, 2002.
[36] B. Stannowski, R. E. I. Schropp, R. B. Wehrspohn, and M. J. Powell, "Amorphous-silicon thin-film transistors deposited by VHF-PECVD and hot-wire CVD," *J. Non-Crystal. Solids*, vol. 299–302, pp. 1340–1344, Apr. 2002.
[37] W. S. Wong *et al.*, "Jet-printed fabrication of a-Si: H thin-film transistors and arrays," *J. Non-Cryst. Solids*, vol. 299–302, pp. 1335–1339, Apr. 2002.
[38] H. Gleskova, S. Wagner, V. Gasparik, and P. Kovac, "150 °C amorphous silicon thin-film transistor technology for polyimide substrates," *J. Electrochem. Soc.*, vol. 148, no. 7, pp. G370–G374, May 2001.
[39] P. I. Hsu *et al.*, "Thin-film transistor circuits on large-area spherical surfaces," *Appl. Phys. Lett.*, vol. 81, no. 9, pp. 1723–1725, Jul. 2002.
[40] M. Halik *et al.*, "Polymer gate dielectrics and conducting-polymer contacts for high-performance organic thin-film transistors," *Adv. Mater.*, vol. 14, no. 23, pp. 1717–1722, Dec. 2002.
[41] H. Klauk *et al.*, "Pentacene organic transistors and ring oscillators on glass and on flexible polymeric substrates," *Appl. Phys. Lett.*, vol. 82, no. 23, pp. 4175–4177, Apr. 2003.
[42] Y.-M. Kim *et al.*, "All-organic thin-film transistors using photoacryl as a gate insulator," *Opt. Mater.*, vol. 21, pp. 425–428, Jan. 2003.
[43] D. Knipp, R. A. Street, A. Völkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport," *J. Appl. Phys.*, vol. 93, no. 1, pp. 347–355, Jan. 2003.
[44] S. Jin *et al.*, "Scalable interconnection and integration of nanowires devices without registration," *Nano Lett.*, vol. 4, no. 5, pp. 915–919, Apr. 2004.
[45] P. Horowitz and W. Hill, *The Art of Electronics*. Cambridge, U.K.: Cambridge Univ. Press, 1989, pp. 153–4.
[46] J. A. Rogers, A. Dodabalapur, Z. Bao, and H. E. Katz, "Low-voltage 0.1 μm organic transistors and complementary inverter circuits fabricated with a low-cost form of near-field photolithography," *Appl. Phys. Lett.*, vol. 75, no. 7, pp. 1010–1012, Jun. 1999.
[47] G. H. Gelinck, T. C. T. Geuns, and D. M. de Leeuw, "High-performance all-polymer integrated circuits," *Appl. Phys. Lett.*, vol. 77, no. 10, pp. 1487–1489, Jul. 2000.
[48] Z. Zhong, F. Qian, D. Wang, and C. M. Lieber, "Synthesis of p-type gallium nitride nanowires for electronic and photonic nanodevices," *Nano Lett.*, vol. 3, no. 3, pp. 343–346, Feb. 2003.
[49] J. R. Sheats *et al.*, "Organic electroluminescent devices," *Science*, vol. 273, pp. 884–888, Aug. 1996.
[50] W. E. Howard and O. F. Prache, "Microdisplays based upon organic light-emitting diodes," *IBM J. Res. Dev.*, vol. 45, no. 1, pp. 115–127, Jan. 2001.
[51] R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, and C. M. Lieber, "High-speed integrated nanowire circuits," Nature, vol. 434, p. 1085, Apr. 2005, submitted for publication.

Michael C. McAlpine was born in St. Louis, MO, in 1978. He received the B.S. degree with honors in chemistry from Brown University, Providence, RI, in 2000 and the A.M. degree in chemistry from Harvard University, Cambridge, MA, in 2002. He is currently working toward the Ph.D. degree at Harvard University.

As an undergraduate, he studied reversible binding of oxygen to inorganic coordination complexes at room temperature. He also performed a summer fellowship at the University of Pennsylvania, where he studied charge density rearrangements in ferroelectric materials. His current interests include the study of nanowire ac measurements and logic on plastic substrates.

Mr. McAlpine received a National Science Foundation Graduate Research Fellowship in 2000.

Robin S. Friedman was born in Van Nuys, CA, in 1979. He received the B.S. degree with honors in chemistry from the California Institute of Technology, Pasadena, in 2001 and the A.M. degree in chemistry from Harvard University, Cambridge, MA, in 2004. He is currently working toward the Ph.D. degree in chemistry at Harvard University.

His undergraduate research focused on polymer-based sensors and their use in land mine detection, as well as theoretical studies of binary phase diagrams and protein folding. His current research is primarily focused on semiconductor nanowire growth, characterization, and assembly into electronic devices.

Charles M. Lieber was born in Philadelphia, PA, in 1959. He received the B.A. degree with honors in chemistry from Franklin and Marshall College, Lancaster, PA, in 1981 and the Ph.D. degree in chemistry from Stanford University, Stanford, CA, in 1985.

He performed postdoctoral research at the California Institute of Technology, and in 1987 assumed an Assistant Professor position at Columbia University. There he embarked upon a research program addressing the synthesis and properties of low-dimensional materials. In 1991, he moved to Harvard University, Cambridge, MA, and now holds a joint appointment in the Department of Chemistry and Chemical Biology, as the Mark Hyman Professor of Chemistry, and the Division of Engineering and Applied Sciences. He has published more than 230 papers in peer-reviewed journals and is the principal inventor on more than 20 patents. He serves on the Editorial and Advisory Boards of a number of science and technology journals. His interests include the synthesis of a broad range of nanoscale materials, the characterization of unique physical properties in these materials, and the development of methods in hierarchical assembly of nanoscale wires, together with the demonstration of applications of these materials in nanoelectronics, nanocomputing, biological and chemical sensing, and nanophotonics.

Prof. Lieber has been recognized by a number of scientific awards, including the ACS Award in the Chemistry of Materials (2004), Scientific American Award in Nanotechnology and Molecular Electronics (2003), World Technology Award in Materials (2003), New York Intellectual Property Law Association Inventor of the Year (2003), APS McGroddy Prize for New Materials (2003), Harrison–Howe Award (2002), MRS Medal (2002), Feynman Award in Nanotechnology (2001), NSF Creativity Award (1996), and ACS Pure Chemistry Award (1992). He is an Elected Member of the National Academy of Sciences and the American Academy of Arts and Sciences and a Fellow of the American Physical Society and the American Association for the Advancement of Science.