Nanoscale Molecular-Switch Crossbar Circuits

Sung Hyun Jo

Ph.D. Student, Dept. of Electrical Engineering & Computer Science

Ken Loh

Ph.D. Student, Dept. of Civil & Environmental Engineering

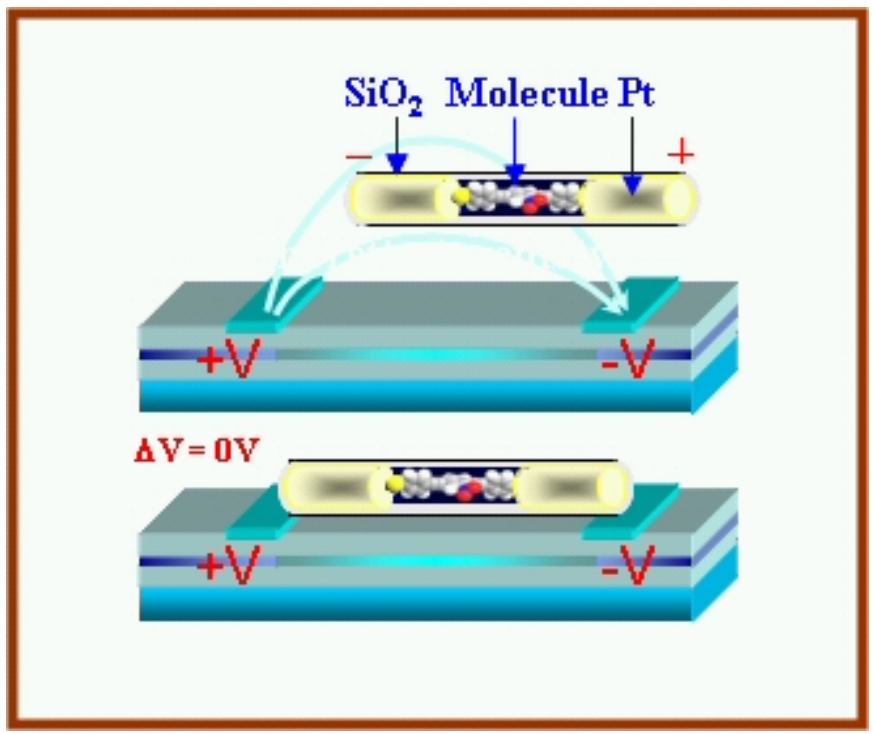
EECS 598 Nanoelectronics Week 12 Presentation
Ann Arbor, MI

November 29, 2005

Research Motivation

- **Develop nanoscale device that switches an electric current on or off**

- **Demonstrate economically viable fabrication process for nanoscale molecular devices while maintaining desired electronic properties**



Preliminary Requirements

- **Build a nanoscale circuit that controllably links very large numbers of these devices with each other and with external systems**
  - To perform memory and/or logic functions
- **Design an architecture that allows the circuits to communicate with other systems and operate independently of their lower-level details**
- **Solution**
  - Propose nanoscale circuits based on configurable crossbar architecture to connect molecular switches in a 2D grid

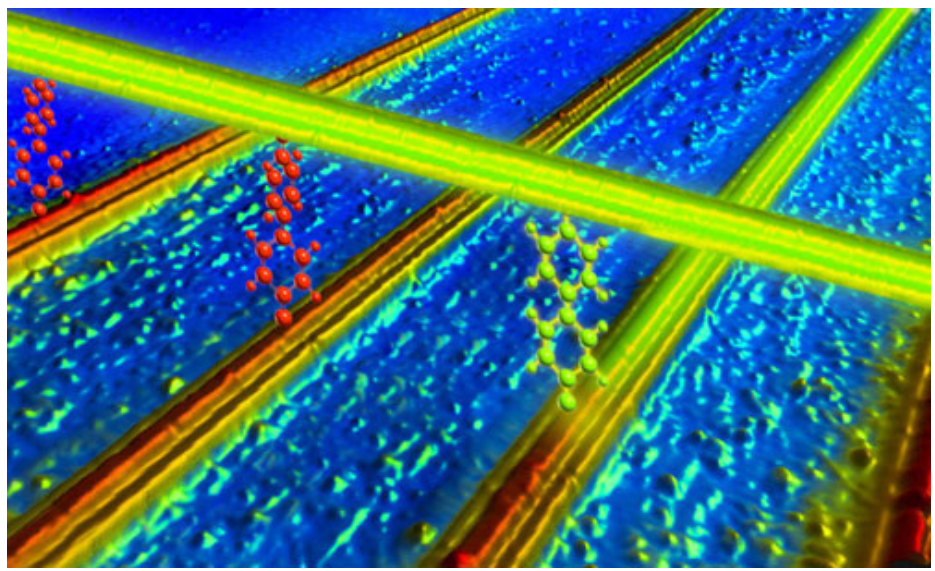
Advantages

- **Wire dimensions can be scaled down to molecular sizes**
  - Number of wires can be scaled up to form large-scale generic circuits
    - Can be configured for memory and/or logic applications
- **Requires only 2N communications to individually address 2^N nanowires with a demultiplexer**
  - Allows nano-circuit to communicate efficiently with external circuits and systems
- **Reconfigurable architecture that can tolerate defective elements generated through nanofabrication process**
- **Simple physical structure of crossbar makes nanoscale fabrication feasible and potentially inexpensive**

Crossbar Circuits (Crossbar Latches)

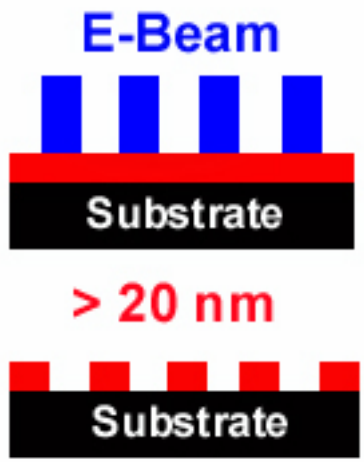
- **Crossbar circuits**
  - Network of nanoscale switches that can be activated by applying a voltage to the corresponding crossing point
  - Difficulties
    - Small size of nanowires exaggerate effects of defects and imperfections
    - Random fluctuations make it impossible to create a perfect structure from elements with the size of a few atoms
  - Solution: novel architectural design and fabrication

Right: Artist's perception of molecular electronic circuit based on crossbar circuits (Mitchell Antony)



Fabrication Methodology

- **E-beam Lithography**
  - Previous devices fabricated with such technique
  - Disadvantages
    - Impractical for commercial applications
      - Slow write speed
    - High-energy electron can damage active molecules in a circuit

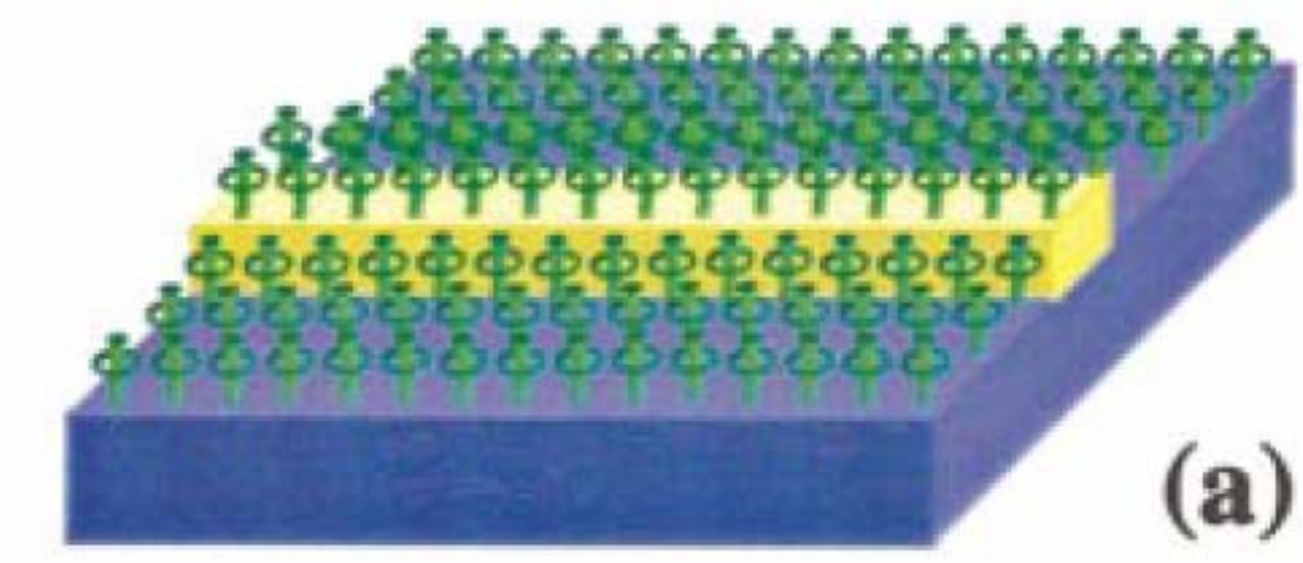


- **Imprint Lithography**
  - Can produce sub-10 nm features sizes
  - High throughput
  - Low cost
  - Preclude damage to sensitive circuit components

Imprint Lithography

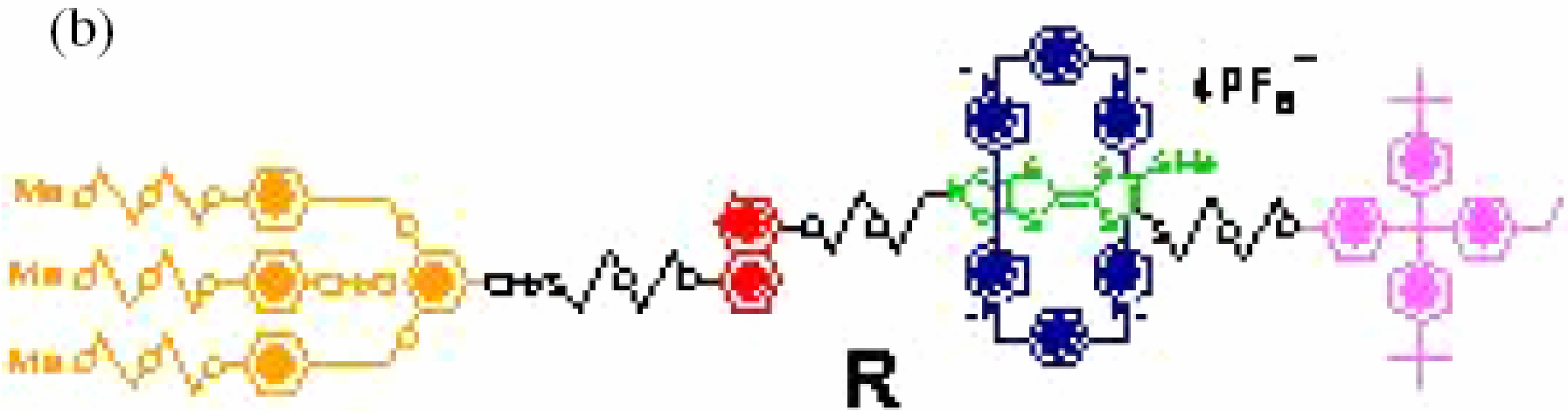
- **Fabricate nanoscale molecular devices from an amphiphilic, bistable [2]rotaxane**
  - Imprinting mold: 100-nm-thick thermally grown silicon oxide on a silicon substrate
    - Using e-beam lithography and RIE
  - SiO_2 surface patterned and etched to leave raised mesas of 40-nm-wide nanowires connected by 3-μm-wide wires to 100-μm-square pads
    - Height of mesas 80-nm
  - Device electrodes: 100-nm-thick PMMA film with 495 K molecular weight
    - Spin-coated onto silicon oxide
  - Mold heated to 150 C, pressed onto coated substrate at 1000 psi
    - Transfer pattern from mold to PMMA layer
    - Allow it to cool to room temperature
  - 5-nmTi and 10-nm-Pt layers evaporated on the substrate
  - Final acetone lift-off process removed the unpatterned field to leave the Ti/Pt nanowires and connections to the contact pads

Chen, *et al.* (2003)



- **A molecular monolayer of the [2]rotaxane R was deposited over the entire substrate**
  - Using Langmuir-Blodgett (LB) method
  - During LB film deposition, aqueous subphase maintained at pH ~ 8.5
  - T = 21 C

[2]rotaxane R

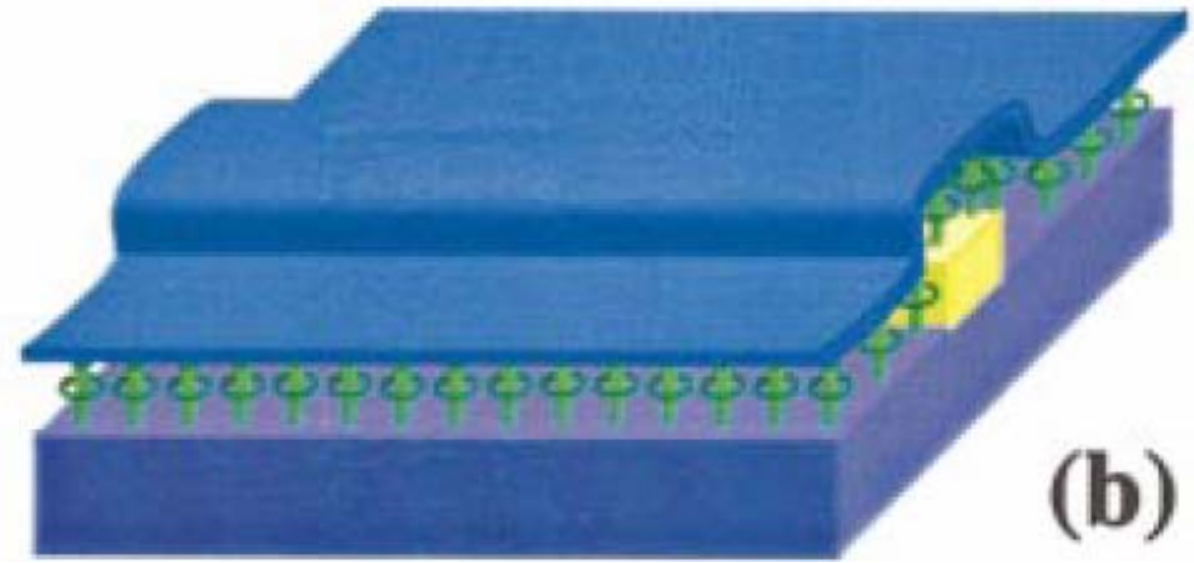


- **Above: Schematic of the bistable [2]rotaxane R**
  - Hydrophobic (purple) and hydrophilic (orange) stopper
  - Cyclobis(paraquat-*p*-phenlyene) (dark blue) as the ring component
  - Supporting counterions are hexaflourophosphate

[2]rotaxane R

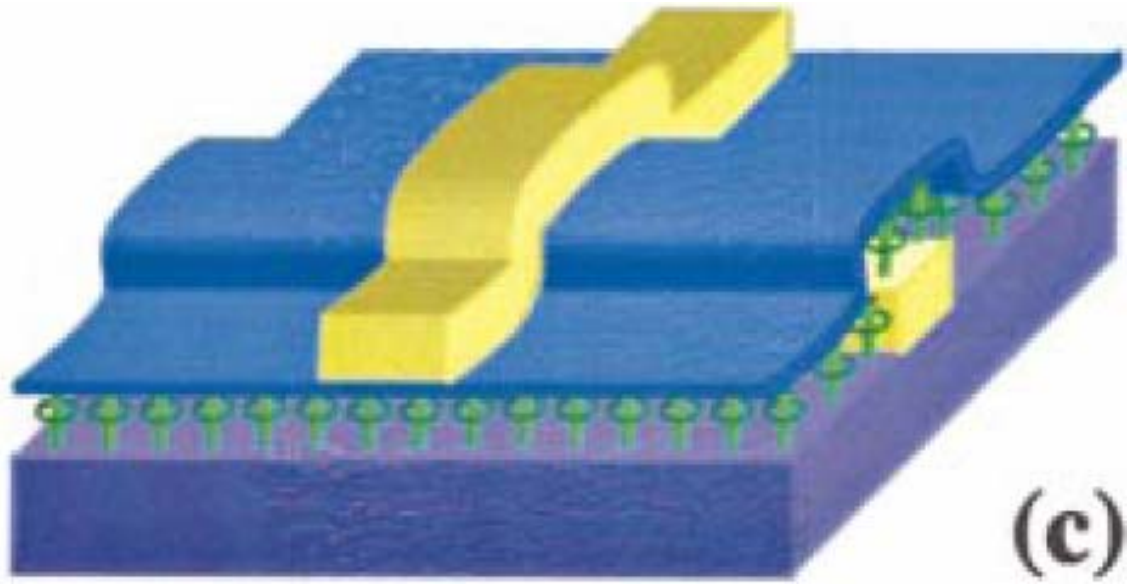
- **[2]rotaxane R form of interlocked molecule**
  - Constituted by macrocyclic ring trapped on a linear unit
  - Submolecular units may undergo relative motions such as “circumrotation”
    - Rotation of one ring inside the cavity of another
    - Prime candidate for molecular-level machines or molecular electronic devices

Chen, *et al.* (2003)



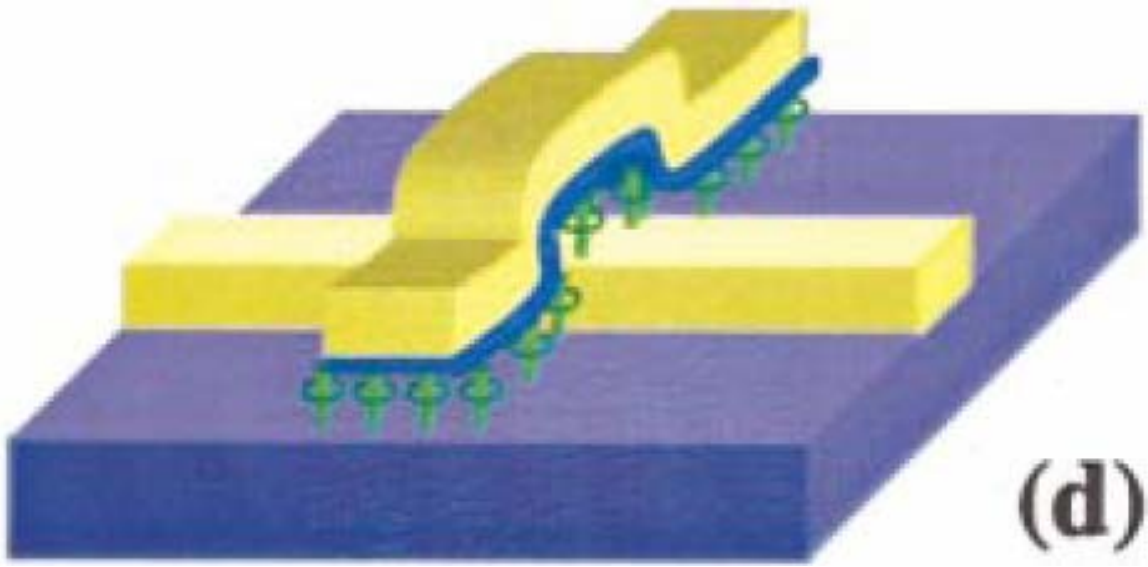
- **Fabrication of top electrode began with the blanket evaporation of a 7.5-nm Ti protective layer**
  - Ti very reactive with top functional group of molecules
  - Forms direct electrical contact with molecules
  - Blocked further metal penetration into LB molecular layers
  - Ti layer minimized subsequent damage to molecules
    - Enable further organic resist and solvent processing

Chen, *et al.* (2003)



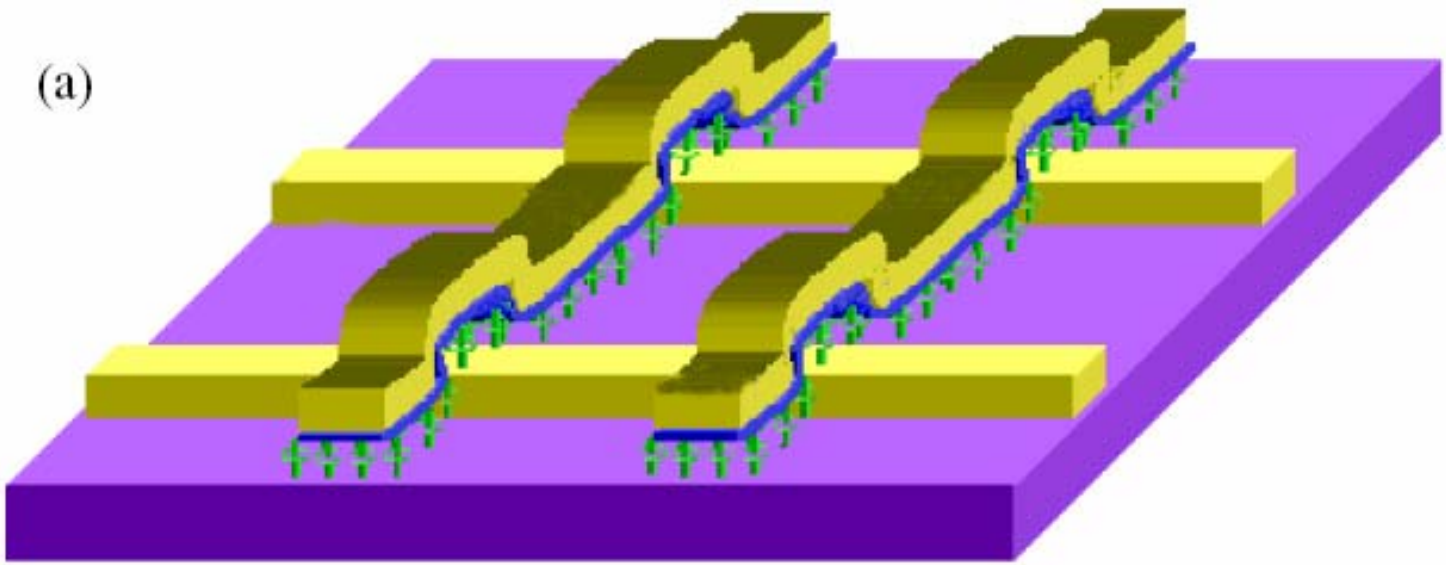
- **Patterned top electrodes of 5-nm Ti and then 10-nm Pt were fabricated with the same imprinting process**
  - Top electrodes oriented perpendicular to bottom electrodes
  - Aligned to ensure that top and bottom nanowires crossed

Chen, *et al.* (2003)



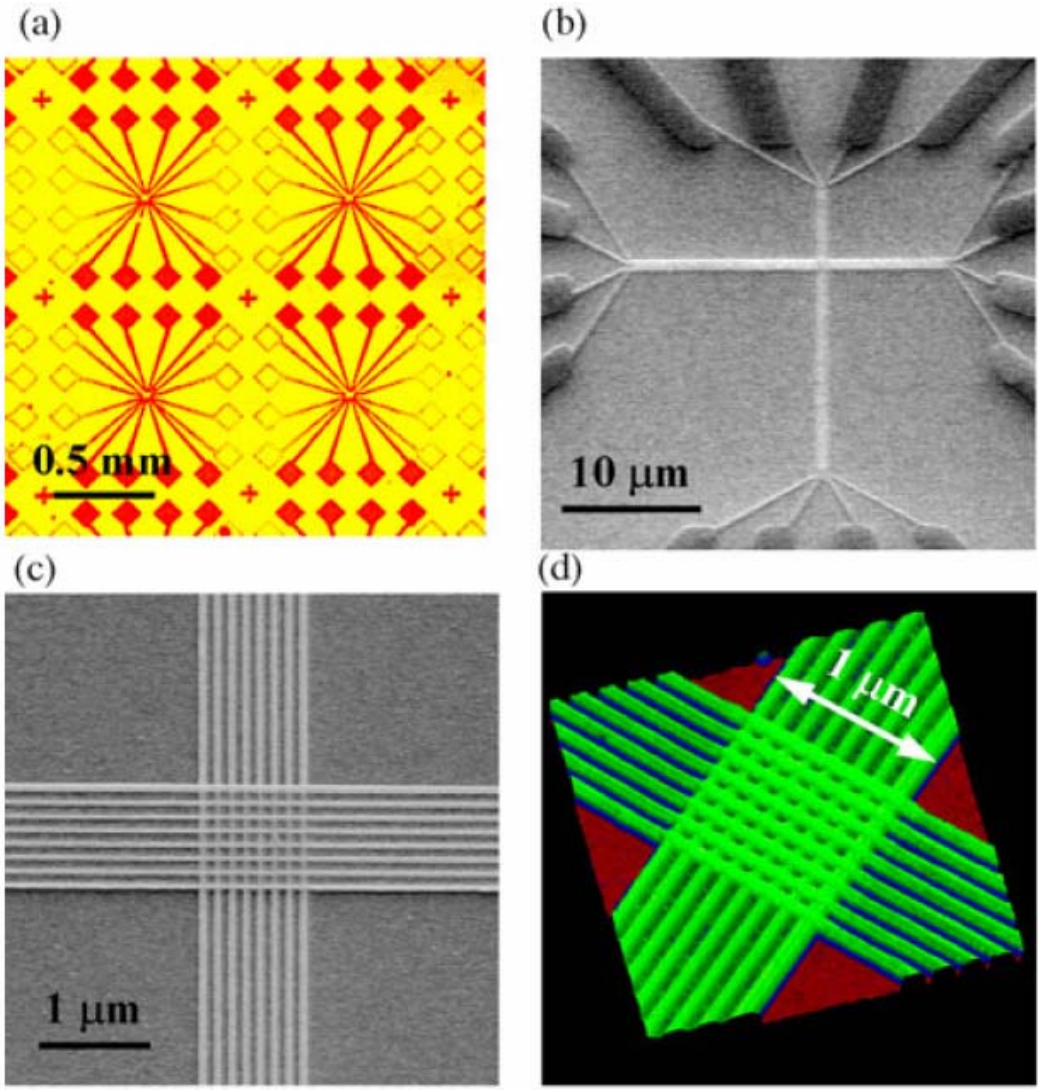
- **RIE with CF_4 and O_2 (4:1) gases used to remove the blanket Ti protective layer anisotropically down to the SiO_2 layer**
  - Pressure of 40 mTorr
  - Power of 200 W
  - Note: [2]rotaxane molecules remained stable up to ~ 210 C
    - Should not be damaged during imprinting process
- **After RIE, an array of devices with the molecular monolayer sandwiched between two metal nanowires remained**

Fabricated Crossbar Circuit



- **Crossbar circuit, fabricated by imprint lithography with process just described**
  - Monolayer of [2]rotaxane molecules sandwiched
    - Top layer: Ti(3-nm)/Pt(5-nm) nanowires
    - Bottom layer: Ti(11-nm)/Pt(5-nm) nanowires
- **Basic element in the circuit is the Pt/rotaxane/Ti junction at each cross point**
  - Acts as a reversible and nonvolatile switch
  - 64 switches connected to form 8 x 8 crossbar circuit in 1 μm^2 area

Crossbar Circuit Images



- (a) Optical microsocope image of 4 of 625 tested circuits, showing 16 contact pads
- (b) SEM image showing two mutually perpendicular arrays of nanowires
- (c) SEM image showing two sets of nanowires crossing each other
- (d) 3D AFM image of the crossbar

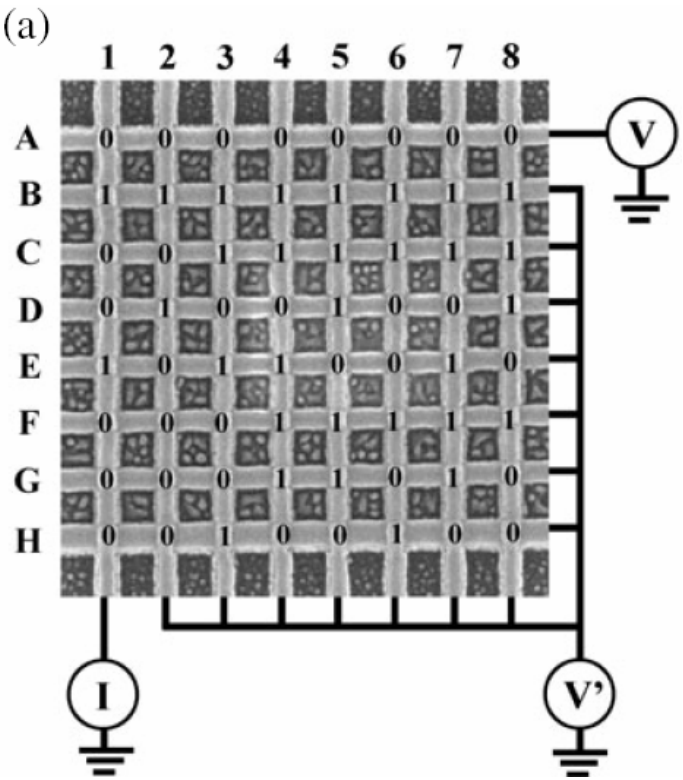
As-Built Crossbar Circuit

- **Nanowires measured width of ~40 nm**
  - Consistent with measured width of the nanowire templates on the imprint mould

- **Active device area at each cross point ~ 1600 nm^2**
  - Corresponds to ~1100R molecules sandwiched between the two electrodes
  - Determined from known density of molecules on the surface

Testing the Circuit

- **8 x 8 crossbar circuits first tested as 64-bit random access memories at room temperature**
  - All 16 nanowires electrically addressed simultaneously via contact pads
  - Computer-controlled switching matrix connected voltage sources to each nanowire and a current meter to a selected output nanowire



Left: Schematic diagram showing test confirguration for the writing and reading modes of the memory

Testing the Circuit

- **How can we test the circuit?**
  - To write one bit at a cross point, select corresponding row and column
  - Apply voltage pulse of amplitude V on top nanowire
    - Ground bottom nanowire
    - To prevent accidental writing of other bits, a voltage pulse of V' = V / 2 should be applied to all other rows and columns
- **Writing to memory**
  - Voltage pulse of duration 0.5 s and V = 3.5 V applied
    - Reduce resistance of a cross point below 5×10^8 Ω
    - If not, voltage increased in 0.5 V until resistance < 5×10^8 Ω
    - Or until voltage reaches 7.0 V
      - Bit declared as defective
- **Reading memory**
  - Bias voltage V = 0.5 V applied to selected row
  - All other rows and columns grounded (V' = 0)
  - Resistance determined by only measuring current flowing to ground via the selected column

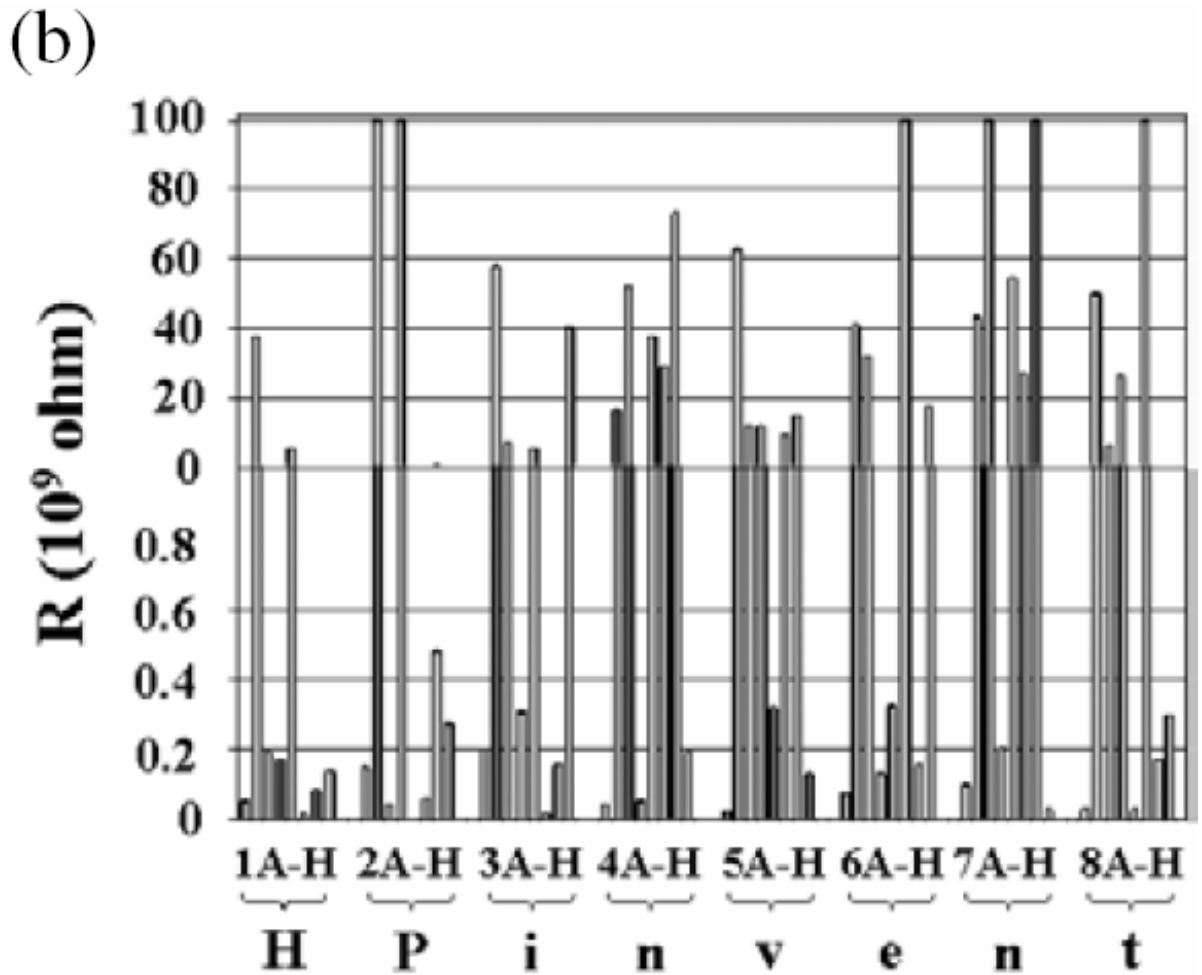
Observations

- **Device shows sharp transition from high-resistance to low-resistance state when applying positive voltage above a threshold**
  - Switching not binary
    - Resistance of junction can be tuned continuously within a certain range by applying increasing magnitude voltages

- **~85% of bits amount the 24 tested 8 x 8 crossbar circuits showed switching properties**
  - Rest of the bits either shorted ($< 10^5\ \Omega$) or open ($> 10^9\ \Omega$)
    - Open devices included some structural defects or contact problems

- **10% of trials show unintentionally writing to unintended bits**
  - Greatly improve by using a switching matrix that can bias all unselected wires to V / 2
  - Better process control to improve uniformity of the bits in an array

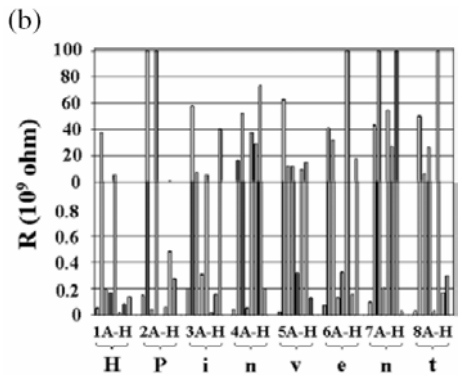
Result



Top: Resistance at each cross point in the circuit after one particular set of bits was written into a defect-free crossbar; each column corresponds to ASCII character

Result

128	64	32	16	8	4	2	1	
0	1	0	0	1	0	0	0	→ 72 = H
0	1	0	1	0	0	0	0	→ 80 = P
0	1	1	0	1	0	0	1	→ 105= i
0	1	1	0	1	1	1	0	→ 110 = n
0	1	1	1	0	1	1	0	→ 118 = v
0	1	1	0	0	1	0	1	→ 101 = e
0	1	1	0	1	1	1	0	→ 110 = n
0	1	1	1	0	1	0	0	→ 116 = t



Making it Realistic

- **Unrealistic and impractical to have direct connections to all wires**
  - Large number of nanowires
  - Micron-scale connections to nanowires

- **Necessary interface is multiplexer and demultiplexer logic circuits**
  - Can use an address code to select and transmit signals from multiple input wires to a single output wire (or single input to multiple output)
  - Offers scaling advantage
    - Requires N pairs of address wires to select and control 2^N nanowires
      - *e.g.* 10 pairs of address wires control 1024 nanowires
      - *e.g.* 20 pairs of address wires completely address a 1 Mbit crossbar memory

Multiplexer / Demultiplexer Basics

- **Multiplexer combines more than one input stream into a single output stream**
  - *e.g.* Boolean equation: Y = (A and S) or (B and not S)

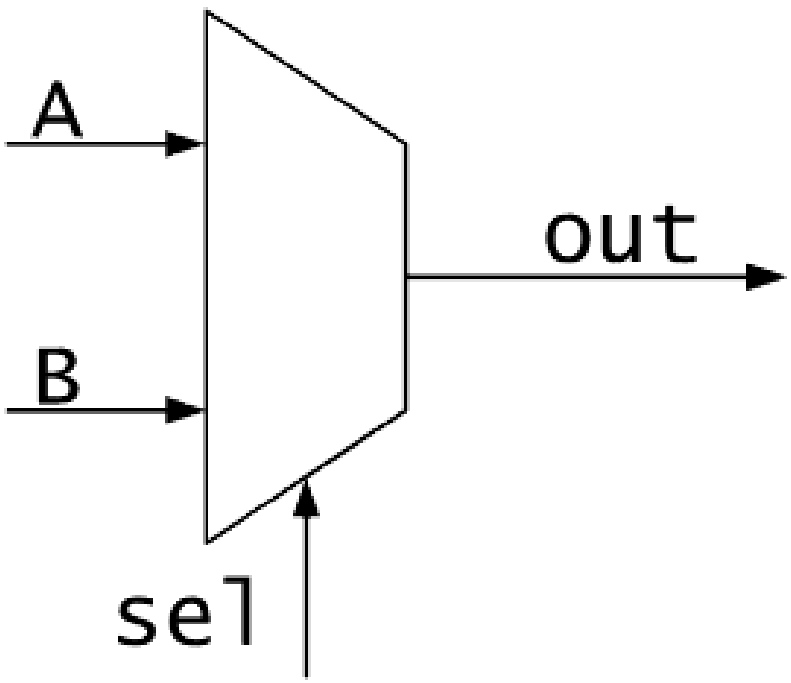
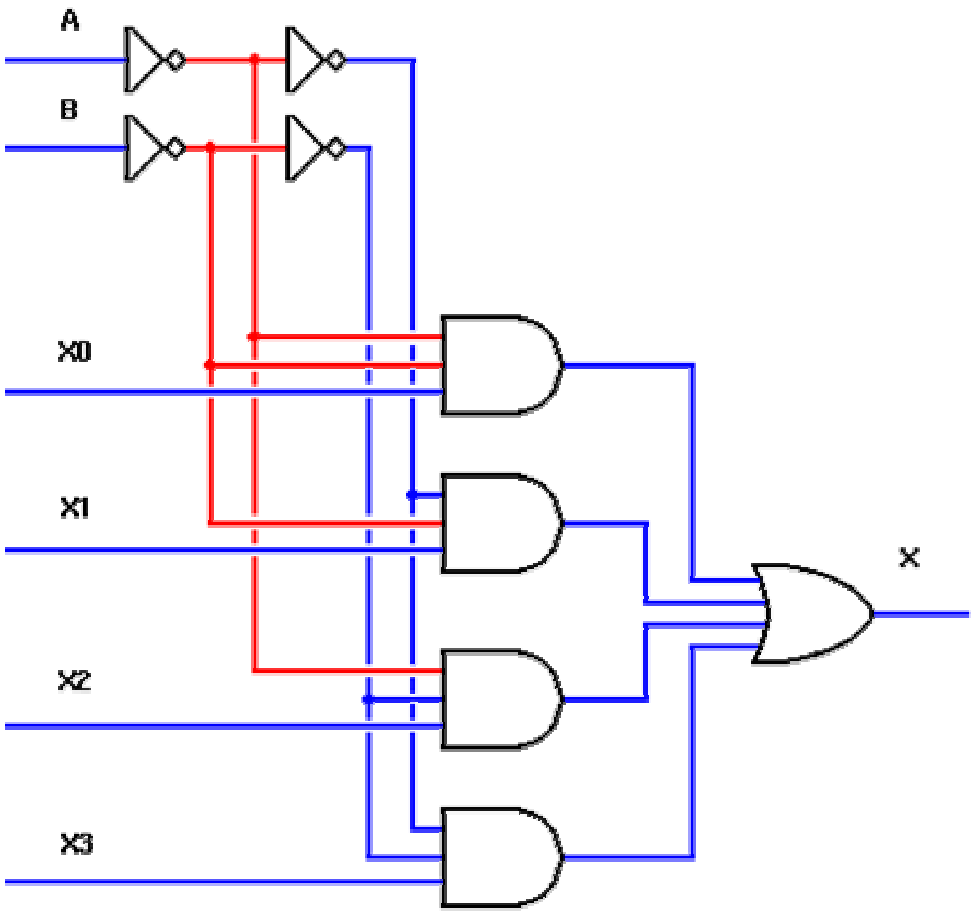
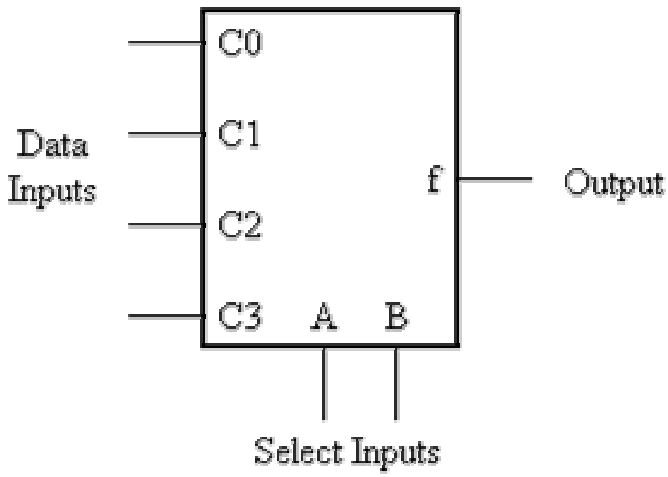


Table: Truth Table

A	B	S	Y
0	0	0	0 (Pick B)
0	0	1	0 (Pick A)
0	1	0	1 (Pick B)
0	1	1	0 (Pick A)
1	0	0	0 (Pick B)
1	0	1	1 (Pick A)
1	1	0	1 (Pick B)
1	1	1	1 (Pick A)

Multiplexer / Demultiplexer Basics

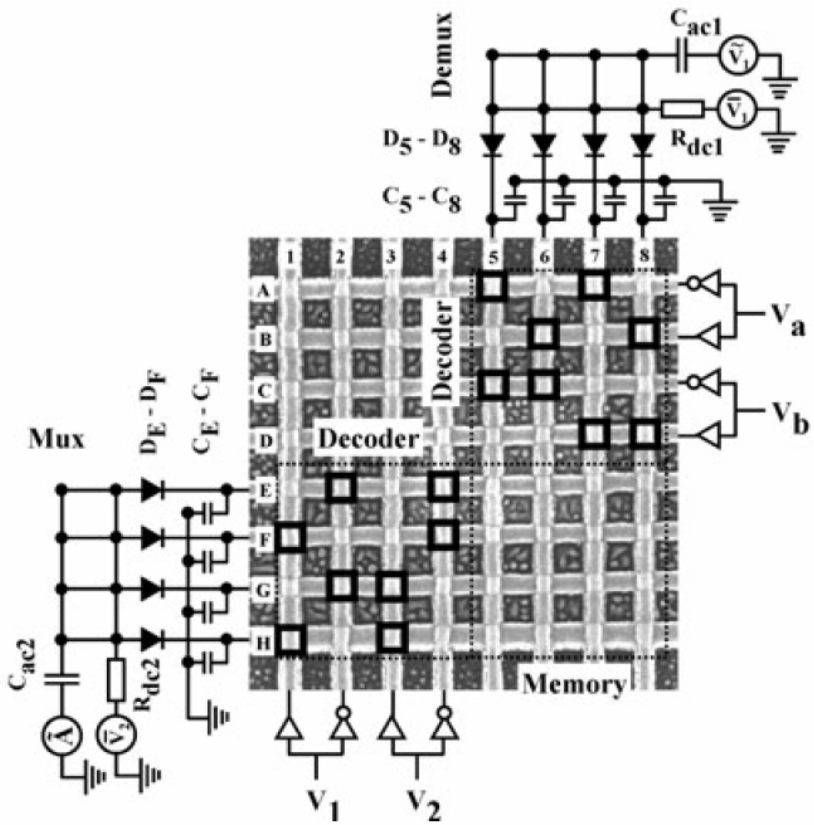




Above: 4-input multiplexer

Demultiplexer / Multiplexer

- **Configured defect-free 8 x 8 crossbar**
  - 4 x 4 crossbar memory
  - Two 4 x 4 decoders for the demultiplexer/multiplexers
    - Set resistance at specific cross points



Left: Crossbar as a combination of a 4 x 4 demultiplexer (top right), a 4 x 4 memory (bottom right), and a 4 x 4 multiplexer (bottom left)

Observations

- **As built, DC resistor-logic decoders suffer from a narrow operating range**

(b)

V_a, V_b	V_5	V_6	V_7	V_8
0, 0	0.92	0.58	0.42	**0.05**
0, 1	0.48	**0.04**	0.92	0.72
1, 0	0.62	0.95	**0.08**	0.48
1, 1	**0.03**	0.52	0.72	0.89

Improvements

- **To widen gap, designed external circuits that connect the decoders with diodes and capacitors to form functional demultiplexer and a multiplexer**
  - Optimize diodes and capacitors to improve demultiplexer
  - Demultiplexer applied an AC voltage selectively on one and only one of the nanowires

(c)

V_a, V_b	V_5	V_6	V_7	V_8
0, 0	0.2	0.2	1.3	**16.5**
0, 1	1.0	**11.9**	0.1	0.2
1, 0	0.1	0.2	**14.8**	0.1
1, 1	**13.6**	0.2	0.3	0.5

  - Multiplexer selected the AC flowing through only one of the nanowires
  - When V_1, V_2, V_a, and V_b set, current flowing through cross point was measured and its resistance determined

Further Testing

- **Resistances at arbitrary cross points in the 4 x 4 memory switched and tested using the direct reading and writing procedure**
  - External circuits disconnected

R (MΩ)	5	6	7	8
E	**36**	**163**	8706	∞
F	**171**	3062	**29**	∞
$\tilde{I}$ (pA)	5	6	7	8
E	**473**	**72**	10	9
F	**151**	7	**365**	9

  - Nanoscale circuit reconnected with external circuits for the demultiplexer and multiplexer

Summary of Results

- **From table before, by changing combinations of voltages in 2 x 4 submatrix, memory could be read**
  - Cross points with measured DC resistances < 500 MΩ corresponds to '0' state
    - Corresponding AC current > 50 pA
  - Cross points with DC resistances > 1 GΩ corresponds to '1' state
    - Corresponding AC currents < 10 pA
- **Clear threshold for the current readout to distinguish b/t 0 and 1 states**
- **Measurements beyond 2 x 4 submatrix could not identify a clear threshold**
  - Large variations of resistances at cross points in demultiplexer/multiplexer and the memory
    - Can be dealt with using different diodes and capacitors
- **Best way to scale up memory will be to improve resistance uniformity of cross points**

Other Groups

Group	Institution	Switch
J. R. Heath J. F. Stoddart	Caltech UCLA	Rotaxane monolayer between silicon and titanium nanowires
C. Lieber A. DeHon	Harvard University Caltech	Silicon nanowire field-effect transistor
M. Aono	National Institute for Materials Science, Japan	Silver sulfide ionic conductor (silver based atomic switch)
R. Waser	Research Center Juelich	Defect motion in ferroelectric thin films
K. K. Likharev	Stony Brook University	Molecular single-electron transistor
P. J. Kuekes, G. S. Snider, R. S. Williams	Hewlett-Packard Laboratories	Metal nanowire oxidation/reduction (crossbar latches)

1kilobit Crossbar Memory Circuits at 30nm half-pitch fabricated by NIL

Sung Hyun Jo

Ph.D. Student, Dept. of Electrical Engineering & Computer Science

Ken Loh

Ph.D. Student, Dept. of Civil & Environmental Engineering

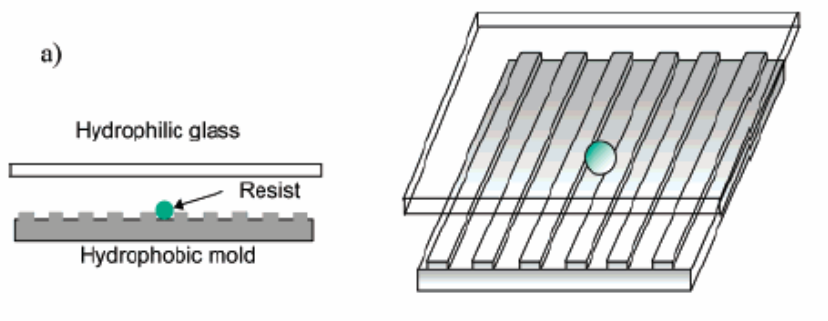
EECS 598 Nanoelectronics Week 12 Presentation
Ann Arbor, MI

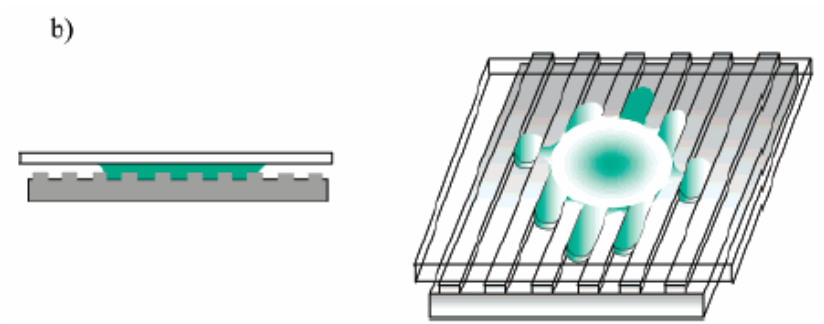
November 29, 2005

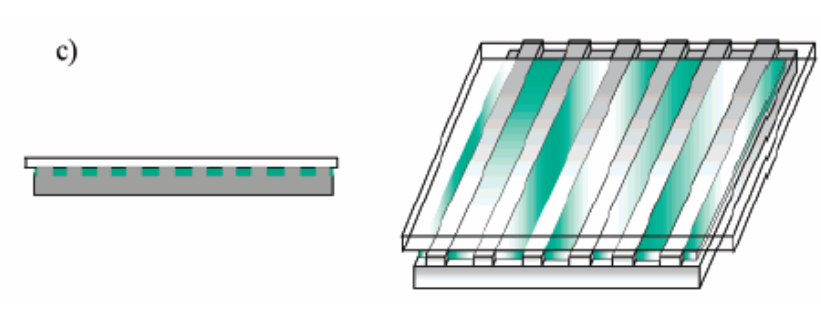
Previous Work

- **50-nm half pitch memory structure by a single layer UV-curable NIL**

- Due to the increased surface to the volume ratio of the imprinted resist, it was unable to make the 30nm half pitch memory structure.
- The easiness of the resist detachment is essential.





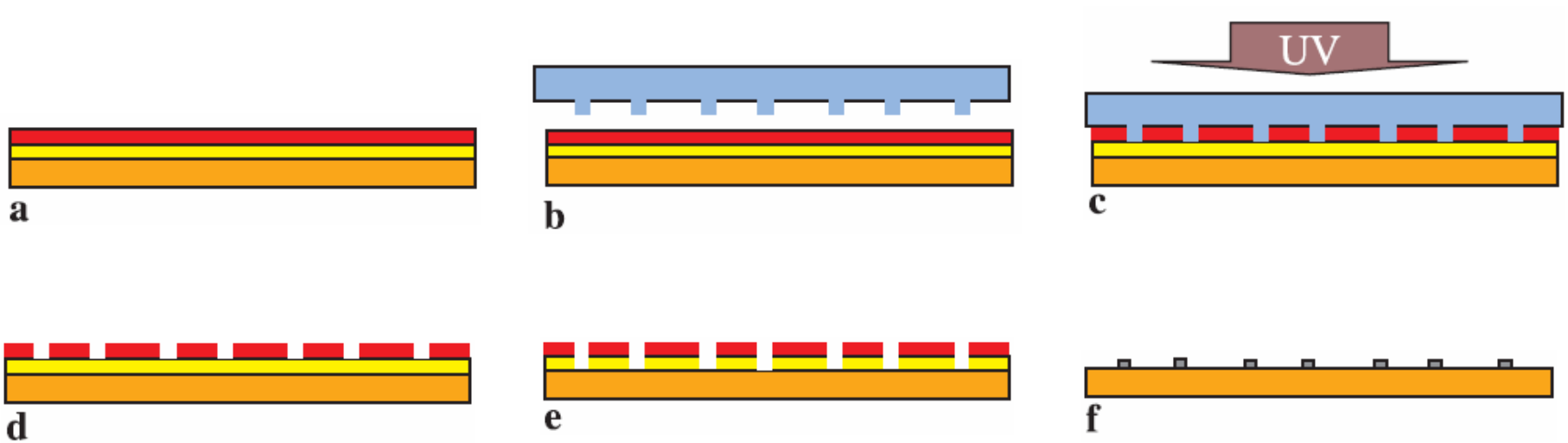


G. Y. Jung, et al. (2004)

- **The requirement for improving mold-resist detachment**
  - Using the resist which has a high mechanical strength
    - The heavily cross-linked resist
  - Trade off between the resist's solubility and cross-linking
    - Lift off vs. pattern size
  - Limitation of the single layer UV-curable NIL process
    - Another method?

UV-curable NIL with double layer

- **The top layer**
  - Structurally robust but not soluble in acetone
  - Making layer for the bottom layer
- **The bottom layer**
  - Soluble in acetone: enabling the lift off process

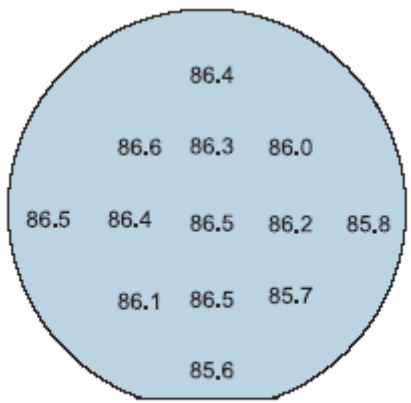


(a) Spin coat the layers (b) Load sample and mold (c) Press and exposure

(d) Separation (e) transfer layer etching (f) metal depo. & lift off

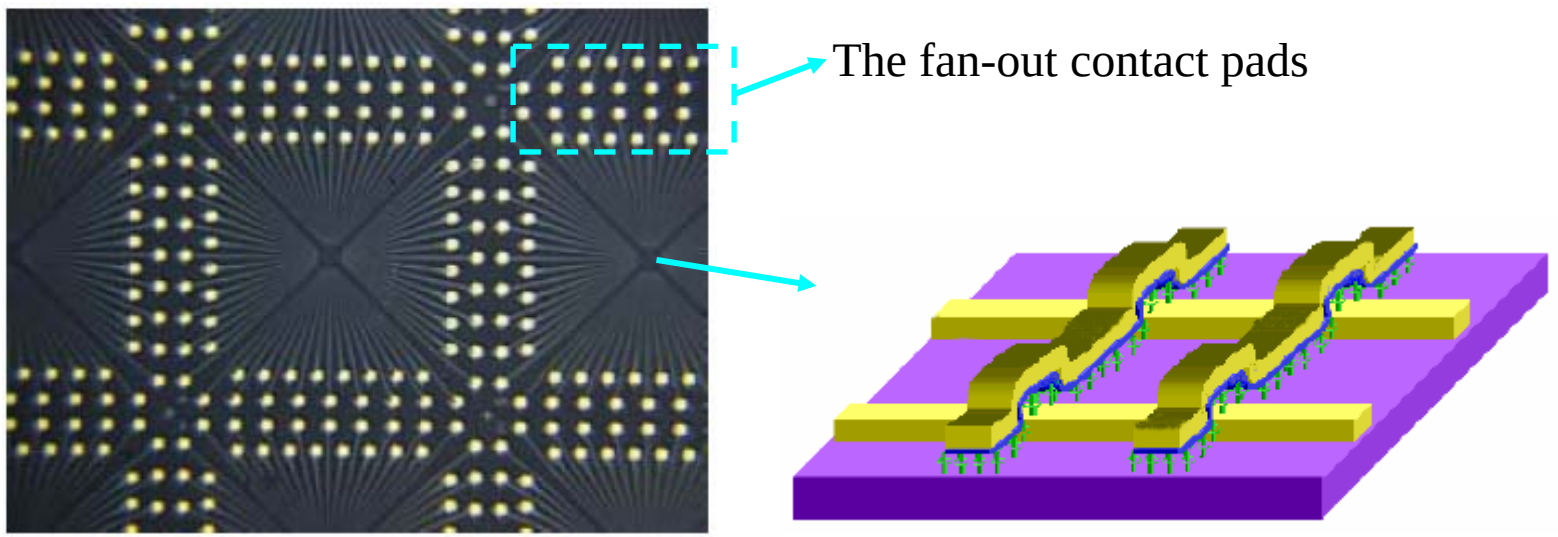
- **The top layer (UV-curable resist): NXR 2010**
  - Heavily cross-linked PR - promotes sturdiness to prevent the nanofeature in the resist from being broken
  - The hydrophobic property - renders the adhesion force between the mold and the imprinted resist

- **The bottom layer**
  - Highly soluble in acetone for the lift off process
  - Exceptional resist thickness uniformity of 1nm 3 sigma



Device Fabrication

- **The device structure**
  - The bottom electrode - the molecular film - the top electrode
    - The bottom and the top electrodes by the UV-curable NIL with double layer



34*34 cross bar memory circuits with 30-nm half pitch

The resist surface wetting property

- **In nano scale regime**
  - Hydrophobic: the solvent cannot easily enter a nanoscale gap
    ⟶ poor lift-off

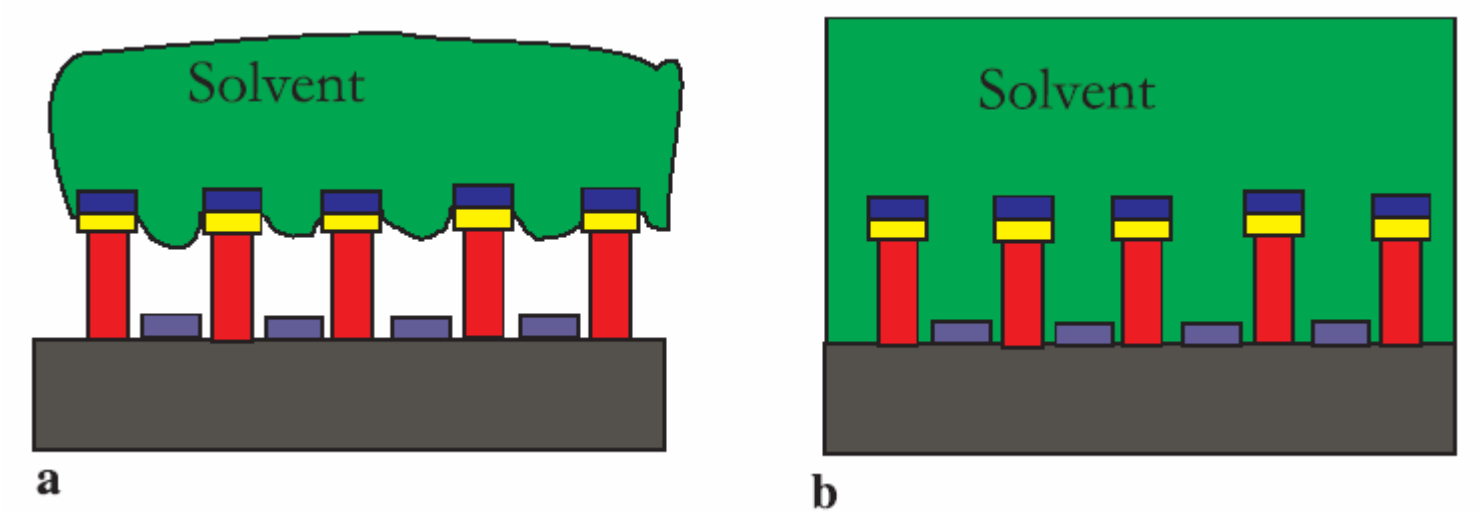
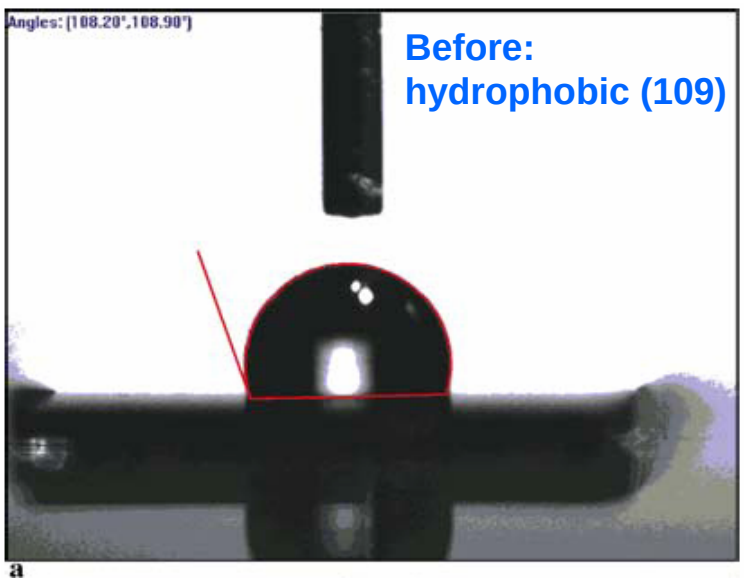
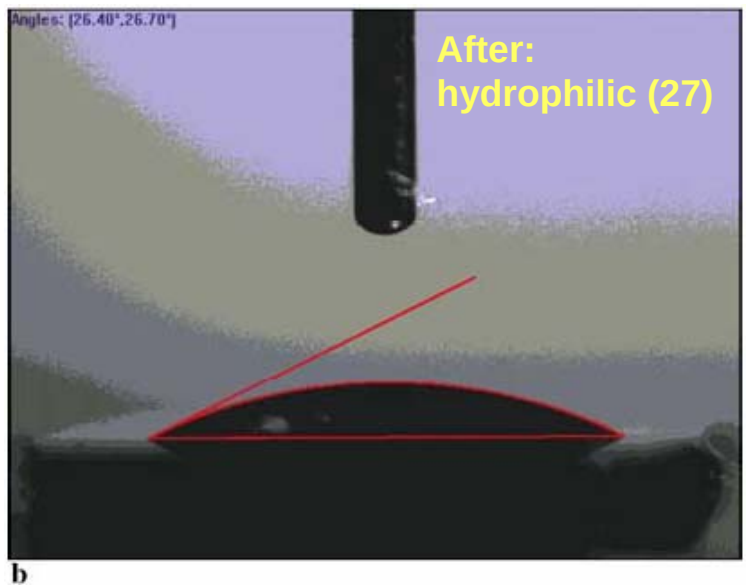


FIGURE 5 Schematic diagram of the resist surface wetting properties' effect on lift-off process. (**a**) When the solvent does not wet the resist surface, the solvent cannot get into a gap smaller than a certain critical dimension. That causes poor lift off. (**b**) The solvent enters into the small gap easily and results in a better lift off if the surface wetting property improved

- **The lift off process: fabricate the electrodes after the layer etching**
- **As feature sizes shrink to the deep nano regime**
  - Surface to volume ratio increases dramatically
    ⟶ changes the surface wetting properties
  - O_2 plasma treatment to the surface improves the wetting property of the resist





- **The result of the lift-off process & the fabricated device**
  - Defects due to the not optimized mold height
  - The taller mold forces to use thinner transfer layer to prevent the aspect ratio of the etched resist structure from being to high

e

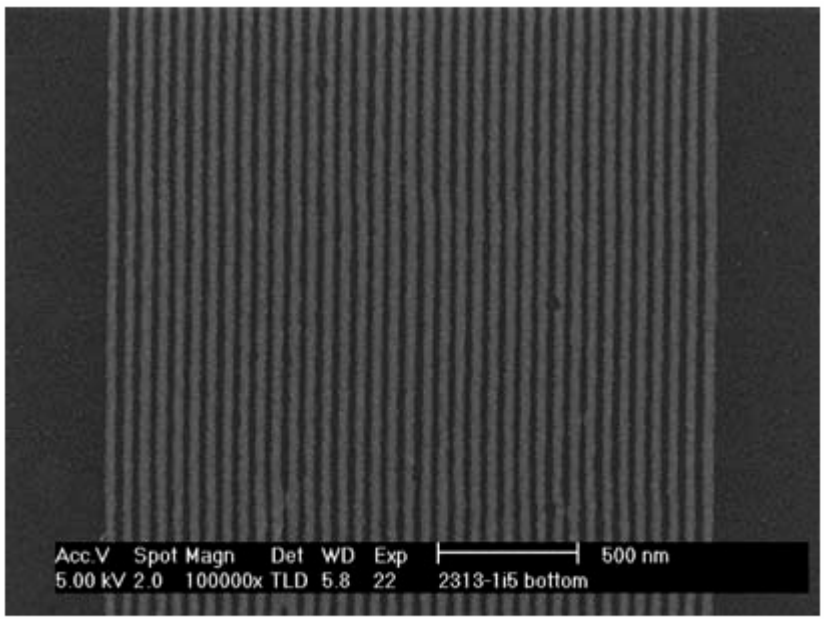


FIGURE 7 Ti/Pt nanowires with 30-nm half-pitch fabricated by nanoimprint lithography and lift off

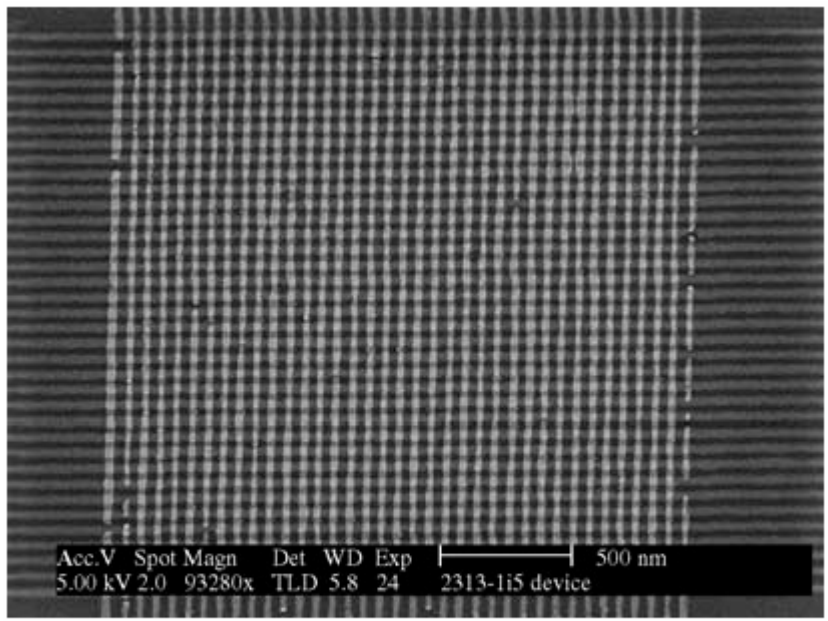


FIGURE 8 SEM image of 34 × 34 cross-bar memory circuit with 30-nm half-pitch fabricated by nanoimprint lithography, lift off and LB film deposition

I-V characteristic of a device

- **The switching loop**

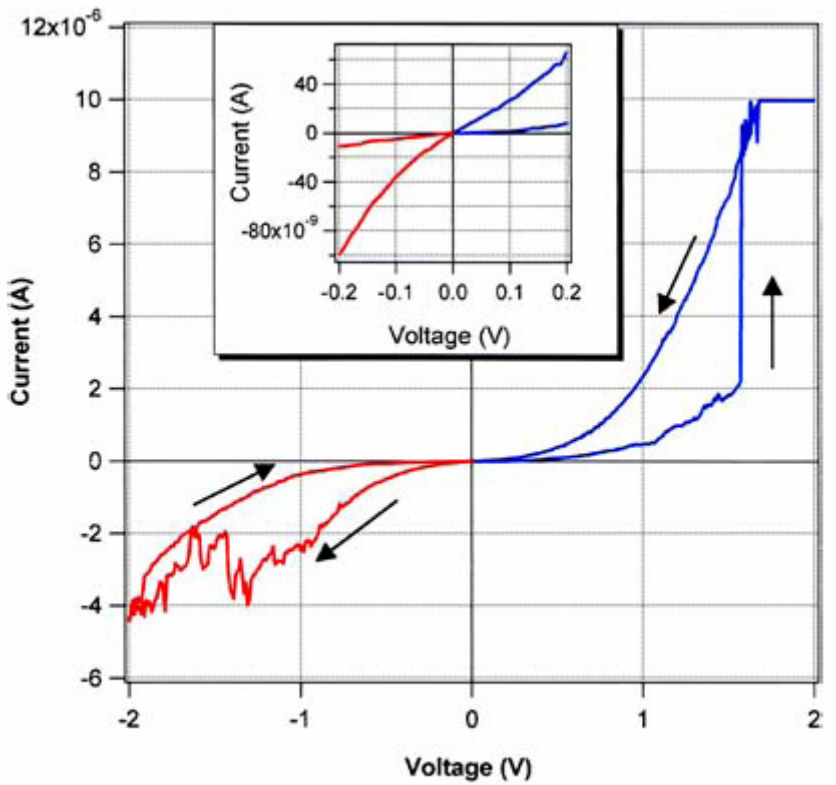
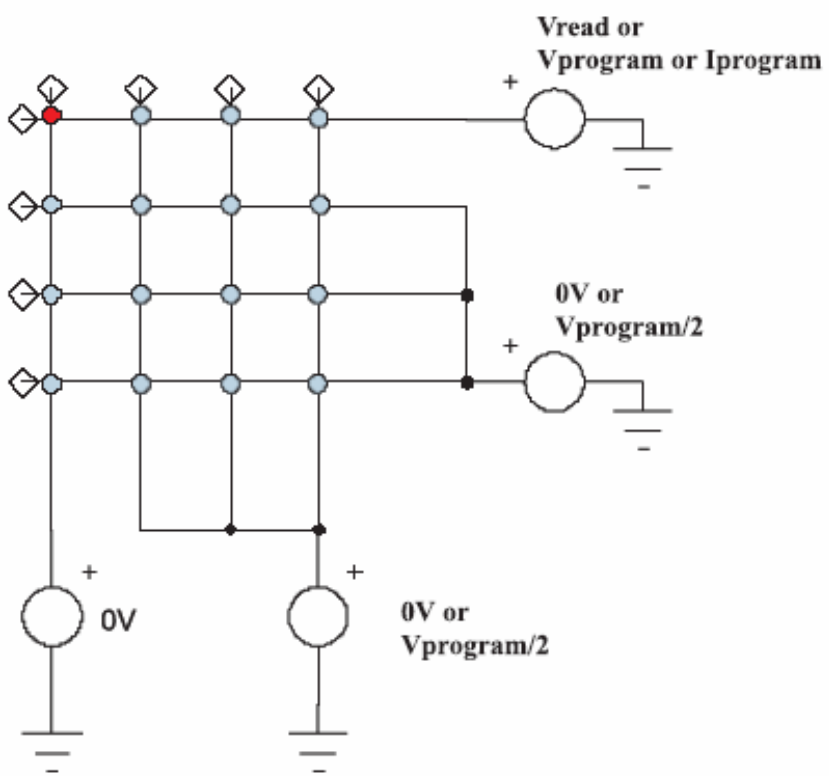


FIGURE 10 Electronic characteristic of a single device measured from an on-chip control device. It shows the switching hysteresis

- V_{th}: ~1.5V
- On/off ratio: ~10

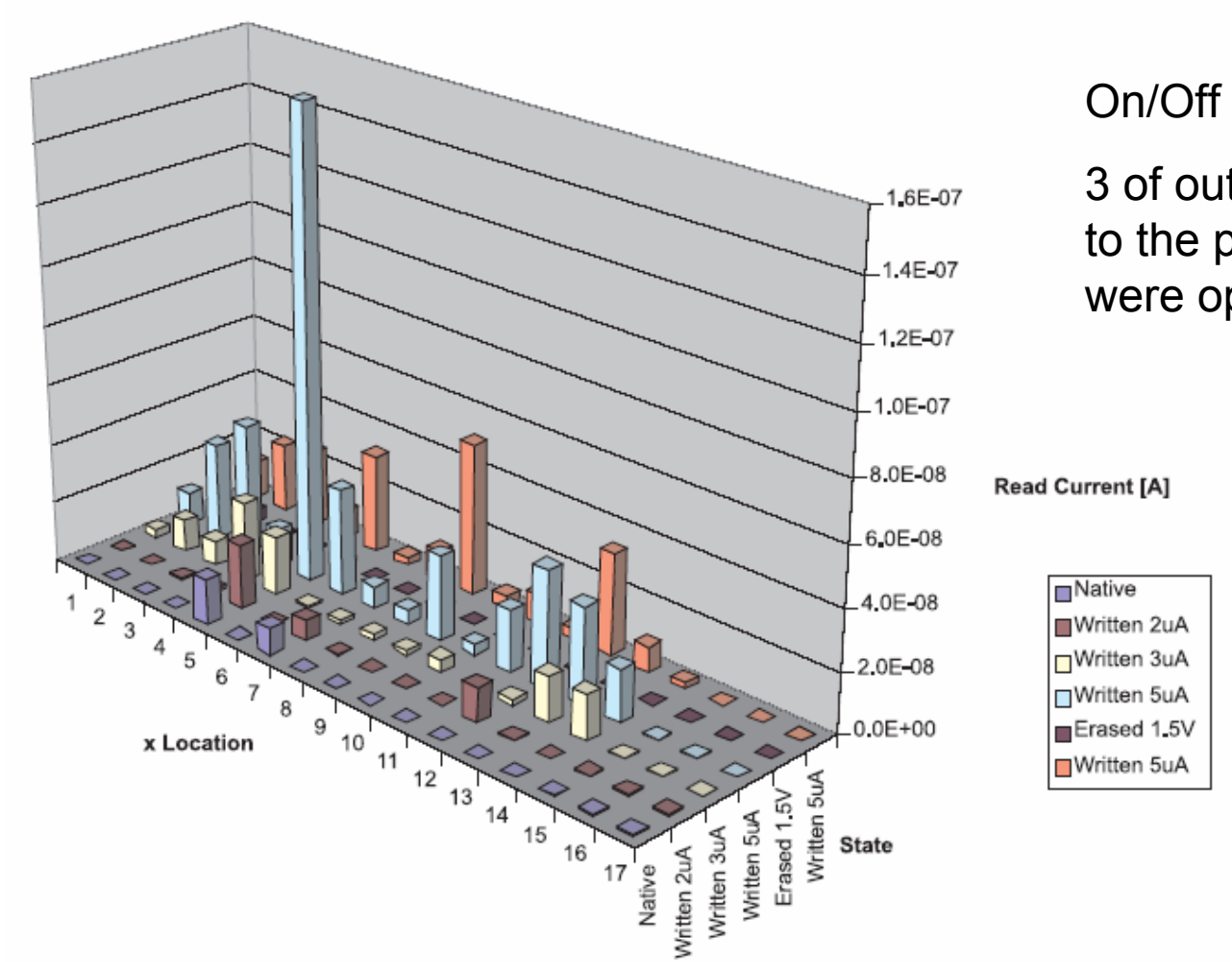
Testing configuration

- Read is done by applying 0.5V to the selected row with all unselected rows and columns at 0V, and reading the current.
- Write is conducted by applying a programming voltage (or current) to the selected row, while maintaining all the unselected rows and columns at one-half of the voltage of the selected row.



Measurement results

- **Read currents of a 1 * 17 cross-bar memory testing at 0.5V**



On/Off ratio: 10~2600

3 of out 17 were broken due to the particles (electrodes were open circuit)

- **In a crossbar structure, the following parameter must be considered**

  l_x, l_y : the horizontal sizes of the cross-point

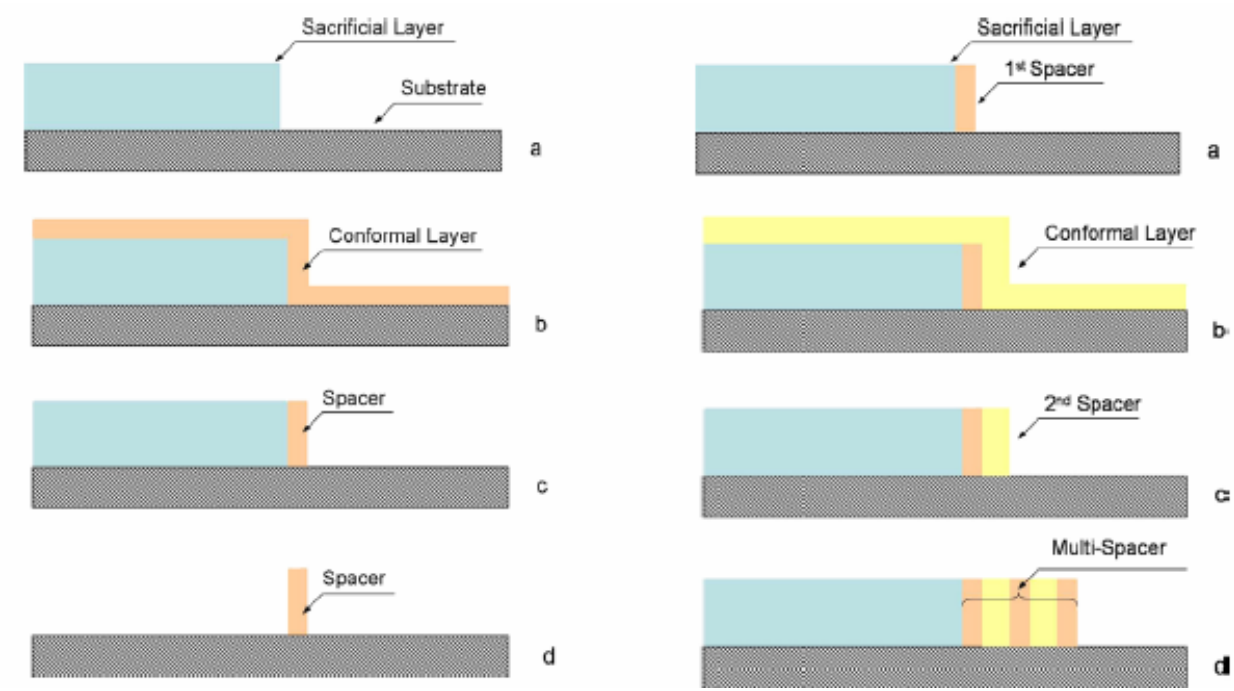
  l_z : the vertical gap between wires

  L_x, L_y : the horizontal pitches

  - In the HP-UCLA collaboration these parameters were controlled by lithography (initially via E-beam lithography, then replaced by imprint method)
  - E-beam lithography produces at best arrays with $L_x \gg 2l_x$

The Spacer patterning technique

- **Transforming vertical features into horizontal features**



G F Cerofolini, et al. Nanotechnology 16 (2005) 1040

The Spacer patterning technique

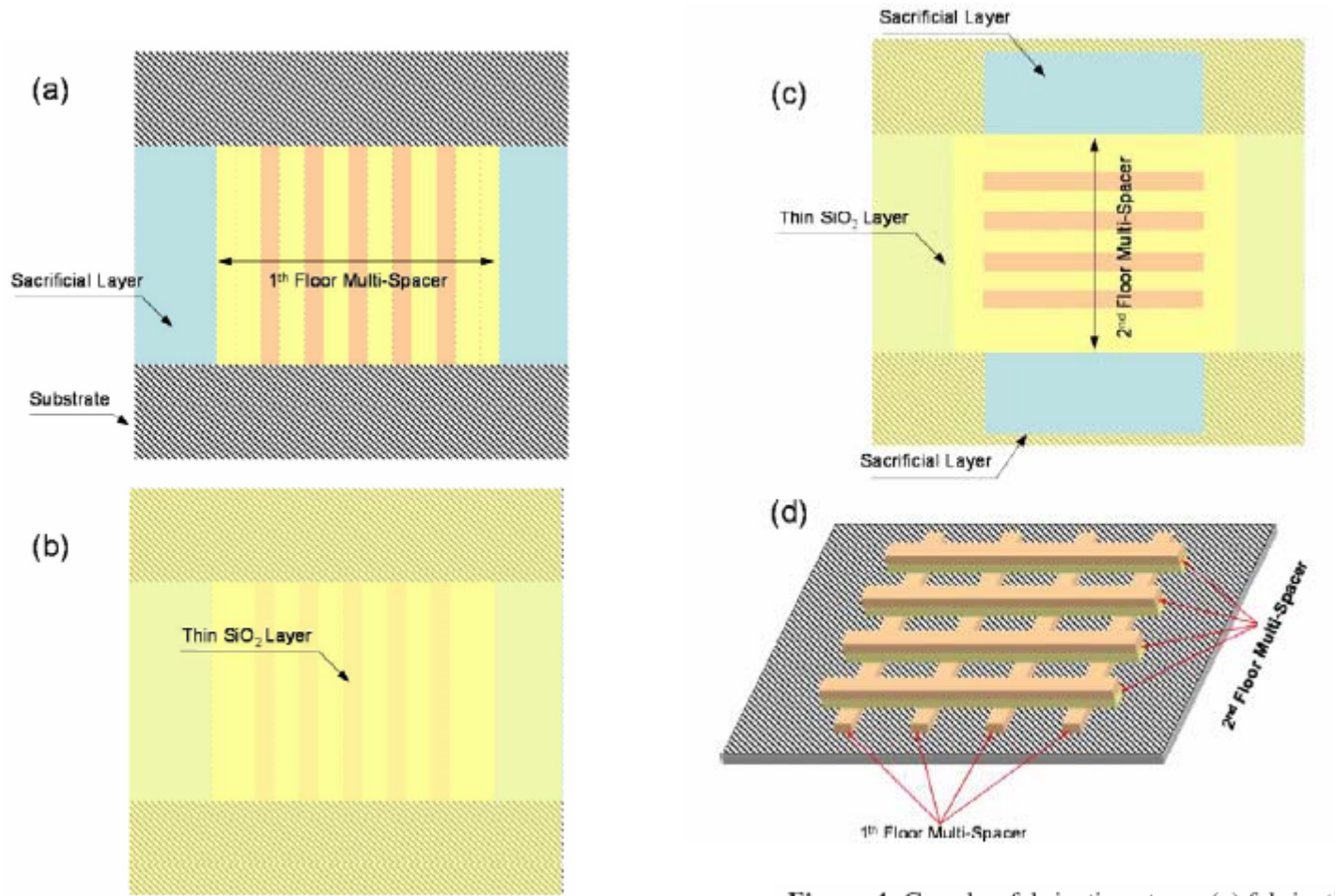


Figure 4. Crossbar fabrication steps: (a) fabrication of a first-floor array of double spacers by means of S^{n}PT; (b) thermal growth of a thin film of SiO_2; (c) fabrication of a second-floor array of double spacers crossing the first-floor array; (d) selective chemical etching of the intralayer SiO_2.

The Spacer patterning technique

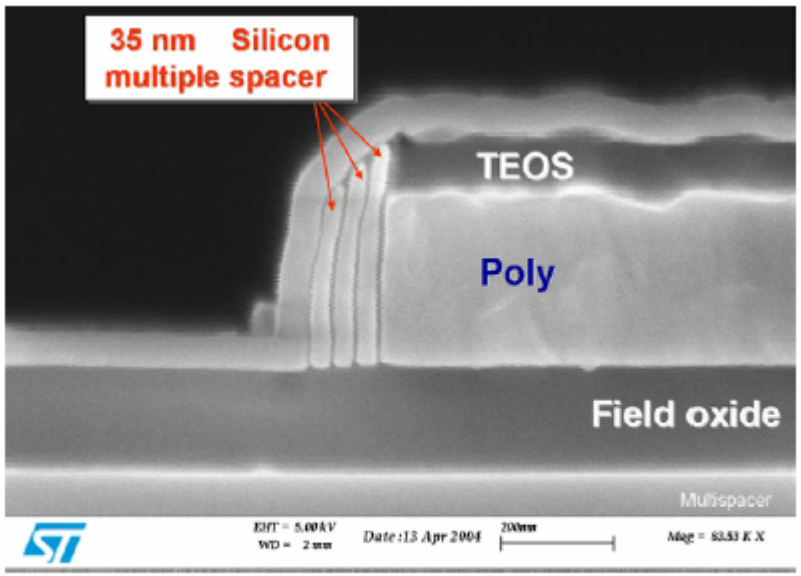


Figure 3. Image from the scanning electron microscope of a cross-section of a structure with three spacers obtained with the S^3PT using undoped polysilicon and thermally grown SiO_2.

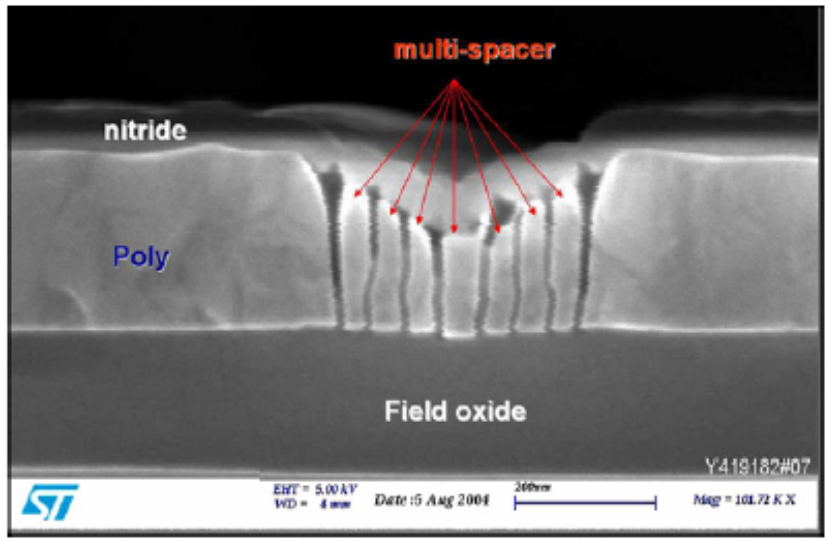


Figure 5. Image from the scanning electron microscope of the cross-sections of a seven-spacer crossbar structure obtained with the S^nPT using undoped polysilicon and thermally grown SiO_2.

Summary

- **Crossbar memory circuits with 30nm half pitch is fabricated by NIL**
- **In nano regime the wetting properties of the PR is important**
  - Hydrophobic property can be changed into hydrophilic by o_2 plasma treatment: enhances lift-off process
- **Another approach (spacer technique) is shown**

The path for the Nano-electronics?

Sung Hyun Jo

Ph.D. Student, Dept. of Electrical Engineering & Computer Science

Ken Loh

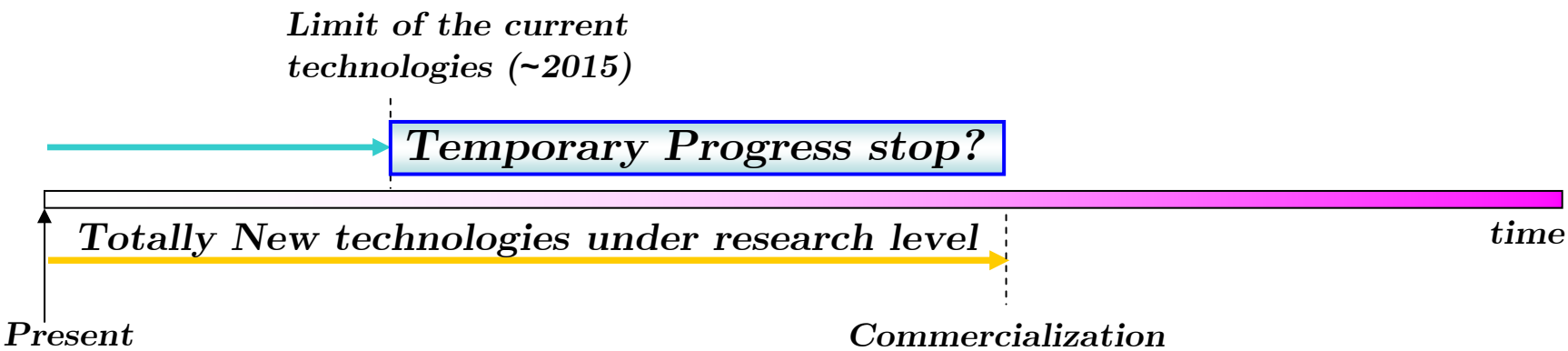
Ph.D. Student, Dept. of Civil & Environmental Engineering

EECS 598 Nanoelectronics Week 12 Presentation
Ann Arbor, MI

November 29, 2005

Background

- **The length of the smallest device feature is shrunk to nearly the molecular size**
- **Innovations will be required to reach the limit of the Si transistor (~10nm)**
- **For further shrinking of the size of the device, alternative technologies are required**



Alternatives to Si-Based CMOS

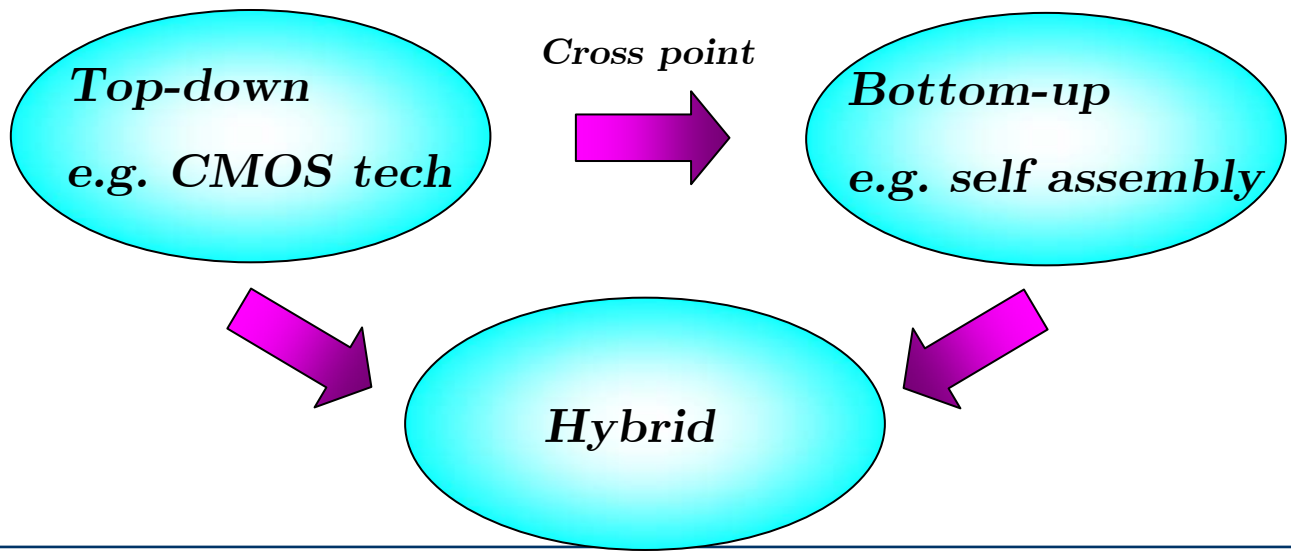
- **Single Electron Transistors**
- **Quantum Cellular Automata**
- **Neural Networks**
- **Molecular Logic Devices**

Push to fabricate the device on the nanoscale length

- **Even atomic-scale irregularities impose significant variations on the size of nano-devices**
  - Destruction of the device's electrical properties
  - Some sizable fraction of the tiny devices will not work
- **In reality, totally defect free devices are not feasible**
- **Deep nanoregime electronics is impossible?**

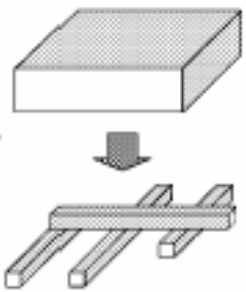
Top-down vs. Bottom-up

- **Top-down approach**
  - The cost of the fabrication plant for Ics is escalating exponentially with time. (Moore s second law)
  - Reliable structure
  - Relatively perfect device
- **Bottom-up approach**
  - The sophistication of inexpensive chemically synthesized component is increasing dramatically



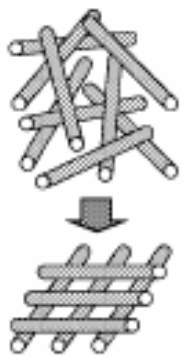
Top-Down Fabrication

- e.g., Lithography
- Limited resolution
- Expensive
- Arbitrary structures
- Reliable



Bottom-Up Assembly

- e.g., Self-Assembly
- Molecular resolution
- Potentially cheap
- Limited to regular or random structures
- Higher Defect Rates



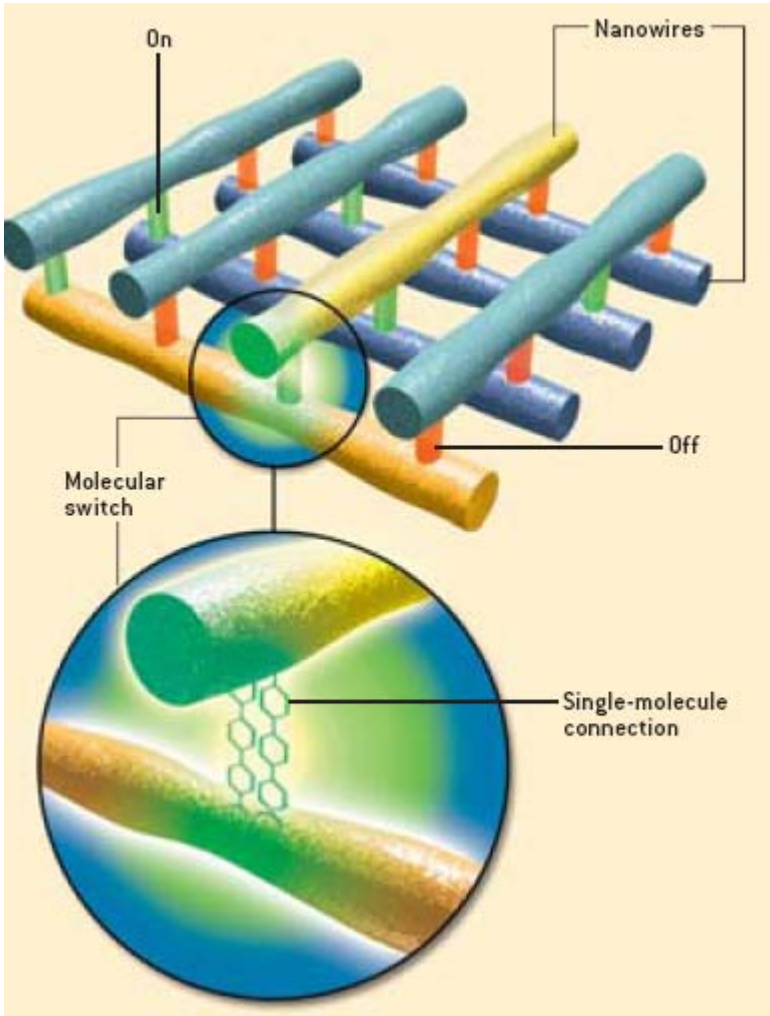
A Hybrid approach to nanodevices

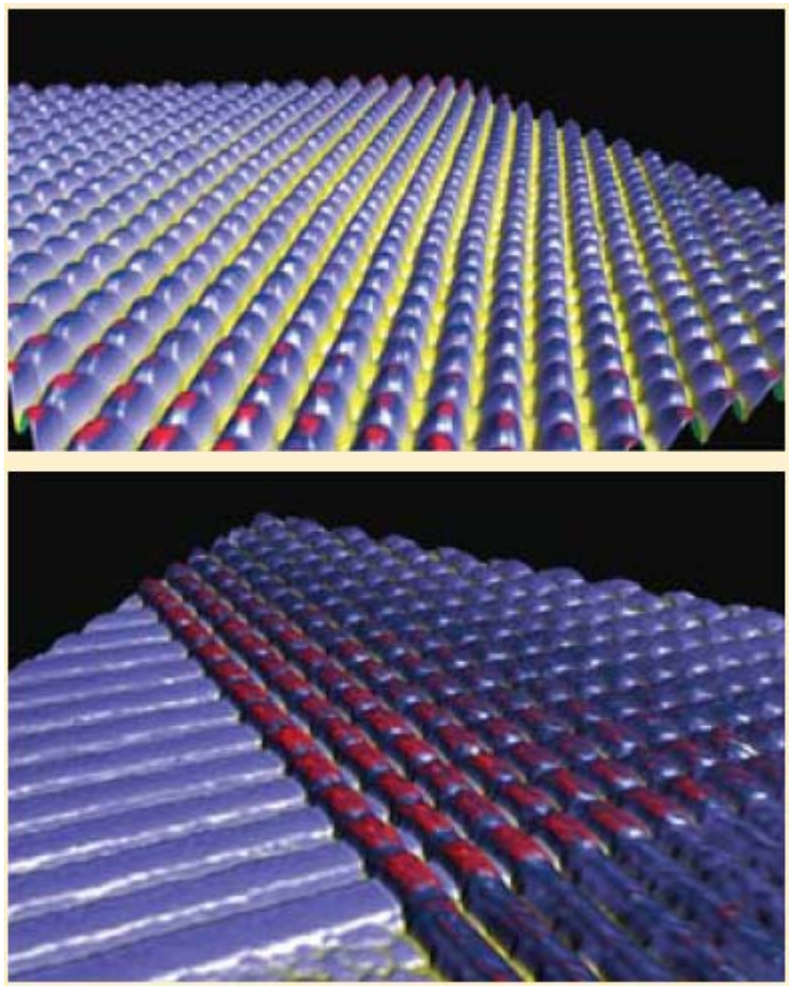
- **Motive**
  - The architecture of the IC is mostly controlled by the microelectronic part
  - It will be very difficult for any new technology to compete head-to-head with silicon's large scale fabrication infrastructure, proven design methodologies, and economic predictability
  - Peaceful coexistence between conventional silicon electronics and nanoelectronics
  - The hybrid method is a more viable path toward the initial nanoscale systems

Crossbar structure

- **One of the most likely path forward**
- **Advantages**
  - Very simple structure
  - Array-like composition
  - Flexibility in adapting existing designs to new materials
  - Versatile application: memory, logic and interconnection
  - Within the same entity, both devices and logics are possible
  - Two terminal structure: enabling the aggressive scaling down
  - N wires to control 2^N devices
  - Possibility of defect tolerant architecture

The crossbar architecture

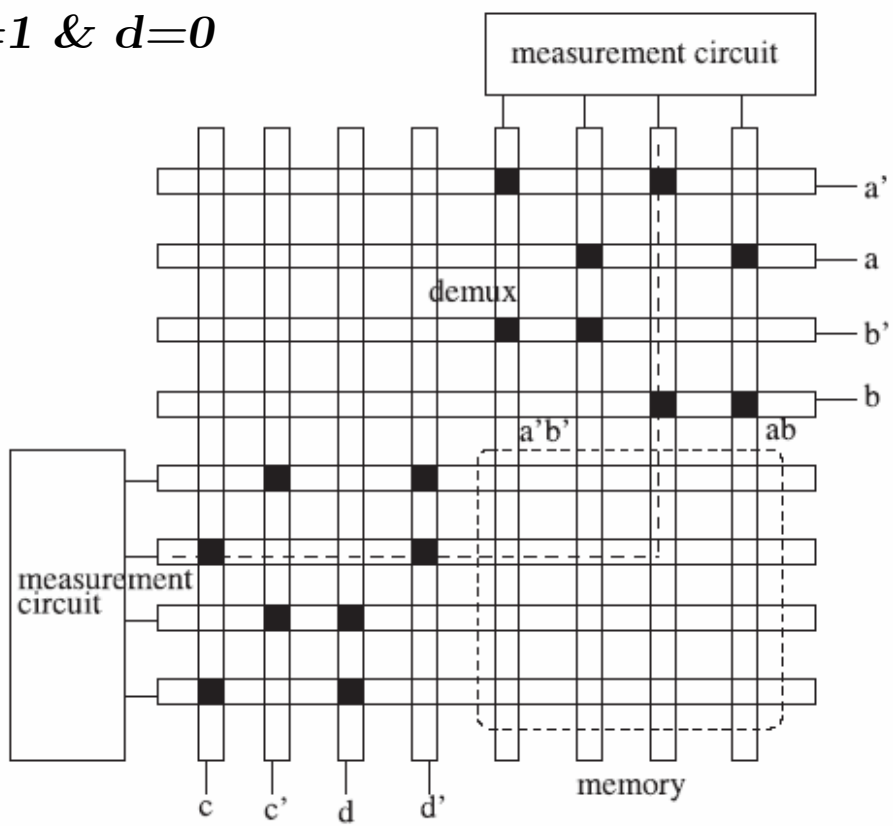




The crossbar memory

- **The crossbar memory architecture**
  - If there are some defects in the crossbar, a memory of the required size cannot be configured without using spares.

$a=0,\ b=1,\ c=1\ \&\ d=0$



Defect-tolerant architecture

- **In a molecular-based memory the defect rate is expected to high compared to the CMOS technology.**
- **Spare lines are required to correct the errors.**
  - How many lines are required? & how effectively it works?

crossbar memory : $2^n \times 2^n$

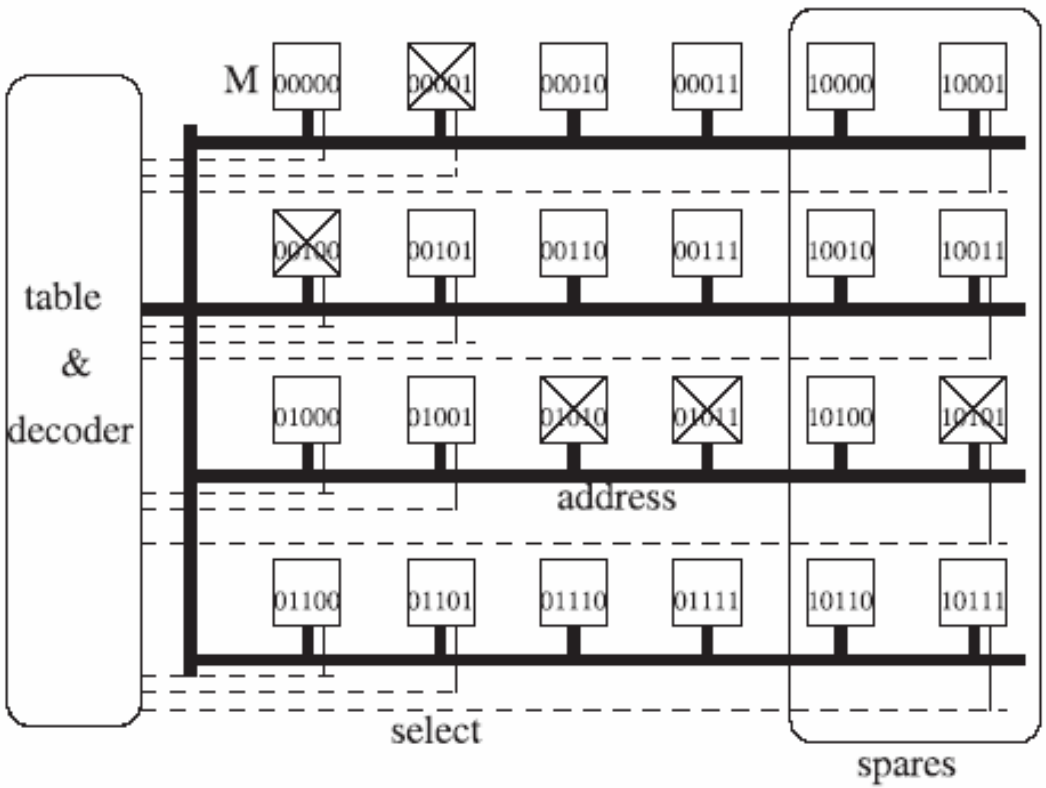
with redundancy lines : $(2^n + 2^r) \times (2^n + 2^r)$, defect rate: 0.001 and 0.002

	r								
n	3	4	5	6	7	8	9	10	11
6	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
7	0.54	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
8	0.00	0.00	0.54	1.00	1.00	1.00	1.00	1.00	1.00
9	0.00	0.00	0.00	0.00	0.00	1.00	1.00	1.00	1.00
10	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.00
6	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
7	0.00	0.46	1.00	1.00	1.00	1.00	1.00	1.00	1.00
8	0.00	0.00	0.00	0.00	0.99	1.00	1.00	1.00	1.00
9	0.00	0.00	0.00	0.00	0.00	0.00	0.00	1.00	1.00
10	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Configurability of crossbar memory with spares

Defect-tolerant architecture

- **Redundancy at module level**
  - About 22% of the crossbar area is enough for the redundancy (2^9* 2^9 memory case)



Yoon-Hwa Choi, et al. Nanotechnology 15 (2004), 639

Summary

- **For continuous extension of the Moor's law, device electronics paradigm need to be changed.**
  - Pursuing perfection ⟶ somewhat defective but defect tolerant
  - The hybrid method is a viable path toward the initial nanoscale systems
  - The crossbar structure is the one of the most likely path toward