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One-kilobit cross-bar molecular memory circuits at 30-nm half-pitch fabricated by nanoimprint lithography

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ABSTRACT We have developed a process to fabricate a cross-bar structure using UV-curable nanoimprint lithography with a UV-curable double-layer spin-on resist, metal lift off and Langmuir–Blodgett film deposition. This process allowed us to produce 1-kbit cross-bar memory circuits at 30-nm half-pitch on both top and bottom electrodes. Read, write, erase and cross talking were also investigated.

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Molecular electronics offers the prospect of scaling device dimensions down to a few nanometers, which is not possible for Si-based devices. However, the density of circuits with molecular components is still limited by the lithography used in electrode and connection fabrication. For practical reasons, not only high resolution but also low cost and high throughput are required for lithography geared for manufacturing. However, today's production tools do not yet have the resolution to produce 30-nm half-pitch structures. Nanoimprint lithography (NIL) [1–4] offers a cost-effective alternative for high-resolution patterning. Previously, our group has reported fabricating a cross-bar memory circuit of 64 bits at a density of 5.9 Gbits/cm^2 and 1 kbits at a density of 10 Gbits/cm^2 by NIL [5, 6]. Here, we report the fabrication of a 1-kbit cross-bar molecular memory at an unprecedented density of 28 Gbits/cm^2 (30-nm half-pitch).

A single-layer UV-curable NIL process was used to fabricate our 50-nm half-pitch memory structure [7]. We were unable to extend this process when the half-pitch shrank to 30 nm mainly because the increased surface-to-volume ratio of the imprinted resist caused the resist to adhere to the mold during mold detachment, even though the mold had been treated with a releasing agent [8]. Thus, one requirement for improving mold–resist detachment is for the as-cured resist to have a higher mechanical strength, which is satisfied by a heavily cross-linked resist. However, the cross-linking will reduce the resist's solubility, which is important for lift off. These two conflicting requirements ultimately limit the resolution of the single-layer UV-curable NIL process.

To pursue 30-nm half-pitch and higher-density structures, we developed a process using UV-curable NIL with double-layer spin-on resists [3, 9]. The top layer, which is structurally robust but not soluble in acetone, will be directly patterned during the imprinting. It serves as the imaging layer (mask) for the pattern to be transferred by reactive ion etching (RIE) to the bottom transfer layer, which is soluble in acetone.

The NIL process of electrode fabrication is depicted in Fig. 1. We employed a bi-layer resist consisting of PMMA with good lift-off properties as the bottom transfer layer and a liquid nanoimprint resist (Nanonex NXR 2010) as the top imaging layer. Both were spin coated in sequence onto the substrate. The sample and the nanoimprint mold, fabricated by electron-beam lithography (EBL) at Lawrence-Berkeley National Lab (LBNL), were loaded into a purpose-built UV-capable NIL tool. After the air between the mold and the sample was pumped out, the mold and the sample were pressed at a calibrated pressure and the resist was cured with UV radiation. The sample and the mold were then unloaded from the NIL machine and separated. After the resist residue layer and the transfer layer were etched in succession by anisotropic

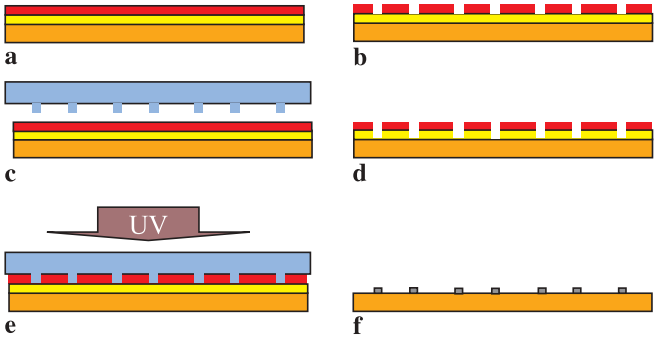

FIGURE 1 Schematic diagram of the electrode fabrication by UV-curable double-layer NIL. (**a**) Prepare substrate, spin transfer layer and liquid resist. (**b**) Align and load sample and mold. (**c**) Press and expose. (**d**) Mold and substrate separation. (**e**) Resist residue layer and transfer layer etching. (**f**) Metal deposition and lift off

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cryogenic RIE, 4-nm Ti and 6-nm Pt were evaporated with an e-beam evaporator. Finally, the sample was bathed in warm acetone to lift off the resist, forming the nanoscale electrode and fan-out connections.

After the bottom-electrode fabrication, a stearic acid molecular film was deposited by the Langmuir–Blodgett (LB) method. A 10-nm blanket Ti layer was then evaporated onto the LB film to protect it from damage during top-electrode fabrication [10].

After both transfer layer and resist layer were spun onto the sample, the patterns on the mold were then aligned at right angles with those on the sample by a contact aligner, which pre-pressed them and caused them to hold tightly together. The attached mold and sample were then transferred into the NIL machine for the same double-layer process as for fabricating the bottom electrodes. The top electrodes then served as the etch mask to etch the blanket Ti protection layer. Finally, the fan-out contact pads, which consist of 100-nm Ti and 300-nm Au, were evaporated through a shadow mask and the circuit fabrication was finished (Fig. 2).

The UV-curable NIL resist (Nanonex NXR 2010) used in our process was heavily cross-linked during the curing process to make it mechanically strong. It is so strong that it is even strong enough to be used as an imprint mold for both thermally and UV-curable imprint in defining parallel lines with half-pitch down to 30 nm [11]. Another advantage is that the surface of the cured resist is hydrophobic (with a water-contact angle of 109°), which rendered the adhesion force between the mold and the imprinted resist low. These two properties were critical in patterning dense nanoscale features, because the former promotes sturdiness to prevent the

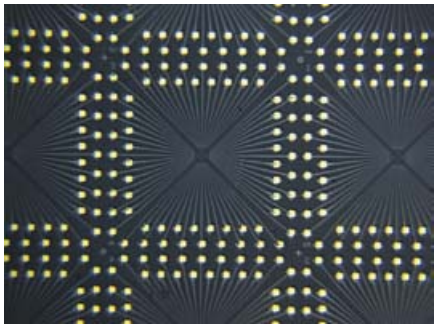


FIGURE 2 Optical micrograph of fabricated 34×34 cross-bar memory circuits with 30-nm half-pitch, showing the fan out from the nanowires and the contact pads (each die is 2.5 nm across)

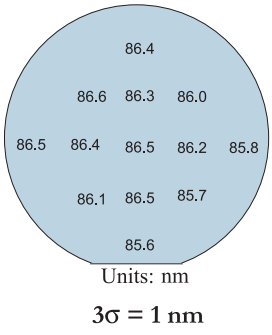


FIGURE 3 Thickness distribution of spin-coated UV-curable imprint resist. It had an exceptional resist thickness uniformity of < 9 Å 3σ over a $4''$ wafer

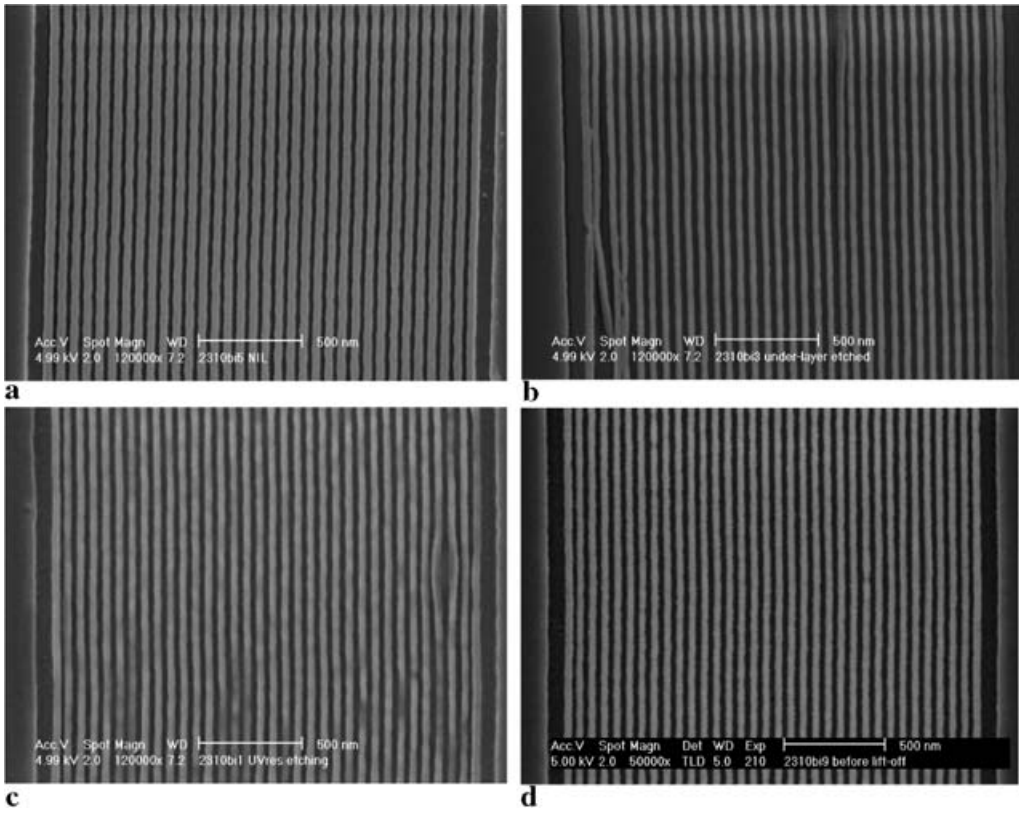


FIGURE 4 (**a**) SEM image of resist as imprinted; (**b**) SEM image of the resist with residue layer etched with CHF_3/O_2, which causes greater CD (critical dimension) loss. Thus RIE without O_2 gas is preferred; (**c**) SEM image of the resist with residue layer and transfer layer etched. The residue layer was etched without O_2 and the transfer layer was etched at $-120\,^{\circ}C$, but the resist structure still collapses if the transfer layer is too thick; (**d**) SEM image of the resist structure with residual layer etched without O_2 and with a thinner transfer layer. The resist structure did not collapse

nanofeature in the resist from being broken and the later reduces the tendency for the resist to adhere to the mold.

Because the top imaging layer is heavily cross-linked, the bottom transfer layer must be highly soluble in acetone for the lift off to occur. The use of a bottom layer also serves to planarize the surface and distribute the imprint pressure homogeneously for the imprint to occur on the top layer. This is particularly important to our devices because the non-uniform surface caused by the bottom electrodes may lead to damage to the molecular layer during the top-electrode imprinting. Finally, a controlled etching undercut of the transfer layer can prevent side-wall deposition that could have produced metal protrusions short-circuiting the junctions.

As with all other aspects of nanoscale pattern generation, pattern transfer from the imaging layer to the substrate becomes increasingly challenging as feature size scales down. The 'over-etching budget' becomes tight, because thinner resists are normally needed for smaller features and there is a more severe micro-loading effect in RIE etching [12]. Hence, a uniform resist coating and a high etching selectivity between the imprint resist and the transfer layer are preferred. Furthermore, much better critical dimension control is required for RIE. The two challenges were met by a multi-step process. We applied the resist by spin coating, and were able to achieve exceptional resist thickness uniformity of 1 nm 3σ (Fig. 3) for average thicknesses ranging from a few dozen to 200 nm. Moreover, the etch selectivity between the transfer and imaging layers is higher than 10, giving us a comfortable margin in over-etching. We found that the use of both CHF_3 and O_2 to etch the imaging layer would lead to a much higher critical dimension loss compared with the original as-imprinted imaging layer (Fig. 4a, b). The likely cause of this is that in the absence of O_2, the etch product formed a passivation layer on the side wall and prevented lateral etching. Therefore, we used pure CHF_3 gas at a pressure of 0.1 mTorr to etch the residual layer for the imaging layer. For the bottom transfer layer, it is important that it is thin, as the nanowire resist/transfer layer structure may collapse if the aspect ratio is high (Fig. 4c). We employed a transfer layer with a thickness of less than 40 nm and obtained good results (Fig. 4d). The RIE was carried out with O_2 at $-120\,^{\circ}C$ in order to control the undercut.

A lift-off process was used to fabricate the electrodes after transfer layer etching. As feature sizes shrink to the deep nano regime, especially as the gap between neighboring wires decreases to less than 50 nm, surface to volume ratio increases dramatically, which changes the surface wetting properties. During the development of our process, we discovered that one of the impediments of a successful lift off is the wetting property of the resist surface, which is still hydrophobic; the solvent cannot easily enter a nanoscale gap smaller than ~ 100 nm (Fig. 5a), causing poor lift off. We solved this problem by using O_2 plasma to treat the surface to improve the wetting property of the resist (Fig. 6). After the plasma treatment, the wetting property improved (water-contact angle 27°) and the solvent entered the small gap easily (Fig. 5b), resulting in good lift off (Fig. 7).

Several 1-kbit memory circuits at 30-nm half-pitch were fabricated. As shown in Fig. 8, there are some visible de-

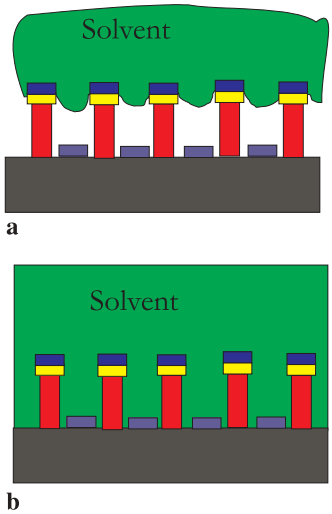


FIGURE 5 Schematic diagram of the resist surface wetting properties' effect on lift-off process. (**a**) When the solvent does not wet the resist surface, the solvent cannot get into a gap smaller than a certain critical dimension. That causes poor lift off. (**b**) The solvent enters into the small gap easily and results in a better lift off if the surface wetting property improved

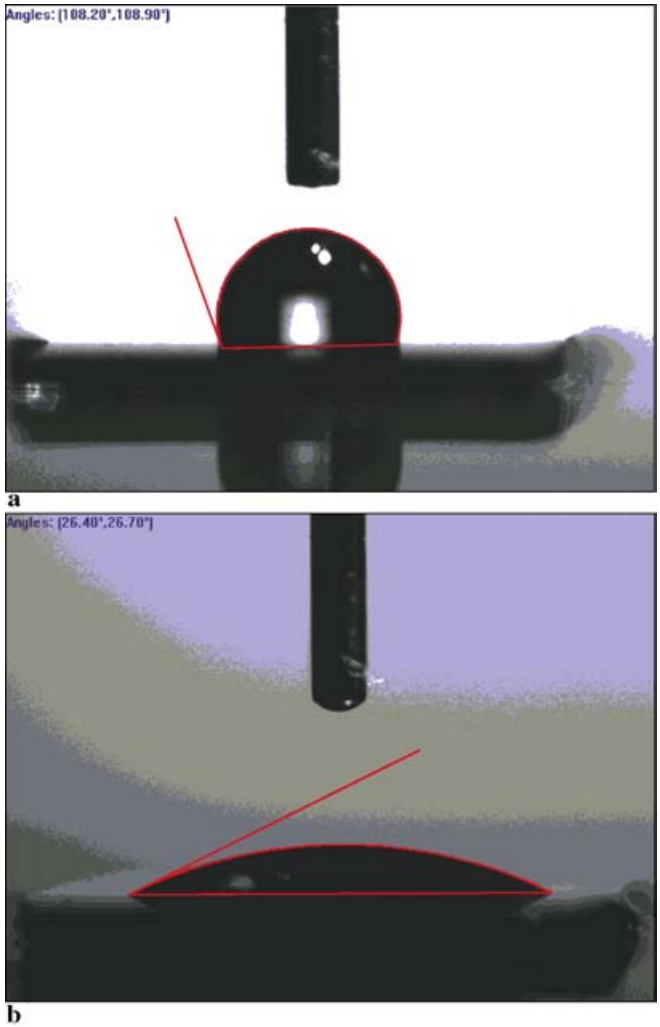


FIGURE 6 Water contact angle measurements show that the imprinted and cured resist surface changed from (**a**) hydrophobic (contact angle of 109°) to (**b**) hydrophilic (contact angle of 27°) after 20 s O_2 plasma treatment

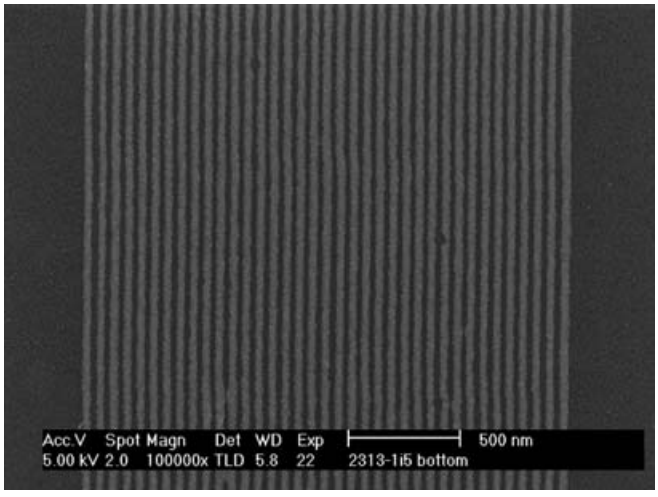


FIGURE 7 Ti/Pt nanowires with 30-nm half-pitch fabricated by nanoimprint lithography and lift off

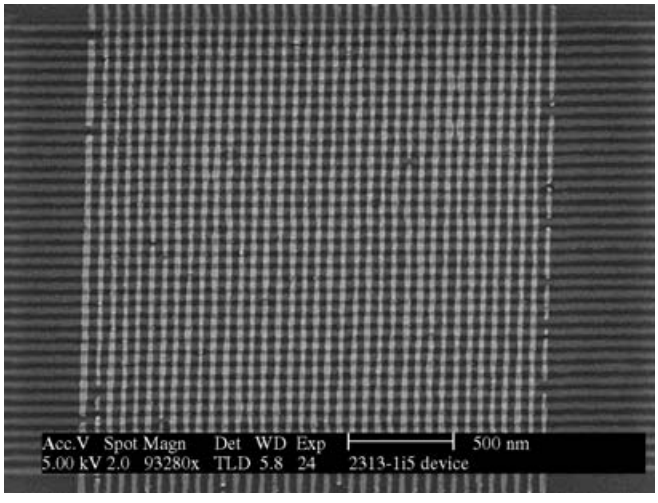


FIGURE 8 SEM image of 34×34 cross-bar memory circuit with 30-nm half-pitch fabricated by nanoimprint lithography, lift off and LB film deposition

fects, especially on the top electrodes. We believe we were mainly limited by our mold height: we initially estimated that a mold height of 75 nm was needed, but we later discovered that a mold height of 35 nm was optimal for our process. The taller height was detrimental because it forced us to use a thinner transfer layer to prevent the aspect ratio of the etched resist structure from being too high. The thinner transfer layer limited the planarization ability of the transfer layer and made the lift-off process more prone to defects, especially for the top electrodes due to the topography underneath.

We also fabricated 1×17 arrays (Fig. 9) on the same chip as control devices; each device in the array has dimensions similar to the device inside the 34×34 arrays (30 nm $\times$ 40 nm). These control devices were used to characterize each individual device without the effect of cross talking.

Figure 10 shows the current–voltage characteristic of a single device. It shows the switching loop. The device switched on by applying positive bias on the top electrode and switched off by negative bias. The threshold of this device is about 1.5 V and the ON/OFF ratio is about 10.

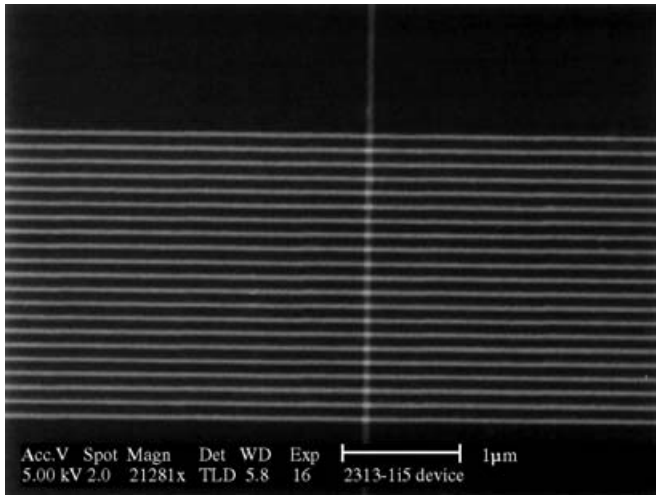


FIGURE 9 SEM image of 1×17 cross-bar memory testing array fabricated by nanoimprint lithography, lift off and LB film deposition

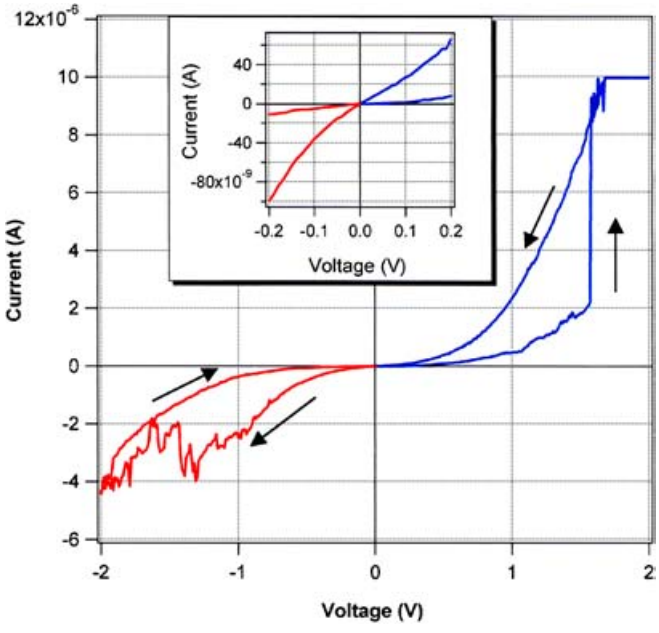


FIGURE 10 Electronic characteristic of a single device measured from an on-chip control device. It shows the switching hysteresis

The electrical measurements of arrays were made with an Agilent 4156c semiconductor parameter analyzer and a Keithley 707 switching matrix as off-chip MUX/DEMUX. Figure 11 shows the configuration scheme (for simplicity showing a 4×4 array). A specific location is read by applying 0.5 V to the selected row with all unselected rows and columns at 0 V, and reading the current in the associated column. A specific location is written by applying a programming voltage or current to the selected row, while maintaining all the unselected rows and columns at one-half of the voltage of the selected row. In our case, we have used current to write a location and voltage to erase a location.

The measurement results of a 1×17 array are shown in Fig. 12. The chart represents the read response (current at 0.5 V) of all 17 junctions after the following stimuli: native, 2 µA write pulse, 3 µA write pulse, 5 µA write pulse, 1.5 V erase pulse and 5 µA write pulse. 14 of out 17 de-

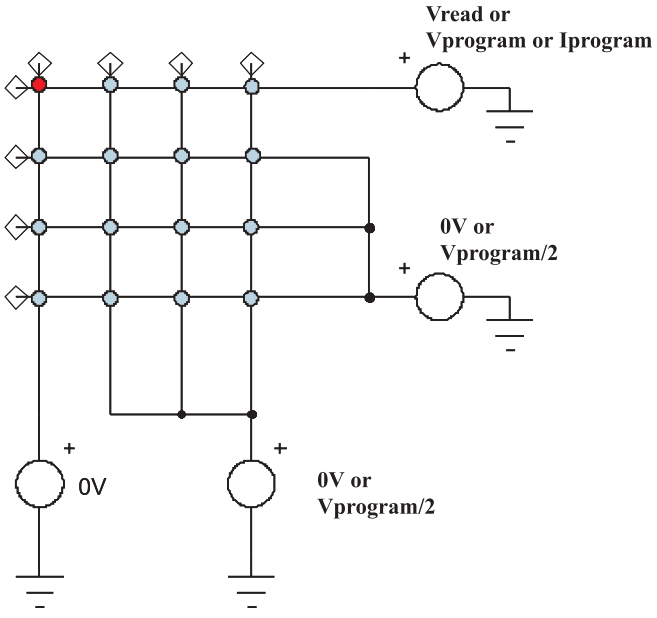


FIGURE 11 Testing configuration for circuits

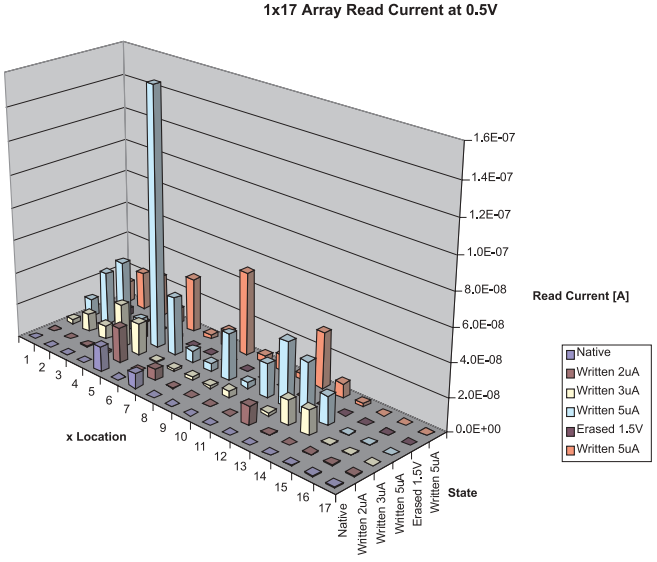
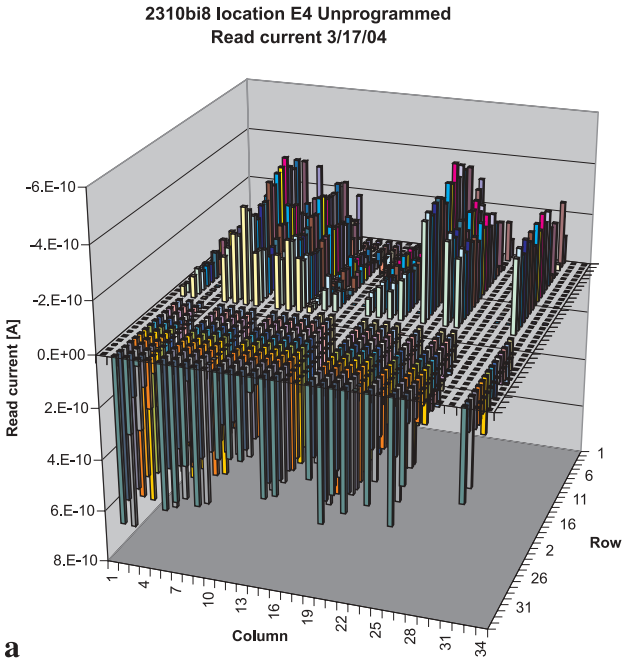


FIGURE 12 Read currents of a 1×17 cross-bar memory testing array at 0.5 V after the following stimuli: native, 2 μA write pulse, 3 μA write pulse, 5 μA write pulse, 1.5 V erase pulse and 5 μA write pulse. 14 out of 17 devices could be read, written and erased



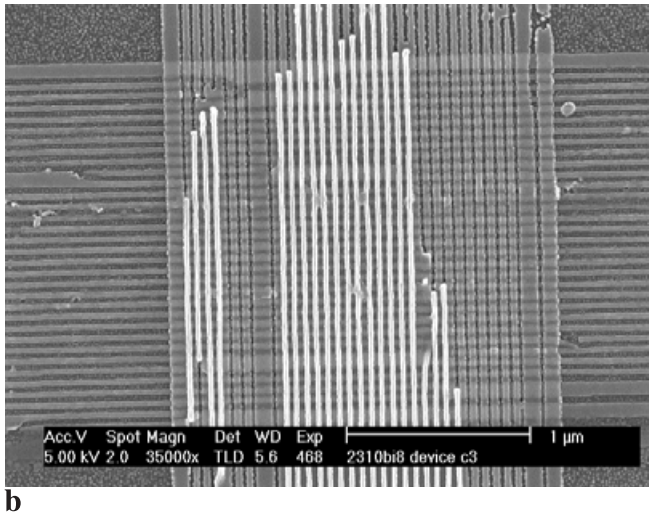


FIGURE 13 (**a**) Read currents of a 34×34 cross-bar memory array at 0.5 V. A large portion of the devices show wrong current direction (downward). That indicated that there was cross talking existing. (**b**) SEM image of the measured array. The region with unsuccessfully lifted-off top electrode matched the area with wrong current direction. The upper layer metal left from the lift-off process shorted the top electrode and caused cross talking

vices showed switching behavior and the ratios between the written state and the erased state were between 10 to 2600. Under the microscope we found the top electrodes of device nos. 15, 16 and 17 were broken due to a particle. That explained why these three devices were open circuit.

The 34×34 circuits were measured too. However, due to the high density of defects, none of the 34×34 arrays went successfully through the entire procedure. Especially, after being written, the junctions had lower resistance and were shorted out to the large number of 'dead' junctions and thus no longer accessible. One example of the measurement of a 34×34 array is shown in Fig. 13a. A large region of device shows currents with wrong direction (shown downward), which is a sign of strong cross talking. Comparing with the SEM image of the measured array (Fig. 13b), the area with wrong current direction matches the area with unsuccessfully lifted-off top electrodes. The upper layer metal left from the lift-off process shorted the top electrodes and caused cross talking. Figure 8 shows an array with a much lower defect count, which means that cross talking would be much less. Unfortunately, the SEM image was taken from a sample sacrificed for SEM purposes; after SEM imaging the sample could not be used for electrical measurement any more. However, that is still evidence that we can make cross-bar memory circuits at 30-nm half-pitch with less cross talking. Moreover, with defect-tolerant computer architecture, defective cross-bar memory will still be usable [13].

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