This is a very interesting article which just appeared in the latest issue of *Nature Materials*. It is not only interesting because it brought up an intriguing question (will the trend of ever-increasing clock speed of Si FET continue), but also because it covered many issues which are important in understanding nanoelectronics (with a conventional structure). It will be a challenge to understand all of these issues thoroughly, thus it is ok to bring these points up during the presentation and leave some of the explanations to me (although I do expect to see you to try your best to address them). Such issues include:

- Constant voltage scaling vs. constant field scaling (explain author's predictions for each approach)
- 60 mV voltage required to decrease off current by 10 (sub-threshold slope)
- High-k dielectrics approach
- Series capacitance
- Strained Si technology