Low voltage, scalable nanocrystal FLASH memory fabricated by templated self assembly

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Abstract

We introduce a new method for building nanocrystal FLASH memory devices that achieves precise control of nanocrystal size and position. Nanocrystal dimensions are defined via polymer self assembly, facilitating device scaling. Devices exhibit low voltage memory operation with promising retention and endurance properties.

Introduction

Nanocrystal floating-gate memories offer a number of potential advantages over FLASH devices, including improved scalability, retention, and cyclability, as well as lower voltage operation. In these devices the floating gate is composed of discrete, electrically-isolated particles (rather than a continuous film as in conventional FLASH), which are typically formed by CVD or aerosol deposition (1). Nanocrystals formed in this way have a wide distribution of size and position, which leads to limitations on device performance, scalability, and manufacturability (2).

Here we introduce a new fabrication method for building nanocrystal memories where Si nanocrystals are defined via a polymer self assembly process, which sets the nanocrystal dimensions, density, and uniformity. The characteristic dimensions of self assembled films depend on intrinsic molecular lengths scales, and are therefore inherently more controllable than structures defined using deposition processes, whose size distributions are limited by nucleation and diffusion effects. The self-assembly technique we have employed results in tight control over nanocrystal size and distribution, allows flexibility in target particle dimensions, and makes possible the formation of nanocrystals of different materials.

In this work we describe the process used to achieve highly-uniform Si nanocrystals embedded in a MOS capacitor gate stack. Devices operate at low voltages, are nonvolatile, and exhibit better endurance than today's FLASH memories.

Device Fabrication

We define Si nanocrystals using diblock copolymer thin film self assembly. This straightforward process involves spin-coating a dilute polymer solution and annealing to promote phase separation into nanometer-scale polymer domains (3). Our diblock copolymer is composed of polystyrene (PS) and poly(methyl methacrylate) (PMMA), whose molecular weight ratio produces hexagonally-close-packed PMMA cylinders in a PS matrix. The PMMA is removed with an organic solvent, leaving a porous PS film. This film is used as a sacrificial layer to define nanocrystals at sub-lithographic dimensions.

The key steps in transforming the self-assembled polymer pattern into Si nanocrystals are (Fig. 1): (a) form the porous PS film on a thermal oxide hardmask (4); (b) etch PS pattern into oxide [4]; (c) grow program oxide (2-3 nm) and conformally deposit a:Si; (d) etch a:Si using an anisotropic RIE process. The Si nanocrystals reproduce the dimensions of the original self-assembled polymer film: a diameter of 20 nm (+/-10%) and a center-to-center spacing of 40 nm (hexagonal close-packed), giving a nanocrystal density of $6.5\times10^{10}/cm^2$ (Fig. 2). Smaller nanocrystal dimensions can be achieved by employing a lower molecular weight polymer [3], providing a route to future device scaling.

The devices are completed by depositing a control oxide (7-12 nm) on top of the nanocrystal array, then depositing, doping, and patterning the polysilicon gate (Fig. 3). A single metal layer is used to contact the gate. Process splits for the MOS nanocrystal capacitors are listed in Table I.

Device Performance

Devices are programmed by injecting charge into the nanocrystals (through the program oxide), and erased by expelling charge from the nanocrystals. The stored charge shifts the device flat band voltage, V_{FB} (Fig. 5). A write voltage, V_W, of -4 V shifts V_{FB} by > 0.5 V. Larger V_{FB} shifts are achieved with higher V_W (Fig. 6), and the magnitude and slope of ΔV_{FB} vs. V_W depend on the program and control oxide thicknesses (t_{prog} and t_{ctrl}, respectively). ΔV_{FB} saturates at high $|V_W|$, when charge begins to leak through the control oxide (Fig. 7). Control devices with no nanocrystals (F) show no CV hysteresis or ΔV_{FB} at $|V_W|$>9V (Fig. 6).

Devices with t_{prog}=3 nm show larger ΔV_{FB} than t_{prog}=2 nm at long write times (for fixed t_{ctrl}), due to the larger voltage on the floating gate for the same V_W (Fig. 8). ΔV_{FB} increases with write time for a fixed V_W. A minimum write time of 50 μs provides ~0.2V ΔV_{FB} at V_W=-6V (device A). We fully erase the devices with a 100 μs erase voltage (V_E) pulse of +4 V.

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We evaluate stability of the written and erased memory states using V_W=-6 V and V_E =+4 V and measuring the small signal capacitance at -2 V as a function of time. Capacitance values are converted to ΔV_{FB} by tracking along a measured CV curve (Fig. 9). For times up to 500 s, ΔV_{FB} for t_{prog}=3 nm remained larger than for t_{prog}=2 nm. A simple logarithmic fit to the measured ΔV_{FB} decay projects retention time $>10^6$ s for t_{ctrl}=2 nm. Device endurance was measured using V_W=-6 V, 50 μs and V_E =+4 V, 50 μs. Capacitance in the two memory states was read at -2 V. The write/erase window remains unchanged out to 10^9 cycles (Fig. 10).

Conclusions

We describe for the first time a nanocrystal FLASH memory where Si particle dimensions are templated by a self-assembled polymer film, providing a manufacturable solution to achieving uniformly-sized and -spaced nanocrystals. These devices function as nonvolatile memory elements with $\Delta V_{FB}>0.5$ V for $|V_W|<4$ V, retention times $>10^6$ s for program oxide as thin as 2 nm, and endurance $>10^9$ cycles.

Acknowledgments

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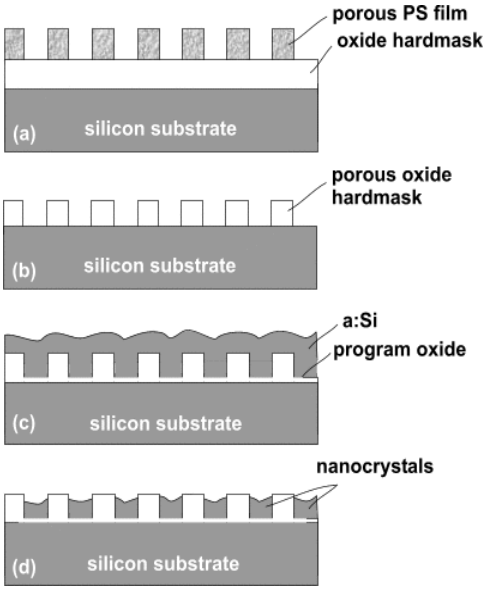

Fig. 1. (a-d) Schematic diagrams of the process flow used to create an array of Si nanocrystals beginning with a porous self assembled polymer template.

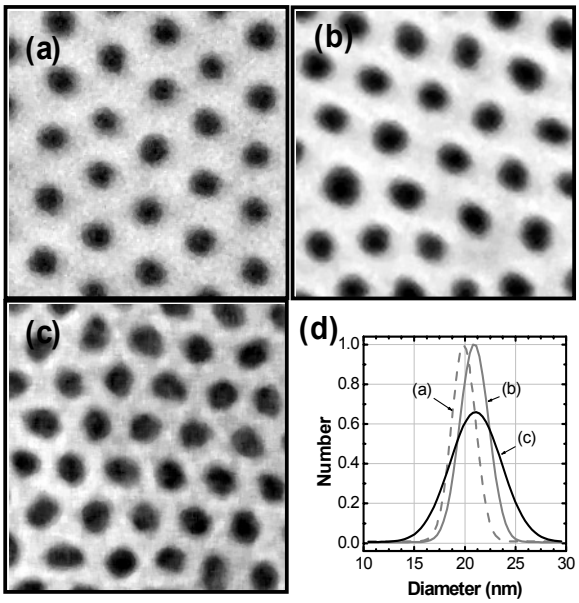

Fig. 2 (a-c) 200×200 nm top-down SEM images of (a) porous polymer film on SiO_2, (b) porous dielectric after pattern transfer into the SiO_2, and (c) Si nanocrystal array. (d) Distribution of polymer pore, dielectric pore, and Si nanocrystal diameters.

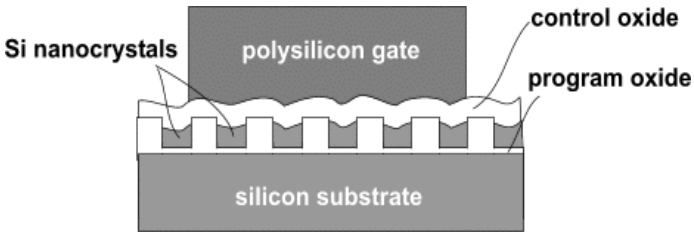

Fig. 3. Schematic diagram of the nanocrystal memory device fabricated and characterized in this work.

Table I. Process splits for nanocrystal MOS capacitors.

Device	Substrate	t_{prog}	t_{ctrl}
A	n+	2 nm	7 nm
B	n+	2 nm	12 nm
C	n+	3 nm	7 nm
D	n+	3 nm	12 nm
E	n–	2 nm	12 nm
F *	n+	2 nm	12 nm

* Control device: no nanocrystals

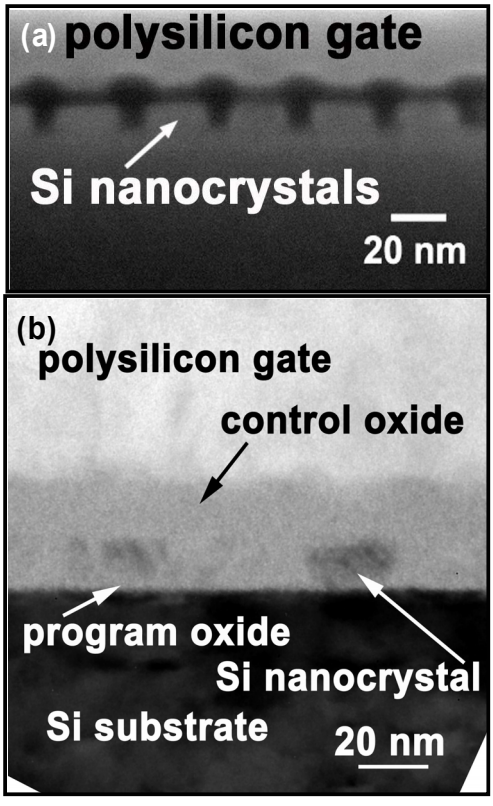

Fig. 4. Cross sectional (a) SEM and (b) TEM images of the nanocrystal memory floating gate device.

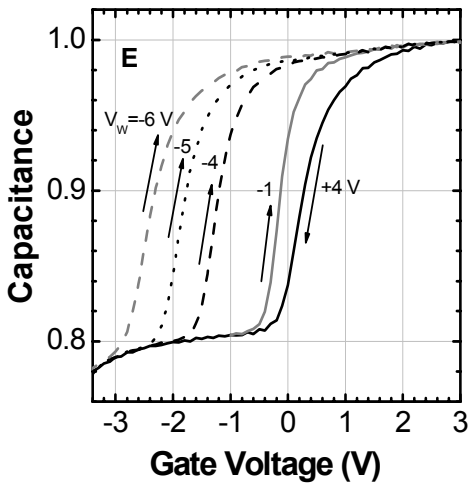

Fig. 5. High frequency (1 MHz) CV traces for device E, showing large V_{FB} shifts for low V_w (write time 20 s).

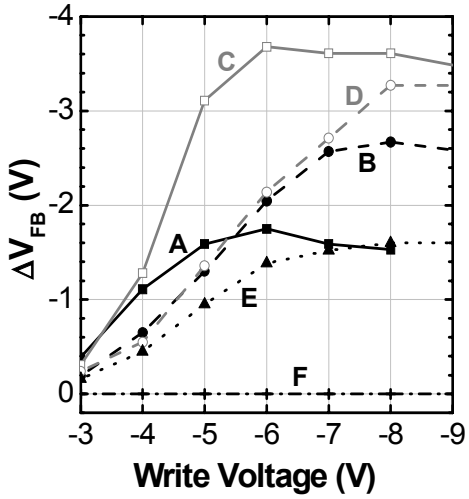

Fig. 6. ΔV_{FB} increases with V_W in all devices (read voltage -2 V, write time 20 s).

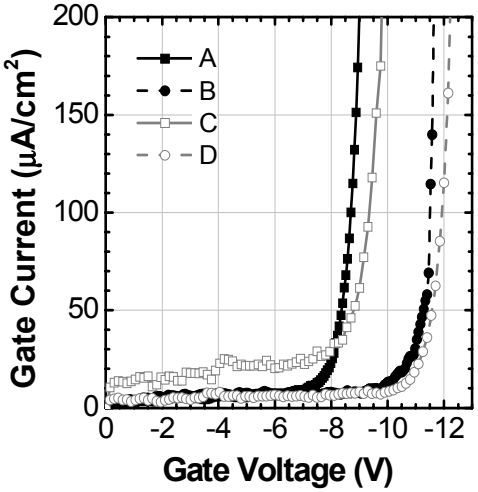

Fig. 7. Device breakdown set by t_{ctrl}.

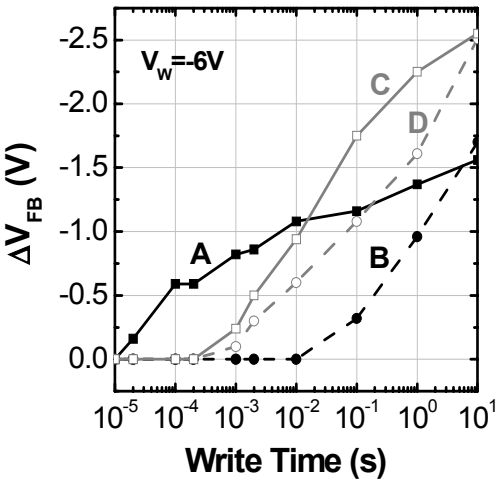

Fig. 8. ΔV_{FB} versus write time (V_W=-6V).

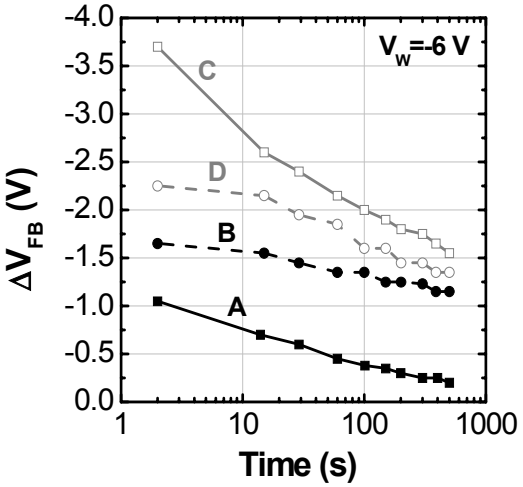

Fig. 9. ΔV_{FB} versus time, showing memory retention for different t_{ctrl} and t_{prog}.

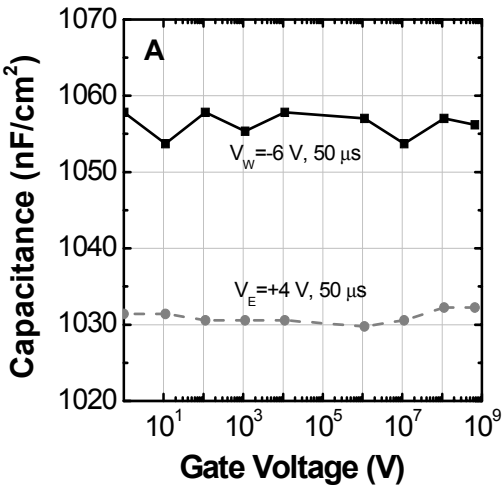

Fig. 10. Capacitance in the written and erased states for device A (read voltage -2V) showing endurance to 10^9 cycles.