Status and Outlook of Emerging Nonvolatile Memory Technologies

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Abstract

This paper reviews the concept, status and challenges of emerging nonvolatile memory technologies. The technologies that are discussed and compared to state of the art Flash technology are the Conductive Bridging RAM (CBRAM), the Ferro-electric RAM (FeRAM), the Magneto-resistive RAM (MRAM), the Organic RAM (ORAM) and the Phase Change RAM (PCRAM).

CBRAM

The CBRAM memory effect is based on a polarity-dependent, resistive switching at a low write threshold voltage Vth of 250mV with typically 2µA write current and an erase voltage threshold of -80mV. The ON-state (low resistance) of a CBRAM memory cell is achieved after a redox reaction driving metal ions in the chalcogenide glass forming metal-rich clusters that lead to a conductive bridge between the electrodes. The memory element can be switched back to the OFF-state by applying a reverse bias voltage. In this case metal ions are removed and due to that size and number of metal-rich clusters are reduced resulting in an erased conductive bridge (resistance increase).

Scalability of the CBRAM technology from 5µm down to 100nm has been demonstrated [1]. As a result the threshold voltage Vth and the ON-state resistance Ron were observed to be feature size independent, whereas the OFF-state resistance ROFF shows the expected dependency up to the resolution limit of 10^{11}Ohm (Fig. 1).

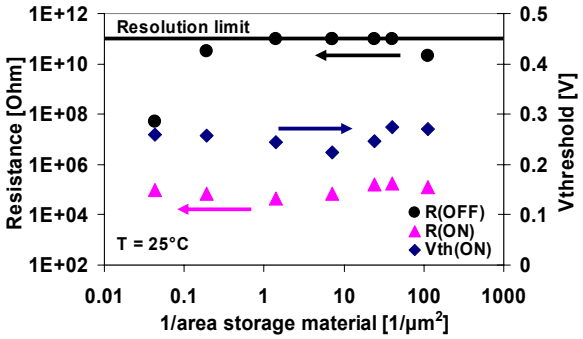

Fig.1 CBRAM cell resistance and threshold voltage as a function of storage material area.

CBRAM data retention has been measured at elevated temperatures (Fig. 2). A slight increase of the low resistance state could be observed, whereas the ROFF values remain constant resulting in a resistance ratio $>10^5$ even after 10 years.

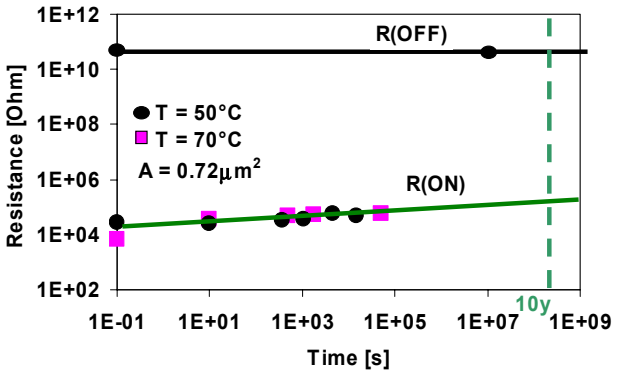

Fig.2 CBRAM data retention measured at elevated temperatures.

FeRAM

FeRAM stores data as remnant polarization in a ferroelectric capacitor. Fig. 3 shows an SEM cross section of a state of the art planar FeRAM cell, used in a 32Mb FeRAM with a cell size of 1.9µm^2. [2]. Key technology ingredients are the chain FeRAM concept and the COP structure (capacitor on plug).

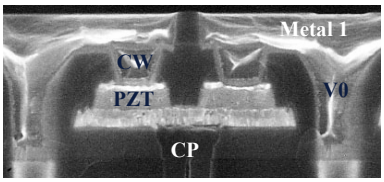

Fig.3 32Mb Chain FeRAM cell with COP (capacitor over plug).

Planar FeRAM cell concepts are limited to cell sizes around 10F^2 (F: minimum feature size) (Fig. 4) and have a limited shrinkability potential. In order to address this, a novel chain FeRAM cell concept using a new 3 dimensional vertical capacitor was developed [2]. This concept is highly scalable and enables structurally small cells down to 4F^2. The 3d vertical capacitor cell saves the space of the V0 contact and the cell size is not defined mainly by the capacitor area. A hysteresis loop of a vertical capacitor is shown in Fig. 5.

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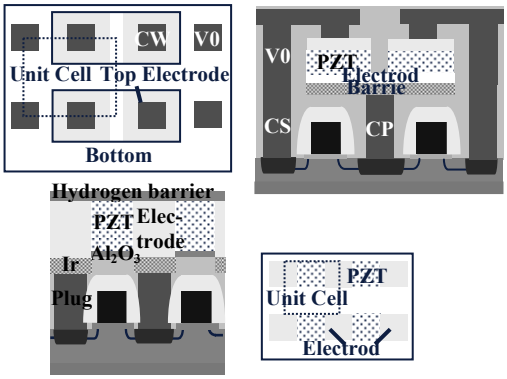

Fig.4 Top: Advanced planar FeRAM cell: $A_{cell}=9.75F^2$
Bottom: Advanced vertical capacitor cell: $A_{cell}=4F^2$

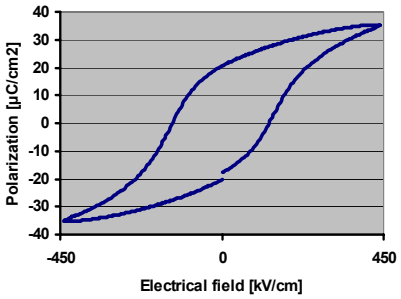

Fig.5 Hysteresis loop from a vertical capacitor with IrO_2 electrodes.

MRAM

In MRAMs the data is stored in the orientation of the magnetization of the storage layer. As for many other BEOL memory technologies 2 cell flavours are possible, a cross point cell and the FET cell, which has an access transistor connected in series with the tunnel junction. The highest published MRAM chip density of 16Mb was accomplished with the FET cell [3] with a 1.4µm^2 cell size. Since the XPC does not require an access device the cell size can be smaller especially because one can stack storage layers on top of each other. However, in order to control parasitic currents and the write operating margin, higher tunnel resistances are required than for the FET cell, resulting in slower random access times.

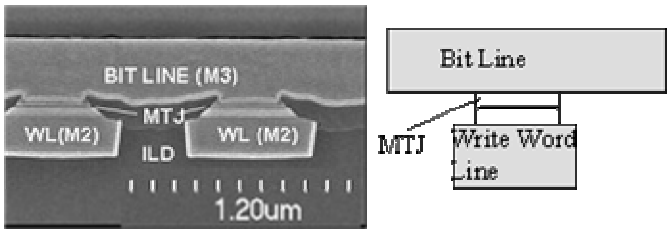

Fig. 6 MRAM cross point cell realization

In XPC MRAM (Fig. 6), the magnetic stack is deposited directly on Cu wires, and then patterned using a single step reactive ion etching process, requiring stopping on Cu and ILD without corrosion. This customized full stack etch process provides magnetic tunnel junction (MTJ) patterning with a local cell resistance spread of ~2%.

The magnetoresistance (MR), the important figure of merit for the READ operation, has been limited to ~ 70%. Higher MR would increase the read operation margin and enable very small MTJs that are essential for scalability. Within our MRAM Alliance with IBM, we pioneered the development of tunnel junctions with 100 bcc textured MgO tunnel barriers and achieved MRs as high as 220% [3]. Fig. 7 shows a resistance versus field characteristic for a tunnel junction of this type, with this example showing a MR of 165%

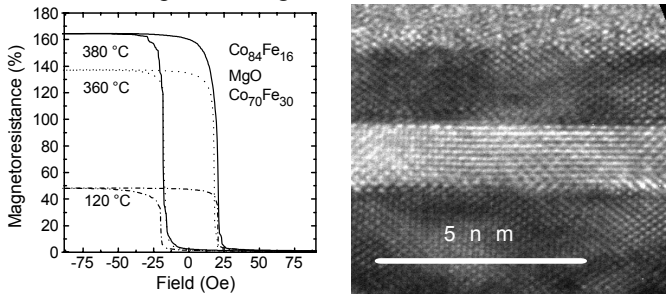

Fig. 7 Tunnelling magnetoresistance of MgO MTJ stack, TaN / IrMn / $Co_{84}Fe_{16}$ / $Co_{70}Fe_{30}$ / MgO / $Co_{84}Fe_{16}$ / Mg, annealed at three different temperatures (left). Cross-sectional TEM image illustrating the highly textured nature of the MgO tunnel barrier (right).

ORAM

The data in the ORAM is stored in an organic storage material that exhibits reversible resistive switching (Fig. 8).

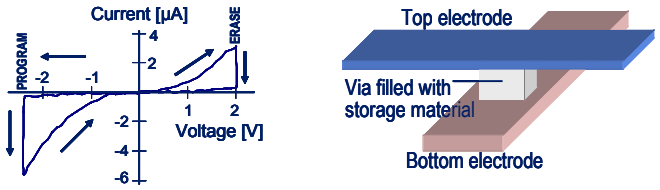

Fig.8 Schematic view of ORAM cell and IV curve. Reversible w/e operation by voltage application, read operation by determination of the high/low conductance state.

With cell structures $\geqslant$ 1x2µm^2 size a retention of >400 days@25° C, extrapolated retention of 10 years@90° C and an endurance of 1E^5 w/e cycles was demonstrated [4]. Fig. 9 and Fig. 10 address the scalability prospects of this technology.

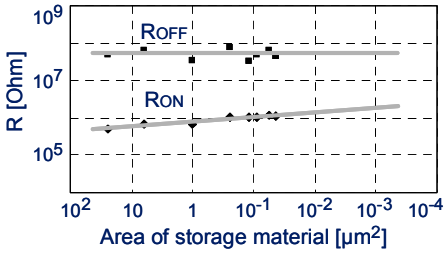

Fig.9 Effect of storage material area on resistance values at T=25°C. Extrapolation indicates a resistance ratio of >10 at an area of 20x20nm^2.

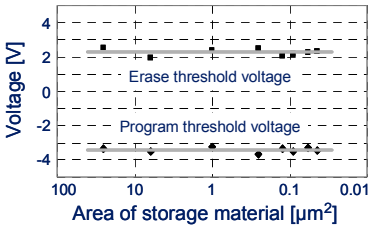

Fig.10 Effect of storage material area on switching voltages (quasi static experiment at 25°C).

Extrapolation indicates a sufficient large resistance ratio ROFF/RON down to a storage material area of 20x20nm^2. The switching voltages are independent of the diameter of the storage material. Very first promising distribution functions for Vth are displayed in Fig. 11. Main challenges for this technology will be the uniformity on large areas and the thermal budget.

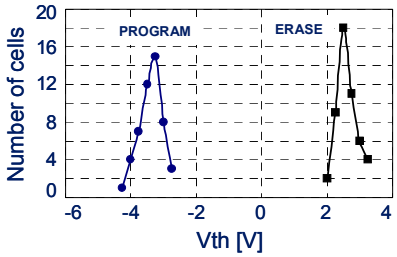

Fig.11 Switching threshold voltage (Vth) distribution functions determined for 50 cells with a via size of 240nm.

PCRAM

The PCRAM is based on a thermally induced reversible phase change between the amorphous and the crystalline phase of a chalcogenide glass ($Ge_xSb_yTe_z$) which is initiated by ohmic heating with an electric current pulse (Fig. 12) [5].

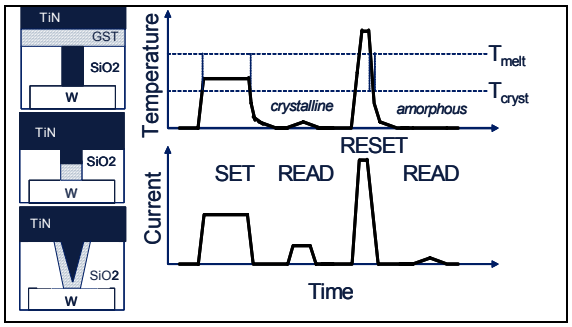

Fig.12 Schematics of different PCRAM resistor geometries with GeSbTe (GST) phase change material: heater cell, active-in-via cell and V-cell (top down). In a set-read-reset-read cycle, the set pulse crystallizes the GST while reset melts and transforms it into the high resistance amorphous state.

Potential concerns for this technology are reducing the reset current in order to obtain structurally small cell sizes while maintaining sufficient write operating margin and thermal cross talk for dense PCRAM arrays. In order to address these concerns, the reset operation was modelled using a finite element approach.

Fig. 13 compares the currents required to melt the GST for different geometries and bottom electrode contact sizes. For all cell designs, the current scales down with decreasing feature size. However, the heater cell exhibits significantly higher reset currents due to lateral current spreading.

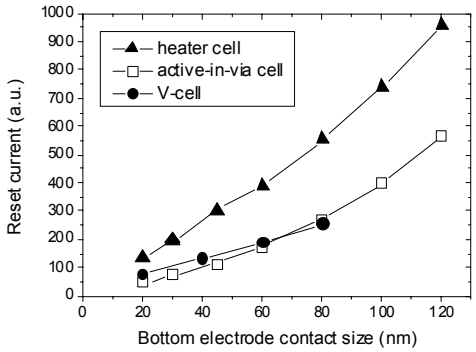

Fig.13 Simulated PCRAM reset current dependence on contact size.

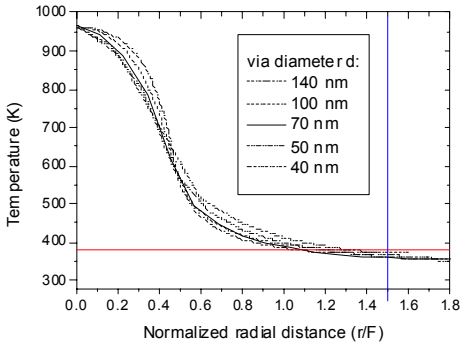

Fig.14 Simulated radial temperature distribution normalized to the via diameter in active-in-via PCRAM cells after 20ns heating. The vertical line indicates the closest position of the next cell in a dense 4F² array. The horizontal line indicates the 10a retention criterion for GST material.

The simulation also shows that the heat plume scales down with the via diameter (Fig. 14). The highest published PCRAM chip density is 64Mb with a cell size of 0.5 µm^2 cell size [5].

Conclusions

Tab. 1 compares the discussed emerging memory technologies to Flash technology [6]. All technologies are non-volatile. All of the emerging memory technologies exhibit a better READ performance than NAND Flash. Flash requires for writing the first bit into the memory many orders of magnitudes longer than the emerging technologies. For FeRAM, MRAM and PCRAM, which are the most widely pursued non-volatile emerging memory technologies, a substantially better WRITE

endurance was demonstrated. With the exception of ORAM all other discussed emerging memory technologies do not require a boosted voltage for the WRITE operation as Flash does. In case of the FeRAM technology the READ operation is destructive, meaning that after every READ operation the information has to be written back into the cell.

The more mature emerging memory technologies, FeRAM, MRAM and PCRAM have comparable properties, with MRAM having a performance advantage, FeRAM having a maturity advantage and PCRAM having a cell size advantage. They all could be used as universal memories, based on their non-volatility, READ/Write performance and high endurance. In order to not just occupy a niche market but to gain a substantial share of the overall memory market, the challenge for all of them is closing the cell size gap to the established memory technologies, Flash and DRAM.

Acknowledgements

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Tab.1 Comparison of the emerging memory technologies to Flash technology.

	Flash	CBRAM	FeRAM	MRAM	ORAM	PCRAM
Maturity	High Volume Product	Single Cells	Niche Products	Product Samples	Single Cells	Product Demonstrators
Density	4Gb	-	32Mb	16Mb	-	64Mb
Cell Size [um^2]	0.025	-	0.6	1.4	-	0.5
Embeddability	Yes	Yes	Yes	Yes	Yes	Yes
Nonvolatile	Yes	Yes	Yes	Yes	Yes	Yes
Random Read Access	80ns/10µs	<200ns	50ns	30ns	<200ns	50ns
Random Write Access	~10µs (erase 100ms)	<200ns	75ns	30ns	<100ns	50ns
Destructive READ	No	No	Yes	No	No	No
Write Endurance	10^6	$>10^5$	$>10^{12}$	10^{15}	10^5	$>10^{12}$
Write Voltage	Vdd+~10V	Vdd	Vdd	Vdd	Vdd+~2V	Vdd
Companies (Criteria: IEDM, ISSCC, VLSI publication during last 3 years)	Actrans Systems, eMemory Tech., Fujitsu, HaloLSI, Infineon, Intel, Macronix, Motorola, Powerchip, Renesas / Hitachi, Samsung, Sandisk, Sony, SST, ST, Toshiba		Agilent, Fujitsu, Hynix, Infineon Matsushita, Oki Ramtron Samsung Sanyo Toshiba TI	IBM Infineon Motorola NEC Renesas Samsung Sony	Infineon	Hitachi Intel Macronix Ovonyx Samsung ST