Room-temperature single-electron transfer and detection with silicon nanodevices

Katsuhiko Nishiguchi, Akira Fujiwara, Yukinori Ono, Hiroshi Inokawa, and Yasuo Takahashi*

NTT Basic Research Laboratories, NTT corporation, 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan
Phone: +81-46-240-2477, FAX: +81-46-240-4317, e-mail: knishi50@aecl.ntt.co.jp
*Present address: Graduate School of Information Science and Technology, Hokkaido University, Sapporo, 060-0814, Japan

Abstract

Transfer and subsequent detection of single electrons are demonstrated at room temperature using a silicon-on- insulator nanodevice. *The turnstile*, which is composed of two Si-wire-FETs with a fine gate, enables us to transfer single electrons by opening and closing the two FETs alternately. The transferred individual electrons are stored in a single-electron box and detected by the electrometer with single-electron resolution. The present device achieves high-speed transfer and long retention.

Introduction

While the scaling of CMOS transistors has allowed to overcome various difficulties and thereby further progress in LSIs, great attention has been attracted, for ultimately low power consumption, by architectures that can treat one electron; e.g. a quantum-dot cellular automata (1) and a single-electron binary decision diagram (2). These architectures require (i) precise control of electron movement and (ii) accurate detection of single electrons. Although various studies demonstrated these two key functions from an academic viewpoint before the implementation of practical architectures, the operation temperature has remained quite low (3,4). This is because the devices were not small enough to prevent thermal energy disturbing electron movement and gain sufficient sensitivity for single-electron detection.
Here, we present an experimental demonstration of single-electron transfer and detection at room temperature.

Fabrication

The device was fabricated using MOS fabrication processes. A one-dimensional wire and a narrow constriction were firstly patterned on a 30-nm-thick silicon-on-insulator layer (Fig. 1). The widths of the one-dimensional wire and constriction before oxidation were 80 and 35 nm, respectively. This was followed by pattern-dependent- oxidation (PADOX) (5). PADOX converts the constriction to a single-electron transistor (SET) structure (an island and tunnel junctions), which was used as an electrometer. Then, two gate electrodes made of phosphorous-doped poly-Si were formed on the one-dimensional wire (Fig. 2). The gate length was 50 nm. These gates, hereafter referred to as lower gates (LG1 and LG2), constitute two one-dimensional FETs (FET1 and FET2) for the turnstile. The tip part (20 nm) of FET1, which is capacitively coupled to the SET island, acts as a single-electron box (SEB1). The other SEB (SEB2) was formed in the channel between FET1 and FET2. We fabricated two devices with a different gap (50 and 100 nm) between the two lower gates, which affects the size of SEB2 and thereby the operating temperature. Finally, an 50-nm-thick oxide layer and an upper gate (UG) were formed. The UG, which covers the entire region shown in Fig. 2, is used to make electrons accumulate in the Si layer and control the potential of SEB1, SEB2 and SET island. Fig. 3 (a) shows the equivalent circuit of the fabricated device. Electrons are transferred between the ER and SEB1 through FET1 and FET2. The SET electrometer detects the number of electrons in SEB1. Fig. 3(b) shows the measured current (I_d) characteristics of the SET as a function of the UG voltage (V_g). From this curve, the size of the SET island is expected to be less than 10 nm. And the SET is carefully positioned close to SEB1. Therefore, the sensitivity of the SET electrometer is high enough for a single electron in SEB1 to be detected (6).

Principle of electron transfer

Fig. 4 explains how electrons are transferred one by one by LG1 and LG2 (7). When FET1 and FET2 turn off, energy barriers to electrons are formed in the channel, and SEB1 and SEB2 are electrically defined. By turning on FET1 and FET2 by turns, electrons are transported from the ER to SEB2 (steps (i) and (ii) in Fig. 4(b)). SEB2 is small enough to retain a fixed number of electrons by the Coulomb blockade (CB). At steps (iii) and (iv), electrons in SEB2 are transferred to SEB1. One transfer cycle for injecting electrons into SEB1 is composed of these four steps. Although there are electrons in SEB1 transferred in the previous cycle, electrons can be transferred by the same mechanism as the cycle shown here until the repulsive force from electrons stored in SEB1 becomes prominent. Therefore, when the repulsive force is not dominant, the number of electrons in SEB1 equals the number of electrons in the SEB2 at step (ii) multiplied by the number of repeated cycles. For electron transfer from SEB1 back to the ER, the energy potential of the ER should be set lower than that of SEB1. Because electrically formed SEB2 can be made smaller than the physical dimension by controlling the external biases [$V_{LG1,2}$, V_g, and V_p; for notations, see Fig. 3(a)], the electron transfer can be achieved at very high temperatures (6).

Experiments

We first investigated the single-electron transfer and detection using the device with the larger gap (100 nm) between the two lower gates at a relatively low temperature (26 K). This is because a larger device at a lower temperature allows a more

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detailed analysis of electron transfer and detection, thereby making it easier to confirm the operation principle. Fig. 5(a) shows changes in the electrometer current I_d when the transfer cycle was repeated at V_p=-0.7 V. Abrupt changes appear at step (iii) in Fig. 4(a). At any change, the height always corresponds to the I_d-V_g shift (ΔV_g) of 4.5 mV, supporting the idea that each change comes from single-electron transfer. As shown in Fig. 5(c), when V_p decreases, ΔV_g per cycle (or the slope) increases. This is because lower V_p increases the number of electrons transferred in one cycle (7). This feature is clearly confirmed by Fig. 5(d). There are V_p ranges in which ΔV_g per cycle did not change. These features reveal that ΔV_g was caused by one electron and that the number (N_c) of electrons per cycle was controlled by the CB. In addition, arbitrary addition and subtraction of a single electron was demonstrated at two V_p's by repeating cycles as shown in Fig. 6. Changing V_p allows to control the number of electrons for each addition and subtraction, e.g. addition of a fixed number of electrons as shown in Fig. 5(c).

Fig. 5(d) shows another noteworthy point. When the total number of electrons in the SEB1 increased, the repulsive force from electrons stored in SEB1 caused a reduction of ΔV_g per cycle. This repulsive force caused the non-linearity of characteristics shown in Fig. 5(c) when the total number of electrons in SEB1 exceeded 40.

We investigated single-electron transfer and detection with this device at room temperature. Although V_p was set so that the average number of electrons per cycle became one, transfer error appeared as shown in Fig. 7. This is because the charging energy in SEB2 is not large enough for the CB to become dominant at room temperature.

To achieve a larger charging energy (i.e. smaller SEB2) for room-temperature operation, we used the device with the smaller (50 nm) gap between the lower gates. We also applied a negative (-5 V) bias to the SOI substrate so that electrons would accumulate at the front interface of the SOI for stronger confinement. This accumulation and small gap of the lower gates were expected to make SEB2 small enough for the CB to become effective at room temperature. Fig. 8 shows that the fixed number of electrons was transferred to SEB1 in every cycle; that is, the controllability of N_c was improved for the smaller gap even at room temperature. For the purpose of revealing that the CB controls the electron transfer, we discuss the dependence of the number of transferred electrons per cycle on V_p by using the pulse sequences shown in Fig. 9(a). During "OUT", all electrons are ejected from SEB1 to the ER in order to eliminate the repulsive force caused by electrons in the SEB1. I_d is plotted in Fig. 9(b). When V_{LG1}= V_{LG2}=-4 V, I_d gradually increased because of the capacitive coupling between the ER and SET (the solid curve). On the other hand, when pulsed voltages were applied to LG1 and LG2 as shown in Fig. 9(a), I_d discretely changed (open circles). And there are $V_{p\text{-}LOW}$ ranges in which I_d did not change. These features reveal that the CB becomes dominant for the control of N_C.

Finally, we mention high-speed transfer and long-term-retention characteristics. Fig. 10 indicates that transfer speed and retention times can reach 10 nanoseconds and 10^4 seconds, respectively. These results are due to the *variable* height of the barriers controlled by the lower gate voltage; i.e., the barriers become very transparent when electrons are transferred, while they become insulative when electrons are stored in SEB1 (7,8).

Conclusion

At room temperature, single-electron transfer and detection were demonstrated with a device having a FET-based turnstile and SET electrometer. The FET-based turnstile allows arbitrary addition and subtraction of a single electron as well as accurate and fast electron transfer and long retention time. The PADOX SET can be fabricated close to the SEB and has sufficient sensitivity to detect single electrons. The present results represent the characteristics of multilevel single-electron memories and are promising for the implementation of single-electron-transfer-based solid-state circuits. Since the device is fabricated by the MOS LSI fabrication process, the scaling of CMOS transistors can be expected to further improve the performance (accuracy and speed).

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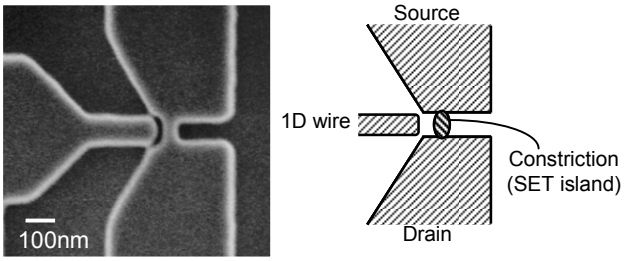

Fig.1. SEM image and schematic view of the one-dimensional FET and detector before lower gate formation. The widths of the one-dimensional wire and constriction for the SET channel before oxidation were 80 and 35 nm, respectively.

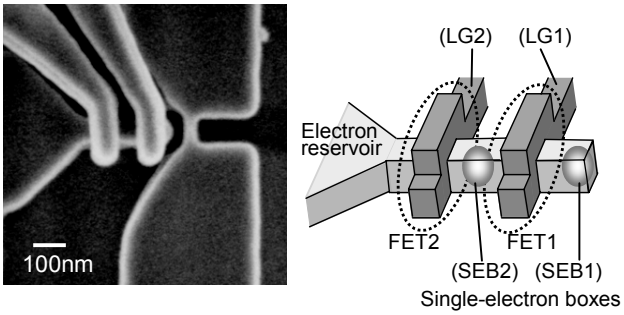

Fig. 2. SEM image and schematic view of the one-dimensional FETs after lower gate formation. The gate length was 50 nm, and the gap between the two lower gates was 50 or 100 nm.

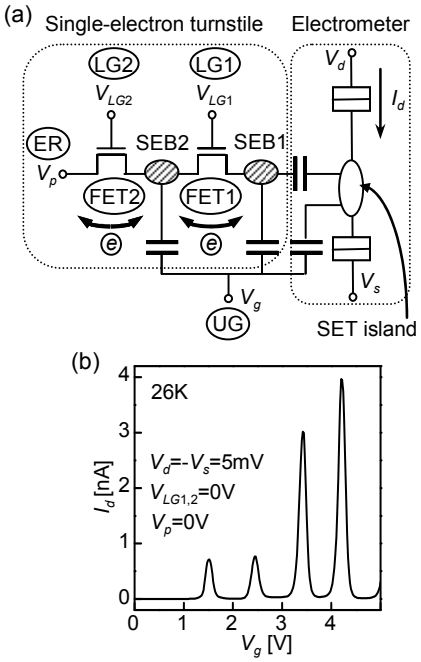

Fig. 3. (a) Equivalent circuit of the fabricated device. (b) Measured current characteristics of the SET electrometer as a function of V_g. The SOI substrate voltage was 0 V.

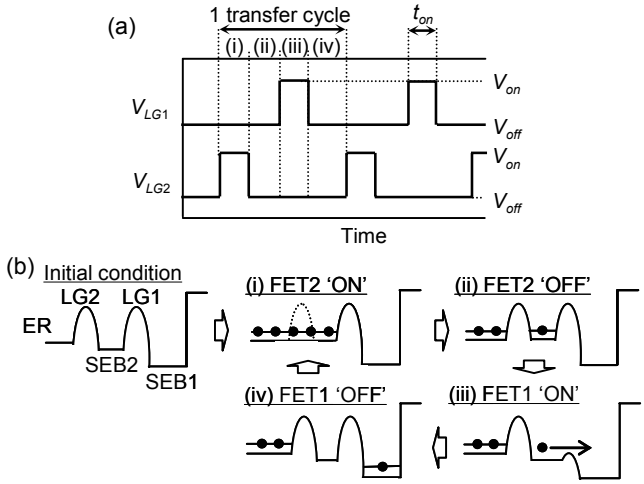

Fig. 4. (a) Pulse sequences of V_{LG1} and V_{LG2}. The phase of V_{LG1} is different from that of V_{LG2} by π . (b) Sequences for transferring electrons from the ER to SEB1 through SEB2.

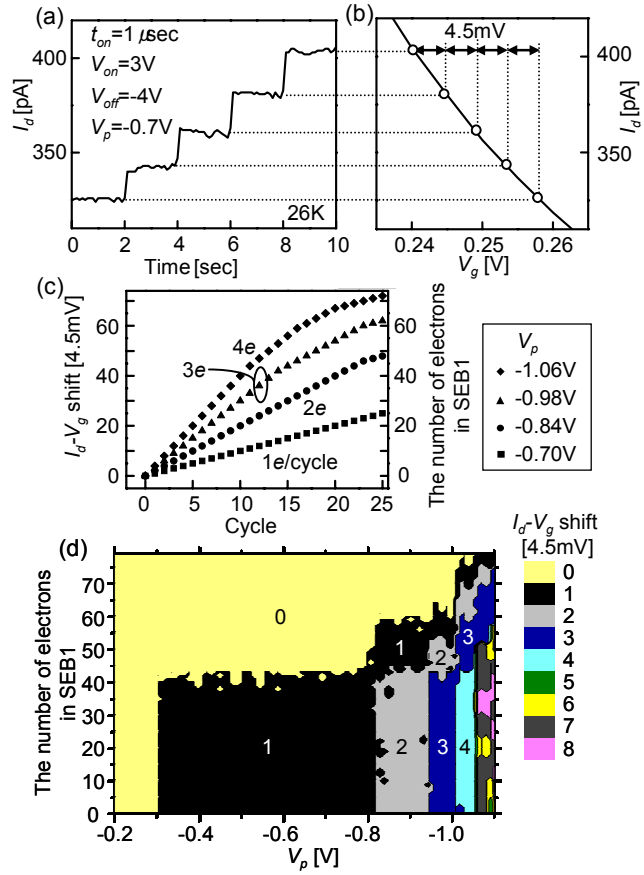

Fig. 5. (a) Change in I_d when transfer cycles were repeated. V_d=-V_s=5 mV. Transfer cycle time was 2 s. (b) Fitting of quantized I_d (open circles), shown in (a), to I_d-V_g (solid line) of the SET. (c) Dependence of I_d-V_g shift and number of electrons in SEB1 on the number of cycles at various V_ps. (d) Contour plot of I_d-V_g shift per one transfer cycle versus V_p and total number of electrons in SEB1. The plot interval for V_p was 10 mV.

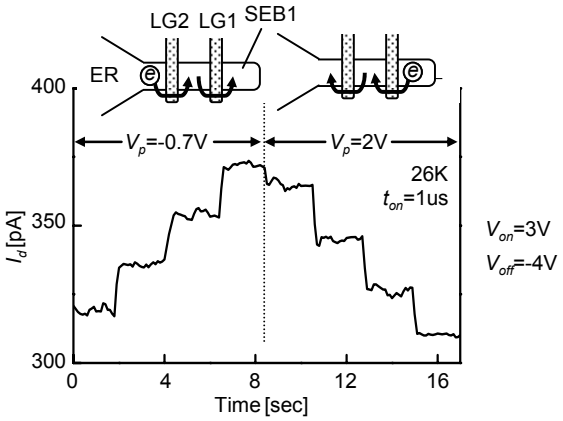

Fig. 6. Addition and subtraction of single electrons. Transfer cycle time was 2 s. The small decrease in I_d was caused when V_p was changed from -0.7 to 2 V because of the capacitive coupling between the electron reservoir and the electrometer.

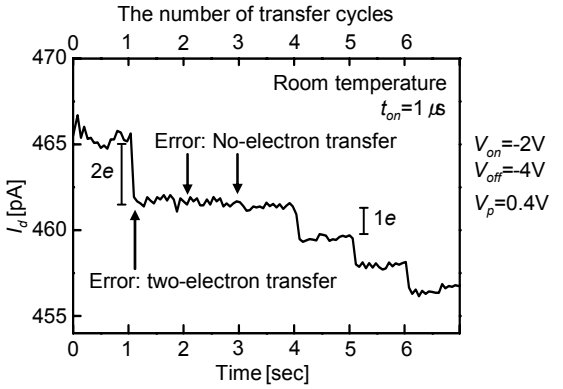

Fig. 7. Transfer error at room temperature for the device with a 100-nm gap between the two gates. V_d=-V_s=5 mV and V_g=0 V. Time for transfer cycle was 1 s. The SOI substrate was biased at 15 V.

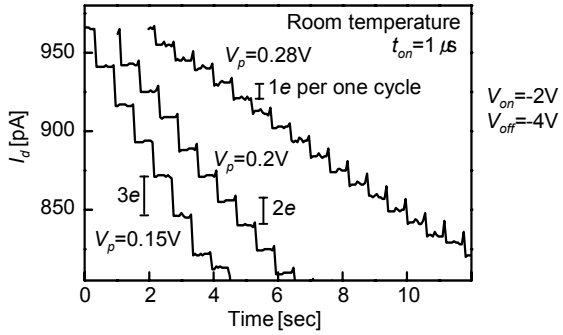

Fig. 8. Successful transfer at room temperature for the device with a 50-nm gap between the two gates. The curves at V_p=0.2 and 0.28 V are shifted horizontally by 1 and 2 seconds, respectively, for clarity. V_d=-V_s=5 mV. Time for one transfer cycle was 0.5 s.

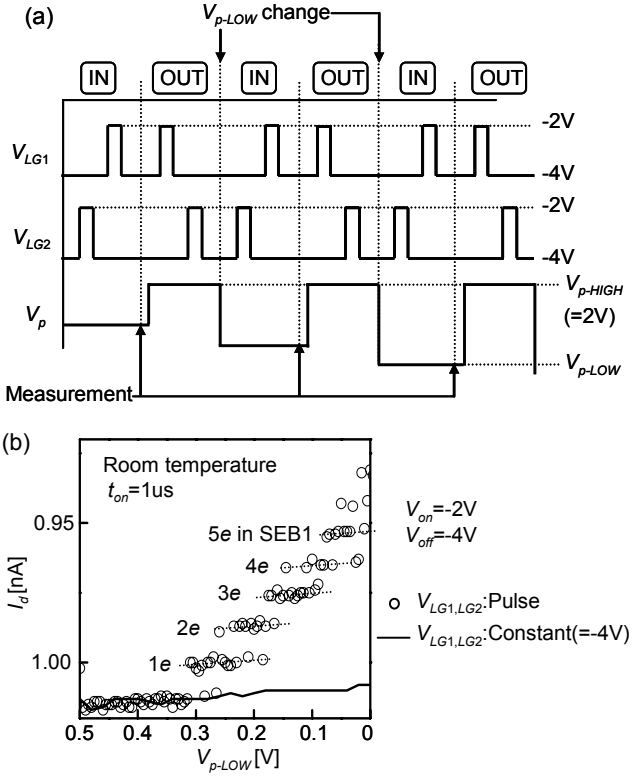

Fig. 9. The electron injection characteristics for various ER pulse voltage $V_{p\text{-}LOW}$. (a) Sequences of V_{LG1}, V_{LG2}, and V_p. During "IN", electrons are transferred from the ER to SEB1. During "OUT", all electrons are ejected from the SEB1 to the ER. I_d was measured just after "IN". (b) Experimental characteristics. The solid curve is when V_{LG1}= V_{LG2}=-4 V, where no electron movement occurs because of complete shutoff.

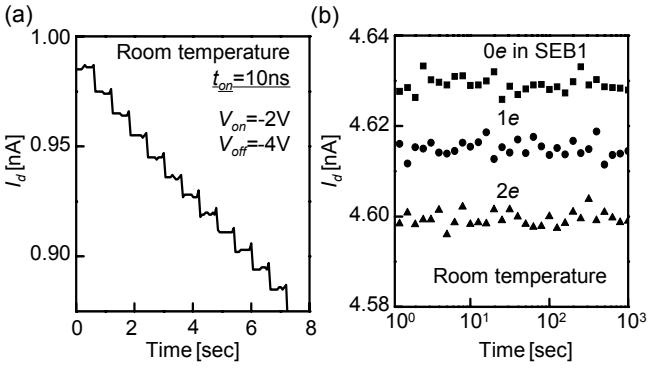

Fig. 10. (a) High-speed electron transfer. Time (t_{on}) for opening FET1 or FET2 was 10 ns. The other measurement conditions are the same as those in Fig. 8. The device may be operated faster, but further investigation is required for optimization of the measurement system for higher frequency measurement. (b) Retention characteristics of electrons in SEB1 at V_{LG1}=V_{LG2}=-4 V. The other measurement conditions are the same as those in Fig. 7.