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Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-κ Gate Dielectrics

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ABSTRACT

High-performance enhancement-mode semiconducting carbon nanotube field-effect transistors (CNTFETs) are obtained by combining ohmic metal–tube contacts, high-dielectric-constant HfO_2 films as gate insulators, and electrostatically doped nanotube segments as source/drain electrodes. The combination of these elements affords high ON currents and subthreshold swings of ~70–80 mV/decade and allows for low OFF currents and suppressed ambipolar conduction. The doped source and drain approach resembles that of MOSFETs and can impart excellent OFF states to nanotube FETs under aggressive vertical scaling. This presents an important advantage over devices with a metal source/drain, or devices commonly referred to as Schottky barrier FETs.

In recent years, intensive research on single-walled carbon nanotube (SWNT)-based field-effect transistors (FETs)[1−9] has revealed the excellent properties of these novel materials, including ballistic transport[2] and high chemical stability and robustness.[1] Nevertheless, it remains an open question as to what the ultimate nanotube FETs may be in structure and performance and how to achieve the optimum ON current and conductance, high ON/OFF current ratios, steep switching, and highly scaled gate dielectrics and channels. It has been shown recently that with high-work-function Pd contacts one can obtain zero or slightly negative Schottky barriers (SBs) to the valence bands of semiconducting tubes (for diameters of $d > \sim 2$ nm).[2] This can improve the ON currents and afford low drain-bias conductance near $4e^2/h$. Steep switching between ON and OFF states for nanotube transistors can be achieved by the integration of thin high-κ gate dielectrics, which produces subthreshold swings close to the theoretical limit of $S \approx (k_B T/e) \ln(10) = 60$ mV at room temperature.[1]

Here, we report p-channel nanotube FETs composed of ohmic Pd−tube contacts and high-quality thin HfO_2 gate insulator films. The objective is to advance nanotube transistors through the integration of optimum contacts and gate dielectrics, a task that has not yet been undertaken. The structure of our nanotube FETs is shown in Figure 1b. Its operation involves the bulk switching of the segment of a nanotube underneath an Al top-gate/HfO_2 gate stack, while outside the top-gate region the two segments of the tube are electrostatically "doped" by a back gate and act effectively as source and drain (S/D) electrodes. Such nanotube device structure (named DopedSD-FETs here) has been made previously,[1,8] mainly for the demonstration of bulk nanotube switching that differs from SB modulation in nanotube FETs with metal as S/D (Figure 1a, denoted as MetalSD-FETs). However, the integration of ohmic contacts for ON-state optimization and detailed characteristics of the OFF states of DopedSD-FETs have not been addressed.

The fabrication of our DopedSD-FETs was similar to that described in ref 1, involving first the formation of MetalSD-FETs (Figure 1a) on SiO_2 ($t_{ox} = 10$ nm)/p^+ Si substrates. Pd was used in place of Mo to contact nanotubes here. The SiO_2/Si substrates were as described in ref 9, with 100-nm SiO_2 covering most of the areas of the substrates and 10-nm SiO_2 (grown by dry oxidation) formed locally under the transistor channel regions.[9] The Pd MetalSD-FETs (Si as the back gate) were characterized by electrical transport measurements before being subjected to the atomic layer deposition (ALD) of an ~8-nm-thick HfO_2 ($\kappa \approx 20$) film using a

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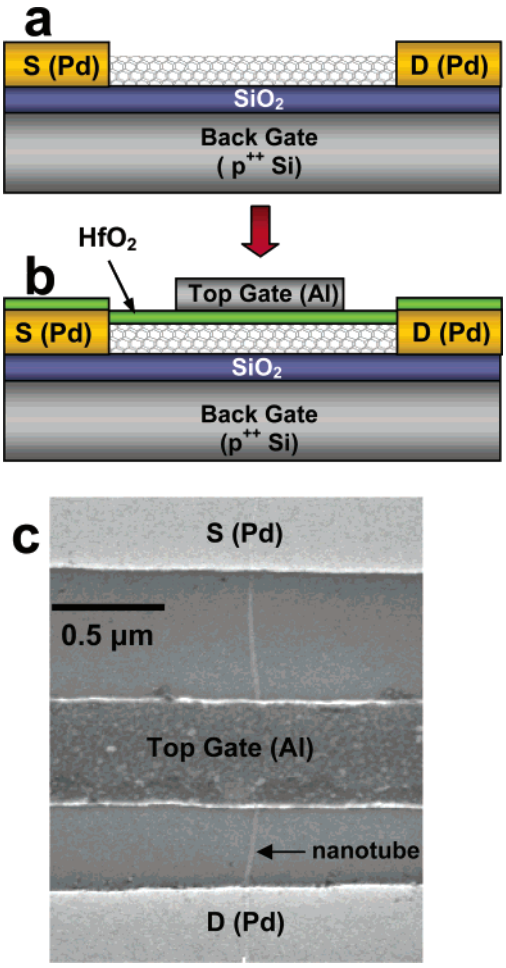

Figure 1. (a) Schematic device drawings for a nanotube FET with metal as S/D (MetalSD-FETs, thickness of SiO_2 = 10 nm). (b) Nanotube FET with back-gate electrostatically doped nanotube segments as S/D (DopedSD-FET). The thickness of the top Al gate is ~20 nm. (c) Scanning electron microscopy (SEM) image of the device depicted in b. For all of our devices here, the total tube length between metal electrodes was ~2 μm, and the top-gated section length was ~0.5 μm. Misalignment caused differences in the lengths of the S/D tube segments.

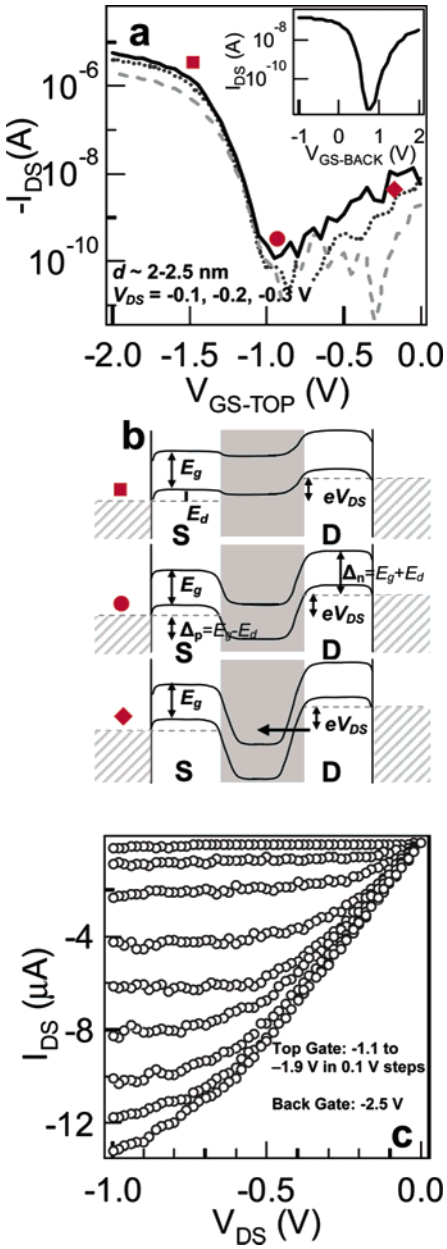

Figure 2. Electrical properties of a DopedSD-FET (tube diameter ≈ 2.3 nm). (a) Transfer characteristics at different V_{DS} (dashed curve, V_{DS} = −0.1 V; dotted, V_{DS} = −0.2 V; solid, V_{DS} = −0.3 V). (Inset) Same tube versus back gate under V_{DS} = 10 mV in MetalSD-FET geometry prior to high-κ deposition. (b) Band diagrams corresponding to I_{ON} (top), I_{MIN} (center), and $I_{n-channel}$ (bottom) regions in a. The shaded region corresponds to the top-gated nanotube section. (c) Output characteristics of the top-gated device in a.

tetrakis(diethylamido)hafnium precursor at 150 °C.[10] Top-gate electrodes were then patterned to afford DopedSD-FETs (Figure 1b). Note that in ref 1 ALD of ZrO_2 at 300 °C using $ZrCl_4$ as a precursor was employed for dielectric deposition. Compared to the $ZrCl_4$/300 °C ALD approach, the alkylamide/150 °C approach is advantageous in two respects. First, the chloride precursor tends to cause irreversible (by, for example, annealing) unintentional p-doping of the nanotubes, resulting in depletion-mode FETs. The alkylamide ALD process does not cause such a doping effect, especially after an annealing step (at 180 °C for 2 h) following the deposition. Second, ALD at 300 °C tends to degrade the Pd−SWNT contacts and causes a significant increase in contact resistance. Such degradation is avoided by ALD at 150 °C.

The simultaneous integration of high-κ gate dielectrics and high-quality Pd−tube contacts affords the highest performance DopedSD-FETs thus far (with the back gate set at a constant bias of $V_{GS\_BACK} \approx -2$ V). Figure 2 shows a representative device (tube diameter $d \approx 2.3 \pm 0.2$ nm) exhibiting a transconductance of $g_m = dI_{DS}/dV_{DS}|_{V_{DS}} \approx 20$ μS (corresponding to 5000 S/m, normalized[7] by 2d; ON-current $I_{ON\_sat} \approx 15$ μA (~3750 μA/μm)) and a linear ON conductance of $G_{ON} \approx 0.1 \times 4e^2/h$. A rough estimation shows that the observed g_m and I_{ON_sat} are higher than the state-of-the-art Si p-MOSFET[11] by a factor of ~5 at a similar gate overdrive and better than previous DopedSD-FETs (with Mo electrodes)[1] by a factor of ~3 because of the improved Pd−tube contacts. The subthreshold swing of the device is $S \approx 80$ mV/decade. The minimum current (I_{MIN}) in I_{DS}−

V_{GS} is relatively bias-independent (for $V_{DS} = -0.1$ to -0.3 V) and $I_{ON}/I_{MIN} > 10^4$. At higher gate voltages, ambipolar n-channel conduction is observed for this $d \approx 2.3 \pm 0.2$ nm SWNT device with $I_{ON}/I_{n-channel}$ close to 10^3.

We observe comparable p-channel ON states for our Pd MetalSD-FETs and DopedSD-FETs (i.e., the same devices before and after ALD and top-gate formation, respectively) with similar $I_{ON} \approx 15-20$ μA and $G_{ON} \approx 0.1 \times 4e^2/h$. This suggests that high-κ deposition does not cause degradation of the ON states.[1] Because relatively long tubes with $L \approx 2$ μm are used in this work, the channel transmission is $L_{mfp}/(L + L_{mfp}) \approx 0.1$ (nonballistic channel) where $L_{mfp} \approx 300$ nm is the mean free path for scattering in nanotubes at low drain biases.[2] We note that in the future, channel-length scaling should include both the top-gated tube section and the S/D segments of the ballistic regime ($L < \sim 10$ nm)[13] to minimize the parasitic resistance. Novel lithography approaches and self-aligned process will be necessary to achieve this goal.

In the subthreshold region, $S \approx 70-80$ mV/decade for our DopedSD-FETs, and $S \approx 130$ mV/decade for our MetalSD-FETs. The difference appears to be due to the more efficient electrostatic gating for the high-κ/top-gate stack. The top and back gate capacitances are $C_{top} \approx 2.9$ pF/cm and $C_{back} \approx 0.38$ pF/cm, respectively, as extracted by numerically solving[14] the 2D Poisson equation for a slice in the direction normal to the nanotube. The top-gate capacitance of $C_{top} \approx 2.9$ pF/cm is in fact near the quantum capacitance of $C_Q \approx 4$ pF/cm for SWNTs.[1,3]

It is interesting to compare the minimum currents I_{MIN} and n-channel leakage currents for various types of nanotube FET geometries. First, we note that the back-gated MetalSD-FETs (for tubes with $d \geq 2$ nm, $t_{ox} \approx 10$ nm) exhibit strong ambipolar conductance with high n-channel leakage currents even under a low bias of $V_{DS} = 10$ mV (Figure 2a inset). This differs from our previous MetalSD-FETs with thicker SiO_2 ($t_{ox} = 67$ nm) that display negligible n-channel leakage currents.[2] The high n-channel currents for the $t_{ox} = 10$ nm case is due to tunneling currents through the thin SB (because the width of SB $\approx$ dielectric thickness t_{ox}) to the conduction band (CB) of the nanotube.[14,18] For thick gate oxides, the minimum current is determined by thermal activation over the full band gap of the tube,

$$I_{MIN} \propto \exp\left(-\frac{E_g}{k_B T}\right) \tag{1}$$

which can afford $I_{ON}/I_{MIN} \approx 10^6$ even for $d > 3$ nm ($E_g < 0.4$ eV) tubes under high V_{DS}.[2] Although the ambipolar conduction and minimal leakage current can be suppressed by producing highly asymmetric Schottky barrier heights for electrons (SB height $\approx E_g$) and holes (SB height ≈ 0) when the gate oxide is thick, Figure 3a clearly shows that the situation is different for thin gate oxide MetalSD-FETs because of high tunneling currents. With aggressively scaled t_{ox} and highly transparent SBs, the minimum current is governed by electron and hole thermal activation barriers

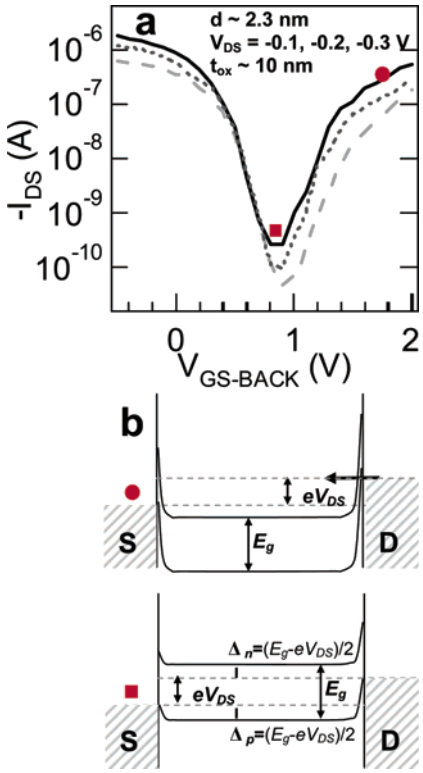

Figure 3. (a) $I_{DS}-V_{GS}$ curves for MetalSD-FETs ($d \approx 2.3$ nm, back-gated, SiO_2 thickness 10 nm) under various V_{DS} (solid line, $V_{DS} = -0.3$ V; dotted, -0.2 V; dashed, -0.1 V). (b) Band diagrams for the device under gate biases corresponding to the n channel (top diagram) and minimal (bottom diagram) leakage currents, respectively.

(see Figure 3b) of $\Delta_n = \Delta_p = (E_g - e|V_{ds}|)/2$,[14]

$$I_{MIN} \propto \exp\left[-\left(\frac{E_g - e|V_{ds}|}{2k_B T}\right)\right] \tag{2}$$

For our $t_{ox} \approx 10$ nm MetalSD-FETs (though not yet scaled to $t_{ox} \approx 2$ nm), we indeed observe the trend of higher I_{MIN} for higher V_{DS} (Figure 3a). Note that it has been pointed out recently[14,16] that as a result of eq 2, ultrascaled MetalSD-FETs will exhibit unacceptable OFF state leakage under useful operating voltages (e.g., $V_{DS} \approx 0.6$ V), even for devices with small-diameter tubes ($d \approx 1$ nm, $E_g \approx 0.8$ eV).

Our DopedSD-FETs exhibit low I_{MIN} and much suppressed ambipolar conduction (relative to those of the MetalSD-FETs, Figure 2a inset) for $V_{DS} = -0.1$ to -0.3 V (Figure 2a). No significant bias dependence for I_{MIN} is observed, at least for $d < \sim 2.3$ nm, and high $I_{ON}/I_{MIN} \approx 10^5$ can be readily obtained at $V_{DS} = -0.3$ V. These characteristics are drastically improved over those of the MetalSD-FETs, owing to the design of using nanotube segments as S/D, as predicted theoretically.[14] The minimum leakage current is predicted to be determined by a hole activation barrier of $\Delta_p \approx (E_g - E_d)$,

$$I_{MIN} \propto \exp\left[-\frac{(E_g - E_d)}{k_B T}\right] \tag{3}$$

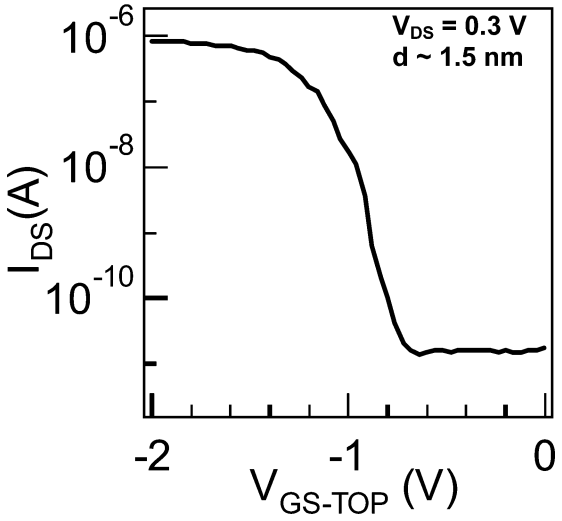

Figure 4. Transfer characteristic of a DopedSD-FET with a $d \approx$ 1.5 nm SWNT at $V_{DS} = 0.3$ V.

where E_d is the energy spacing from the valence band edge to the Fermi level in the p-doped S/D segments (Figure 2b).[14] In our experiments, E_d is set by back-gate electrostatic doping under $V_{GS\_BACK} \approx -2$ V, which corresponds to $E_d \approx 0.2$ eV. (The back gate efficiency for $t_{ox} = 10$ nm SiO_2 is ~0.1.) Equation 3 also predicts the insensitivity of I_{MIN} to V_{DS}, as observed experimentally. The fundamental difference for the OFF state characteristics between the Metal- and DopedSD-FETs is that the latter employs doped semiconductors as S/D, much like a conventional MOSFET. Because there are no states within the band gap of the S/D electrodes, I_{MIN} will be determined by activation over $\sim E_g$ as opposed to $E_g/2$ in the MetalSD-FETs. The n-channel leakage current in the DopedSD-FETs is due to band-to-band tunneling (Figure 2b, bottom drawing), which is low because high gate voltages are required to obtain $I_{n-channel}$ comparable to I_{ON}. The results here clearly demonstrate that DopedSD-FETs are much more vertically scalable than MetalSD-FETs and can afford a low OFF state current even for relatively large diameter (~2 nm) tubes and high biases.

We have also characterized DopedSD-FETs for SWNTs with diameters of ~1.5 nm. The measured transfer characteristics of $d \approx 1.5$ nm ($E_g \approx 0.6$ eV) DopedSD-FETs is shown in Figure 4. Because of the presence of small but finite SBs at the Pd−tube contacts for $d < 2$ nm tubes[2] and thus higher parasitic resistance, relatively low $G_{ON} \approx 0.02 \times 4e^2/h$ is measured for this device. Nevertheless, the device exhibits $S \approx 80$ mV/decade, as a result of near-MOSFET operation (instead of SB modulation). We observe high $I_{ON}/I_{OFF} \approx 10^5$ and no ambipolar conduction, suggesting excellent OFF states for DopedSD-FETs with small-diameter nanotubes (but at the expense of lower ON states).

In summary, enhancement-mode nanotube FETs with high-quality contacts, high-κ dielectric HfO_2 films, and electrostatically induced nanotube source/drain regions are demonstrated. Future tasks will include chemical doping of the nanotube S/D segments to replace back-gate electrostatic doping. Contacts with nearly-zero SBs to small-diameter SWNTs should be developed to optimize I_{ON}/I_{OFF} during vertical scaling. Strategies for channel-length scaling for DopedSD-FETs should also be devised.

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