EECS 627, Lab Assignment 3

1 Introduction

In this lab assignment, we will use *Cadence ICFB* and *Calibre* to become familiar with the process of DRC/LVS checks on a design. So far, we have placed and routed each individual block and have completed the global assembly of our multiplier chip. Next, we will perform physical design verification on the layout to ensure that the layout generated by silicon ensemble actually matches the Verilog file. We will keep this lab simple and perform DRC/LVS only on the multiplier block.

2 Cadence and Calibre Setup

You will have to perform the following steps in order to setup your environment for Candence-ICFB and Mentor-Calibre

- From `swselect` on the CAEN prompt, select latest versions of CADENCE IC, CALIBRE, MENTOR DFT
- Add the following line to your .cshrc
  ```
  setenv MGC_HOME /afs/engin.umich.edu/caen/sun_9/mentor-D.1/
  ```
- Create a library (e.g. MY_LIB_3) in your working directory (e.g. labs/drc_lvs) in the allotted CAEN disk space
- Copy the following files to your working directory:

  ```
  /afs/engin.umich.edu/class/perm/eecs627/cadence/cds.lib
  /afs/engin.umich.edu/class/perm/eecs627/cadence/display.drf
  /afs/engin.umich.edu/class/perm/eecs627/cadence/opus.map
  ```
- Run icfb and create a new library
  ```
  > icfb &
  > File---> New---> Library
  ```
- Enter the name of your library (e.g. MY_LIB_3).
- Click on the option "`attach to an existing techfile`" and press OK
- Choose tsmc18 to attach your new library to.
- Create a directory called "CALIBRE" in your working directory and copy the following files into it:

  ```
  /afs/engin.umich.edu/class/perm/eecs627/calibre/generic018.drc
  /afs/engin.umich.edu/class/perm/eecs627/calibre/generic018.lvs
  /afs/engin.umich.edu/class/perm/eecs627/calibre/queryskl/calibre.skl
  ```

3 Steps for performing DRC/LVS

For the purposes of DRC/LVS on a block we need to be able to import it in a layout editor such that we can make corrections to it. Import the mult.def generated by silicon ensemble to create a layout view of multiplier in ICFB. The def file format stands for “design exchange format” and serves to, as the name suggests, import designs created as the output of a tool into another in the Cadence tool chain. When we placed and routed the multiplier block in sedsm in the last assignment, we exported a “mult.def” file from sedsm. If you open in the def file in a text editor such as emacs, you will find that it defines the co-ordinate location of each cell in the design and the orientation. The co-ordinate system in a def file has the origin in the same place as it was when the block was routed in sedsm. The orientation of a cell (ie North/Flip-North/South/Flip-South) defines the way in which the particular cell is placed in the block.

There are 4 cell-views in ICFB: abstract, layout, schematic and symbol. The abstract cell view specifies only the metal routing and the placement of pins in the cell. The layout view gives all the mask level detail of the block. The schematic view is just a pictorial representation of the structural netlist and finally the symbol view as the name suggests is the “symbol” of the particular cell/block in a schematic where it is instantiated.

When you import the .def format, you get all the cells in the abstract view. You need to convert it back to the layout view. Here is how you import the def from the icfb command interface window (CIW) menu.

- `File-->Import-->DEF`
- `library name --> MY_LIB_3`
- `cell name -->` Whatever you want to call your multiplier block ie my_mult/mult etc.
- `view name --> abstract`
- `Use reference library names ---> tsmc18`
- `DEF File Name -->` whatever you called your def file (e.g. mult.def)
- `Map names from --> VERILOG`

Basically, what the form does is that it imports the def file and references each cell in the def file to the corresponding cells in hte tsmc18 library. Please note that it is best to import the design names from a library as opposed to copying over the entire library itself.

- Open your multiplier: `File-->Open`
- Select the correct cell name and hit “OK”
- Now save the abstract view: `Design-->Save`
- From the Tools menu, click on Layout and it will bring up the LSW window. The LSW window should have the different layer windows and the colors that is used to represent each layer.

- Back in the main layout editing window, go to `Edit-->Search`

A new window will open. Perform the following tasks in the new window:

- Click "`Add Criteria`"
- In the box below, change "`cell name`" to "`view name`" and enter in "`abstract`" in the text box on the same line
- Click "`Apply`" (this will select everything)
- Click "`Select All`"
- Set the "`Replace`" option at the bottom of the Search window to replace the view name and then enter "`layout`" in the text box next to it
- Click "`Replace All`"
- Close the Search window

You have successfully generated the layout view. Now save the design as follows:

- `Design --> Save As` and then enter in "`layout`" for the view name
- Close the layout editing window. DO NOT save the changes to the abstract view
- Go to `File-->Open` in the main ICFB window and open your cell again, but in the layout view

Now that the design has been successfully imported into icfb, you are now ready to run DRC and LVS on it. For that purpose, you need to load the interface between calibre and icfb into icfb so that you can view the errors generated by calibre in icfb and can fix them.

- Load the icfb/calibre interface by entering the following in the CIW window:

```
load "CALIBRE/calibre.skl"
```

- Calibre operates on the gds2 format of the file for DRC/LVS.
- `File --> Export --> Stream`
- `library name: MY_LIB_3`
- `top cell name: mult`
- `view name: layout`
- `output file: mult.calibre.gds`
- Click "`User-Defined Data`" : (This opens a new window)

- `Layer Map Table: opus.map`
- Click “OK” to close the User-Defined Data window
- The `error message file` is PIPO.LOG.
- Click “OK” to close the Stream Out window
- A window should then pop up after a little while saying that the stream out was completed successfully. There should be no errors and around 4 warnings. Click “OK” - you may ignore the warnings.
- Run RVE from ICFB: RVE is the Calibre interface. Go to `Tools-->Layout` in the layout editing window and you should see a “`Calibre`” menu (the right-most one).
- `Calibre --> Start RVE`

3.1 DRC

- Run `calibre -gui &` at the shell
- Click on DRC
- Click on “`New Runset`”
- Under “`Calibre-DRC Rules File`”, click the “…” button and select the generic018.drc you copied earlier
- Click on “`Inputs`”
- Click on “`Flat`”
- Below, under “`Layout`”, select the mult.calibre.gds file under “`Files`:”. The path should turn green
- Under “`Primary Cell`” enter in the cell’s name (mult).
- Click “`Run DRC`”
- Click “`Start RVE`”
- Double click on any errors you get to zoom to their location in the layout editing window. Fix these errors (most involve drawing metal drawing layers over metal pin layers)
- After fixing the errors, re-export the GDS and re-run DRC.

3.2 LVS

- Generate schematic from APR verilog output using the following command in shell prompt (all on one line):
  ```
  v2lvs -v mult.apr.v -o mult.cdl -s
  /usr/caen/generic/artisan/tsmc18/aci/sc/lvs_netlist/tsmc18.cdl -s0 Vss
  -s1 Vdd
  ```

- You may see some warnings about some modules not being declared. You may ignore these.

- Click on `LVS` on the main Calibre window

- Start a new runset

- Select the generic018.lvs as your rules file

- Click "`Inputs`"

- Click "`Flat`"

- Click "`Layout vs Netlist`"

- Select the gds file as the layout file

- Enter in the name of the primary cell

- Click "`Netlist`"

- Select the cdl file you created earlier as the netlist file

- Select "`SPICE`" as the Netlist Format

- Enter in the name of the primary cell

- Click "`Outputs`"

- Set mult.lvs.report as the report file

- Click `Setup-->LVS Options`

- Under "`Supply`" check the "`Abort LVS on power/ground net errors`" and the "`Ignore layout and source pins during comparison`" boxes

- `Power nets: VDD!`

- `Ground nets: VSS!`

- Under "`ERC`" un-check "`run ERC`"

- Click “Run LVS”

All the errors will be shown in transcript window. In case of no errors, you will see the famous smiley that we so cherished in 427 :-)

4 Deliverables

Include only the following files in your tar-ball:

- README.txt : Any problems encountered and their solution (if solved)
- mult.drc.report
- mult.lvs.report