



Indium Phosphide and Related Materials (IPRM'98)

POWER-HANDLING CAPABILITY OF W-BAND INGAAS PIN DIODE SWITCHES

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I. Introduction

One of the most active research areas in the field of radar applications is the development of collision-avoidance systems (CAS) for automotive industry. The first prototypes of HEMT-based CAS chipsets operating at 77GHz have been recently demonstrated [1]. Such chipsets will greatly benefit from the addition of a monolithic transceiver switch, which would allow using a single antenna for both transmission and reception, and thus greatly reduce the cost of the assembly. PIN switching diodes offer unique advantages over HEMTs such as low ON-state resistance and small OFF-state capacitance combined with high power-handling capability [2,3]. Monolithic switches utilizing InGaAs/InP PIN diodes with excellent characteristics have been reported by the authors at W-band frequencies [4]. InP-based switching PINs offer several important advantages over GaAs-based technology, namely: substrate compatibility with high-performance InP-based HEMTs, low DC power consumption, and low ON-state resistance due to high electron mobility and small bandgap of InGaAs. However, the smaller bandgap of InGaAs also manifests itself in earlier onset of self-biasing effects and a smaller breakdown voltage, which affects their power handling. In this work the power-handling capability of InGaAs PIN diodes is reported and compared to that of GaAs PIN diodes. The trade-off between power handling, high frequency performance, and bias conditions is considered. W-band InGaAs PIN diode monolithic switches were fabricated using coplanar-waveguide technology, and their large-signal characteristics measured using a W-band load-pull characterization system are reported for the first time.

II. W-band InGaAs PIN Switches Fabrication

InGaAs PIN layers were grown with our in-house MOCVD system on semi-insulating InP substrates. The investigated structures had the following layers starting from the substrate: 1 μ m-thick n^+ ($1.5 \times 10^{19} \text{cm}^{-3}$), 1 μ m i (NID $5 \times 10^{15} \text{cm}^{-3}$), and 0.2 μ m p^+ ($1.5 \times 10^{19} \text{cm}^{-3}$). The diodes were fabricated on 5 μ m-diameter mesas using wet etching with $\text{HNO}_3:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:1:8) solution. Anodes

were made using Pt/Ti/Pt/Au, while Ti/Pt/Au was used for cathode metalization. Identical GaAs-based designs were fabricated for comparison using Pt/Ti/Au and Ge/Au/Ni/Ti/Au correspondingly. All contacts were annealed in Ar at 375 $^\circ$ C for 7sec. InGaAs PIN diodes demonstrated turn-on voltage $V_{\text{ON}}=+0.4\text{V}$ and reverse breakdown $V_{\text{BD}}=-23.5\text{V}$ (defined at 10 μ A current), while GaAs PINs showed $V_{\text{ON}}=+0.9\text{V}$ and $V_{\text{BD}}=-33\text{V}$.

W-band monolithic integrated single-pole single-throw switches were fabricated using coplanar-waveguide technology. The switches employed two shunt-connected PIN diodes spaced by $\lambda/4$ for improved performance. The layout of the SPST switch is shown in Figure 1. The circuit dimensions were 0.4mm \times 1.6mm. Low-parasitic Au-plated airbridge technology was used to connect diodes with the transmission line. Airbridges were also used to connect the two ground planes of coplanar waveguide in order to suppress generation of parasitic wave-propagation modes.

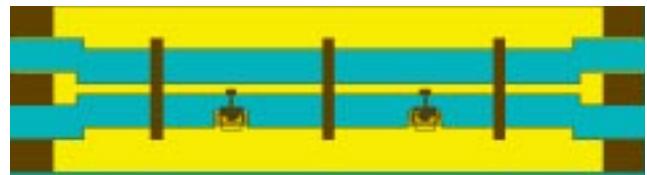


Figure 1. Layout of W-band monolithic integrated InGaAs PIN-diode single-pole single-throw switch

III. Small-Signal Performance

When a negative or zero bias is applied to the anode, the i -layer is depleted of carriers. Only a small charge-displacement current can flow through a small depletion capacitance. The PIN diode is in the high-impedance OFF-state. The signal injected into input port is transmitted to the output port with only a small insertion loss due to the leakage through the diodes.

S-parameters of the fabricated InGaAs PIN diode switches were measured on-wafer at W-band frequencies. The insertion loss (S_{21}) and return loss (S_{11}) of the switch in the OFF-state with bias $V_{\text{D}}=-3\text{V}$ are shown in Figure 2.

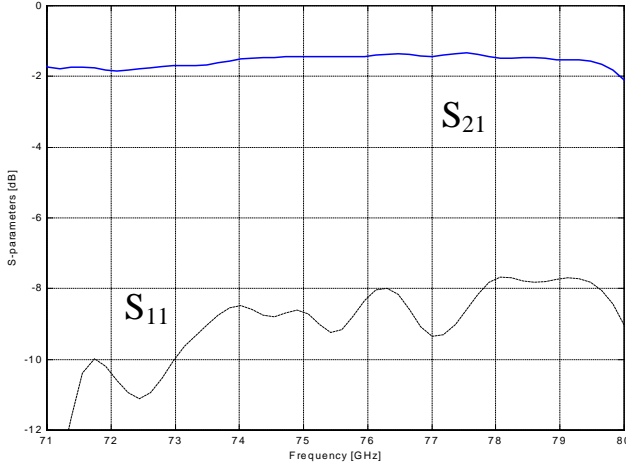


Figure 2. S-parameters of InGaAs PIN SPST switch in the OFF-state.

A low insertion-loss value of 1.4dB was demonstrated at 77GHz. The insertion loss was less than 2dB for frequencies between 71 and 80GHz, while the corresponding return loss was around 8dB.

Using the assumption that losses are due to the two PIN diodes only, the insertion loss (IL) of the SPST switch can be calculated according to equation (1):

$$IL = 20 \log_{10} ((\pi f C_{TOT} Z_0)^2 + 1) \quad (1)$$

where $Z_0=65\Omega$ is the characteristic impedance of the circuit and C_{TOT} is the total capacitance of the OFF-state diode consisting of the i -layer depletion capacitance C_{OFF} and the parasitic pad capacitance $C_{PAR} \sim 5fF$. Equation (1) was used to estimate the depletion capacitance under the assumption of perfect matching to 50Ω and a value of $C_{OFF}=18fF$ was found based on the insertion loss at 77GHz.

When a positive bias greater than the turn-on voltage V_{ON} is applied to the anode, the i -layer is filled with carriers. The larger the bias, the more carriers are added to the i -layer (conductivity modulation phenomenon [5]) and therefore the voltage drop across the i -layer remains constant. The PIN diode under such conditions is in the low-impedance ON-state. The ON-state impedance corresponds to a small access resistance (R_D) due to the n^+ and p^+ layers and an inductance (L_{AB}) resulting from the interconnecting airbridge. A large current swing is possible with only a small change of potential drop across the diode. The signal injected into the input port is shunted through the ON-state diodes and reflected back. Only a small portion of the input signal is transmitted to the output port in this case.

The isolation (S_{21}) and reflection loss (S_{11}) measured in the ON-state with bias $V_D=+0.6V$, $I_D=+0.9mA$ are shown in Figure 3. At 77GHz the isolation was 17.2dB and larger than 13dB for all frequencies between 71 and 80GHz.

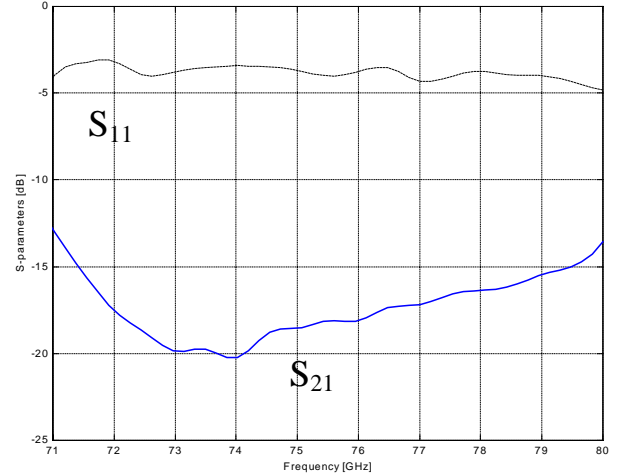


Figure 3. S-parameters of InGaAs PIN SPST switch in the ON-state.

Under the assumption of perfect matching, the isolation (IS) of the switch can be calculated using equation (2):

$$IS = 20 \log_{10} (Z_0 / (2(R_D^2 + (2\pi f L_{AB})^2) + 1)) \quad (2)$$

where R_D is the effective small-signal resistance of the diode, and $L_{AB} \sim 25pH$ is the inductance of the airbridge. Under the above assumptions, a value of 10Ω can be estimated for R_D from equation (2).

IV. Power Saturation Measurements

The power-handling capability of PIN switches was evaluated to complete their characterization for CAS applications. An automated W-band on-wafer load-pull measurement system was developed for this purpose at University of Michigan using electromechanical tuners made by Focus Microwaves Inc [6]. The system consisted of a W-band source, an input coupler, a W-band test fixture with probes, a computer-controlled W-band load tuner, and power sensors. Input power, output power, and biasing currents were measured and recorded at the device level as the function of input power and load impedance.

The InGaAs PIN diode SPST switch was characterized at 77GHz with load impedance Z_L set to 50Ω and demonstrated insertion loss of 2dB ($V_{OFF}=-3V$) and isolation of 18dB ($V_{ON}=0.6V$, $I_{ON}=+0.9mA$). Measurements with the large-signal setup operated under small-signal conditions showed good agreement with the characterization results presented in Section III.

The maximum power available from the source at 77GHz was $-3dBm$ and it was not sufficient to drive InGaAs PIN diodes into self-biasing conditions. A high-power source was, however, available at 102GHz and was used to study power-handling capabilities of W-band InGaAs PIN switches. Self-biasing (SB) effects were investigated by monitoring the insertion loss and current

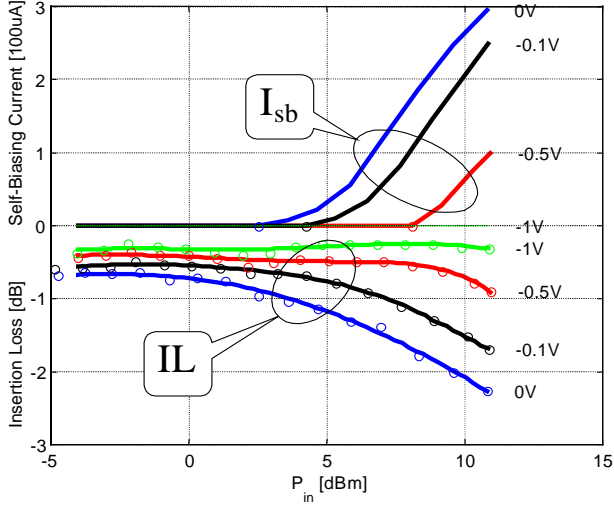


Figure 4. Insertion loss (IL) and self-biasing current (I_{SB}) of InGaAs PIN switch measured at 102GHz as a function of input power for different OFF-state bias conditions.

through the devices as the input power level was varied from $P_{IN}=-4$ to $+12$ dBm and the OFF-state bias V_D was varied between 0 and -5 V. The results are shown in Figure 4. As the input power was increased, the diodes were self-biased into ON-state, which manifested itself in an increase of current through the devices and degradation of insertion loss. The input power level at which the self-biasing current reached $10\mu A$ and insertion loss started to degrade was defined as the power-handling capability P_{SB} .

For zero bias P_{SB} was $+3$ dBm and the insertion loss degraded from 0.6 dB to 2.4 dB. By biasing the diodes in the reverse direction, one can compensate the changes induced by the presence of large-signal power levels. P_{SB} could be increased in this way from $+3$ to $+7$ dBm by changing the bias from zero to $V_D=-0.5$ V. No self-biasing effects were observed for $V_D=-1$ V for up to the maximum available source power of $+12$ dBm. At the same time, the small-signal insertion loss improved from 0.6 to 0.3 dB due to the reduction of the OFF-state capacitance.

The power handling capability of the diodes can be estimated theoretically by considering that self-biasing effects start when the input power level P_{SB} results in voltage amplitude ($V_{ON}+V_{OFF}$) across the diode terminals. The following relation can express this condition:

$$P_{SB} = (V_{OFF}+V_{ON})^2/Z_0 \quad (3)$$

where V_{ON} is the turn-on voltage, V_{OFF} is the OFF-state bias, and Z_0 is the characteristic impedance of the transmission line. The experimental results of the self-biasing study are summarized in Figure 5 together with the theoretical values calculated using equation (1) and (3). The experimentally obtained insertion loss and power-handling capability showed an excellent agreement with the theoretical calculations.

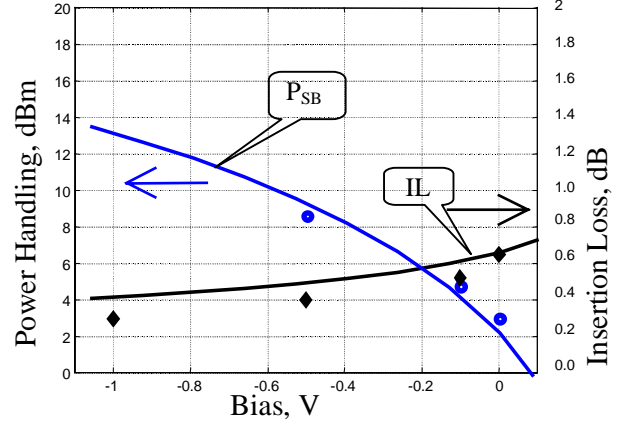


Figure 5. Theoretical and measured insertion loss (IL) and power handling (P_{SB}) of InGaAs PIN switch at 102GHz.

The equations were also used to investigate an optimal design for high-power low-loss InGaAs PIN switching diodes. The results demonstrate that the minimum insertion loss does not continue to improve when i -layer thickness is increased beyond $1\mu m$ due to the limitations imposed by the avalanche breakdown and unintentional doping in InGaAs ($n_i \sim 5 \times 10^{15} \text{cm}^{-3}$). However, power handling is improving for thicker i -layers. The study indicates that an optimal InGaAs PIN diode design for high-power and low-loss should have $1.25\mu m$ -thick i -layer.

To complete the power characterization, measurements were performed at 8 GHz where larger-power signal sources were available. Due to the difference in the energy bandgap between GaAs and InGaAs, the zero biased InGaAs switch started to self-bias into a low-impedance state at $P_{SB}+3$ dBm while for the GaAs switch the same happens at larger $P_{IN,SB}+13$ dBm. However, this difference was compensated by applying negative bias to the InGaAs switch, which then demonstrated $P_{SB}+15$ dBm at $V_d=-1$ V and no self-biasing effects up to the maximum available source power $P_{in}+19$ dBm at $V_d=-2$ V.

V. Load-Pull Measurements

The automated W-band on-wafer large-signal characterization system was also used to evaluate constant loss contours for W-band InGaAs PIN diode switches at the standard CAS frequency of 77 GHz. These are shown in Figure 6 and Figure 7 for InGaAs diodes in the OFF- and ON-state respectively. The contours can be used to evaluate the switch termination impedance values that result to the same transmission loss characteristics.

When the PIN diodes were in the high-impedance OFF-state ($V_{OFF}=-3$ V) the optimum load impedance for minimum loss ($Z_{L1}=40-j8.4\Omega$) was close to the design goal of 50Ω and the corresponding minimum insertion loss was 1 dB as shown in Figure 6. Measurement of the insertion loss at the optimal ($Z_L=Z_{L1}$) load conditions allows to

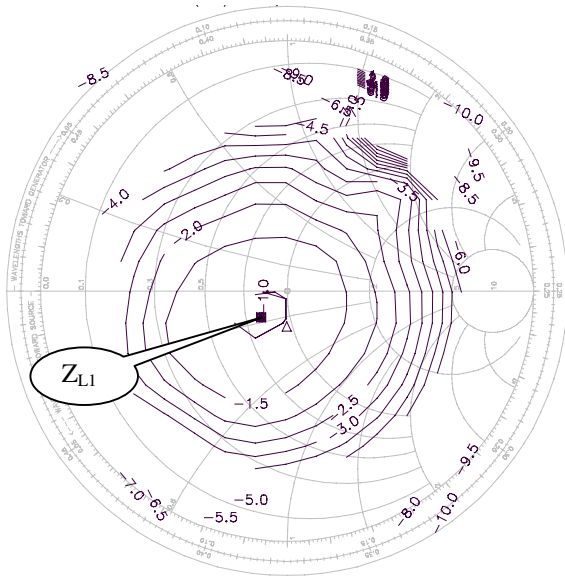


Figure 6. Constant loss contours for InGaAs PIN diode switch in the OFF-state ($V_{OFF}=-3V$)

obtain a more precise value for the depletion capacitance C_D . This is due to the fact that the exact (Z_{L1}) rather than approximate (50Ω) impedance value is used; see Section III for the approximate evaluation. The corrected value of C_D based on the above consideration is 16fF.

When the diodes are biased into the low-impedance ON-state ($V_{ON}=0.65V$ $I_{ON}=9mA$), the impedance point corresponding to maximum-transmission is close to the edge of the Smith chart as shown in Figure 7. The values of impedance corresponding to a minimum insertion loss (OFF-state) and minimum isolation (ON-state) are therefore different. As shown in Figure 7, the isolation is 18dB using 50Ω termination, while a minimum isolation of 15.4dB is observed at $Z_{L2}=14.7-j15.3\Omega$. The 18dB of isolation at 50Ω consist of two parts, 15.4dB from the diodes and 2.6dB due to the mismatch with Z_{L2} . The knowledge of the ON-state matching termination impedance (Z_{L2}) allows more accurate determination of the effective resistance R_D than by the approach described in Section III using impedance of 50Ω . The corrected value of R_D is 17Ω .

VI. Conclusions

Overall, we report for the first time the large-signal characteristics of InGaAs PIN diode switches measured at the CAS frequency of 77GHz and at 102GHz using an automated on-wafer load-pull measurement system and demonstrated their high-power-handling potential. It was found that InGaAs PIN switches did not demonstrate any degradation of P_{OUT} (P_{IN}) characteristics for input power levels up to maximum available power of +12dBm at

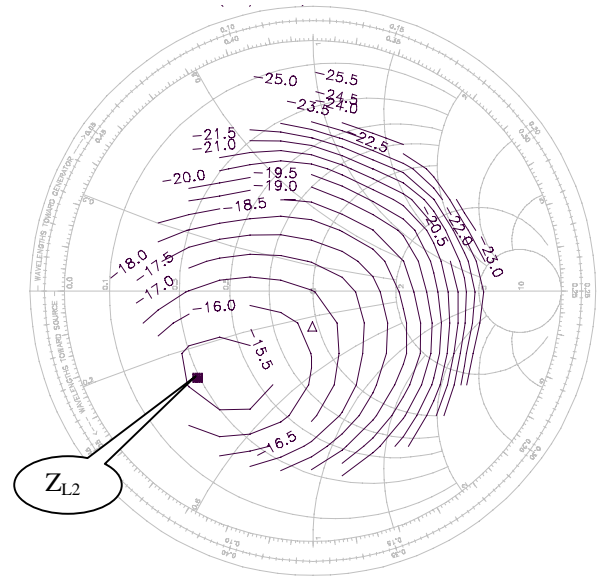


Figure 7. Constant loss contours for InGaAs PIN diode switch in the ON-state ($V_{ON}=0.65V$, $I_{ON}=9mA$)

102GHz and for as much as +20dBm at 8GHz when biased in the OFF-state ($V_D=-1V$ and $V_D=-2V$ correspondingly).

Acknowledgements

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