Abstract

SRAM has always been the most power consuming module in the modern day application for Wireless Sensor Node (WSN). This paper describes the design for low power 8T Static Random Access Memories (SRAM) which is operated in sub V\textsubscript{t} (400mV). This is used with 16 bit RISC general processor in 130nm IBM CMOS process which can be used for wireless sensor node applications. The SRAM cell implemented has Static Noise Margin (SNM) of 125mV and write margin of 155mV. The final SRAM has write time stability of 10 ns (Fig. 1) and read time stability of 12 ns (Fig. 2).

Introduction

Memories have always been an area of great interest and research. With advances in technology and requirements of the market, there has been a significant research in low power SRAM especially when they are used in some WSN application, or systems which are battery powered. Thus, it requires memories that are efficient with optimal performance at the same time.

Approach

This project is targeting the sub-threshold application where the read and write stability are of supreme concern. Hence, we have implemented our SRAM in the 8T architecture. This makes the circuit more robust without losing much on area of the cell compared to 6T SRAM cell. The major problem in the 8T SRAM is that it has one bit read line so for most architectures of sense amplifier cannot be implemented for reading. Another problem is that bit values swing in sub-threshold region, so to feed them to the processor which is running at 1.2V requires level converter. To solve the problem, all of these have been integrated within one analog sense amplifier which senses voltage difference of 10mV from triggering voltage and amplifies the signal to 1.2V level.

• When writing into SRAM, we need to maintain a relatively higher resistivity for the PFETs. Thus, the access transistors are made NFETs to ensure the write stability.
• All the FETs in the 8T array are kept at minimum and are seen to function reliably at 0.4V access and supply voltages.
• The read access transistor MN6 is very crucial for deciding the read access time. So MN6 is sized 2X in length to help in reducing its threshold voltage and improve the read time.

Conclusion

8T SRAM bit cell shows impressive performance and has been characterized extensively by running vital tests on the cell like SNM, write margin, write stability and read stability. Lot of innovation has been put into the read phase of the cell, for improving read time stability. The final layout of whole SRAM has been successfully laid out and it is highly dense. Furthermore, SRAM displays its correct functionality and has reasonably good write and read time stability.

For future, we are targeting to work on sleep mode in the SRAM when the SRAM is not being used.

Simulation Result

Figure 1: The simulation above shows write time stability of 10ns. Values are written into SRAM at 0 ns, 10 ns, and 20 ns. The Monte Carlo results suggest that values are written reliably into SRAM.

Figure 2: The simulation above shows read time stability of 12ns. Values are read from SRAM at 30.5 ns. The Monte Carlo results suggest that values are read reliably from SRAM.