EECS 373

Introduction to Embedded System Design

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Lecture 12: Power

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Review

- Memory
- PCB design

Outline

- **Power and energy**
- Power integrity

Definitions

- Why? Power, temperature, energy, performance, and reliability important and deeply connected.
- Understand
  - why system failing and
  - why it consumes power.
- Temperature: Average kinetic energy of particle.
- Heat: Transfer of this energy.
  - Heat flows from regions of higher temperature to regions of lower temperature.
- Particles move.
- What happens to a moving particle in a lattice?
- Power: Rate of energy transfer (watts).

Why do wires get hot?

- Scattering of electrons due to destructive interference with waves in the lattice.
- What are these waves?
- What happens to the energy of these electrons?
- What happens when wires start very, very cool?
- What is electrical resistance?
- What is thermal resistance?
- Why do metals often have low thermal resistances?

Why do transistors get hot?

- Scattering of electrons due to destructive interference with waves in the lattice.
- Where do these waves come from?
- Where do the electrons come from?
  - Intrinsic carriers.
  - Dopants.
- What happens as the semiconductor heats up?
  - Carrier concentration increases.
  - Carrier mobility decreases.
  - Threshold voltage decreases.

Power consumption trends

- Initial optimization at transistor level.
- Further research-driven gains at this level difficult.
- Research moved to higher levels, e.g., RTL.
- Trade area for performance and performance for power.
- Clock frequency gains linear.
- Voltage scaling V_{DD}^2 – very important.

DON'T PANIC

Power consumption

- $P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$
- $P_{SWITCH} = C \cdot V_{DD}{}^{2} \cdot f \cdot A$
- $P_{SHORT} = b/12 \cdot (V_{DD} - 2 \cdot VT)^{3} \cdot f \cdot A \cdot t$
- $P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$
- C : total switched capacitance
- V_{DD} : high voltage
- f : switching frequency
- A : switching activity
- b : MOS transistor gain
- V_T : threshold voltage
- t : rise/fall time of inputs
- † PSHORT usually ≤ 10% of PSWITCH
- Smaller as $V_{DD} \rightarrow V_T$

DVFS

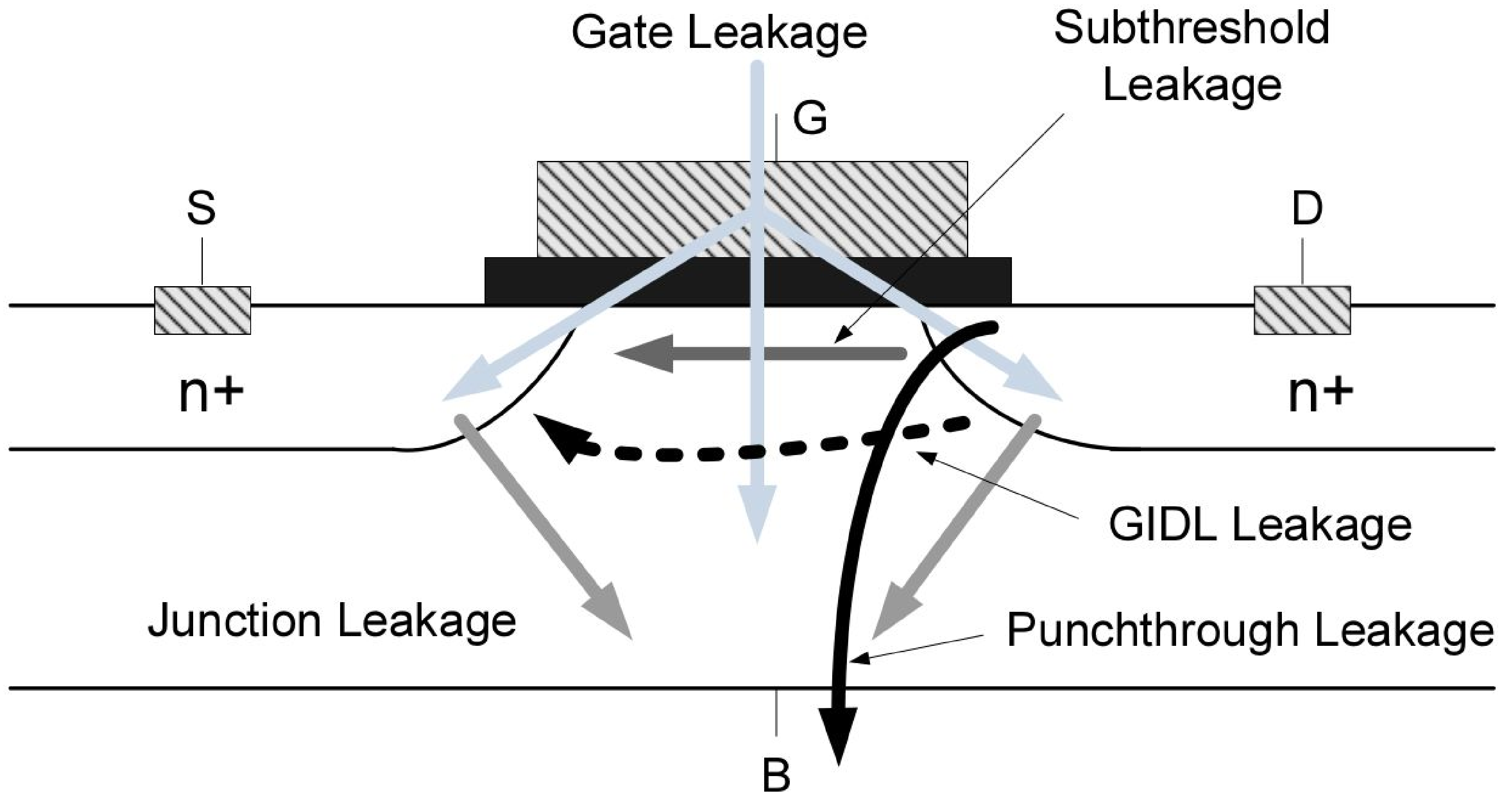
- Power drops superlinearly in V.
- Performance drops linearly in V.
- Double transistor count.
- Drop V.
- Drop f.
- Net result.
  - Reduced power.
  - Reduced energy, even though t increases.
- Fails when Vdd → Vth.

Typical control policies

- If utilization < ~80%, drop V, f.
- If utilization > ~80%, increase V, f.
- Latency: >100ms in some cases.
- Based on flawed assumption for interactive systems.

- If device has been used within X minutes, keep on.
- Otherwise, put in lower power management state.

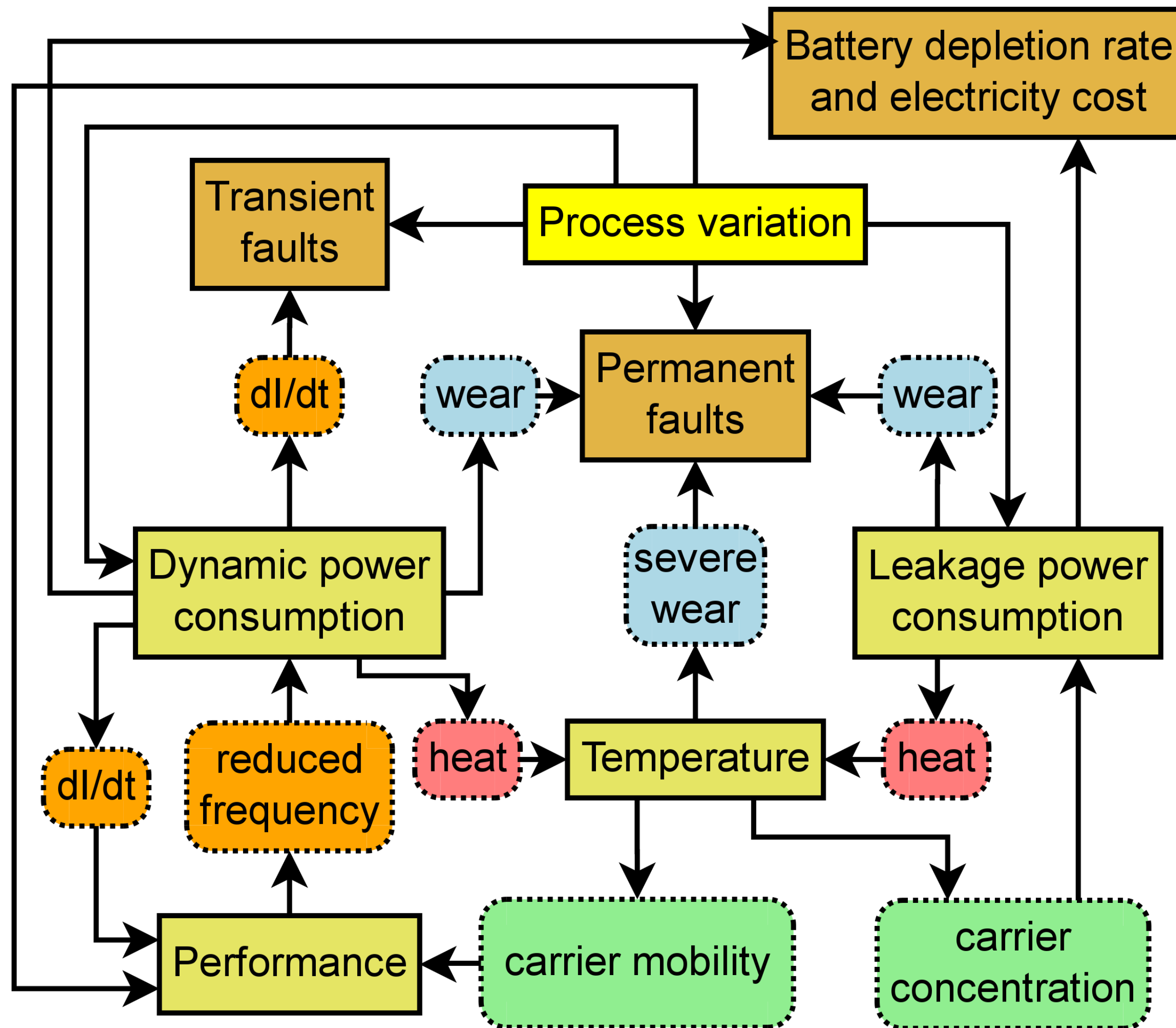
Leakage paths



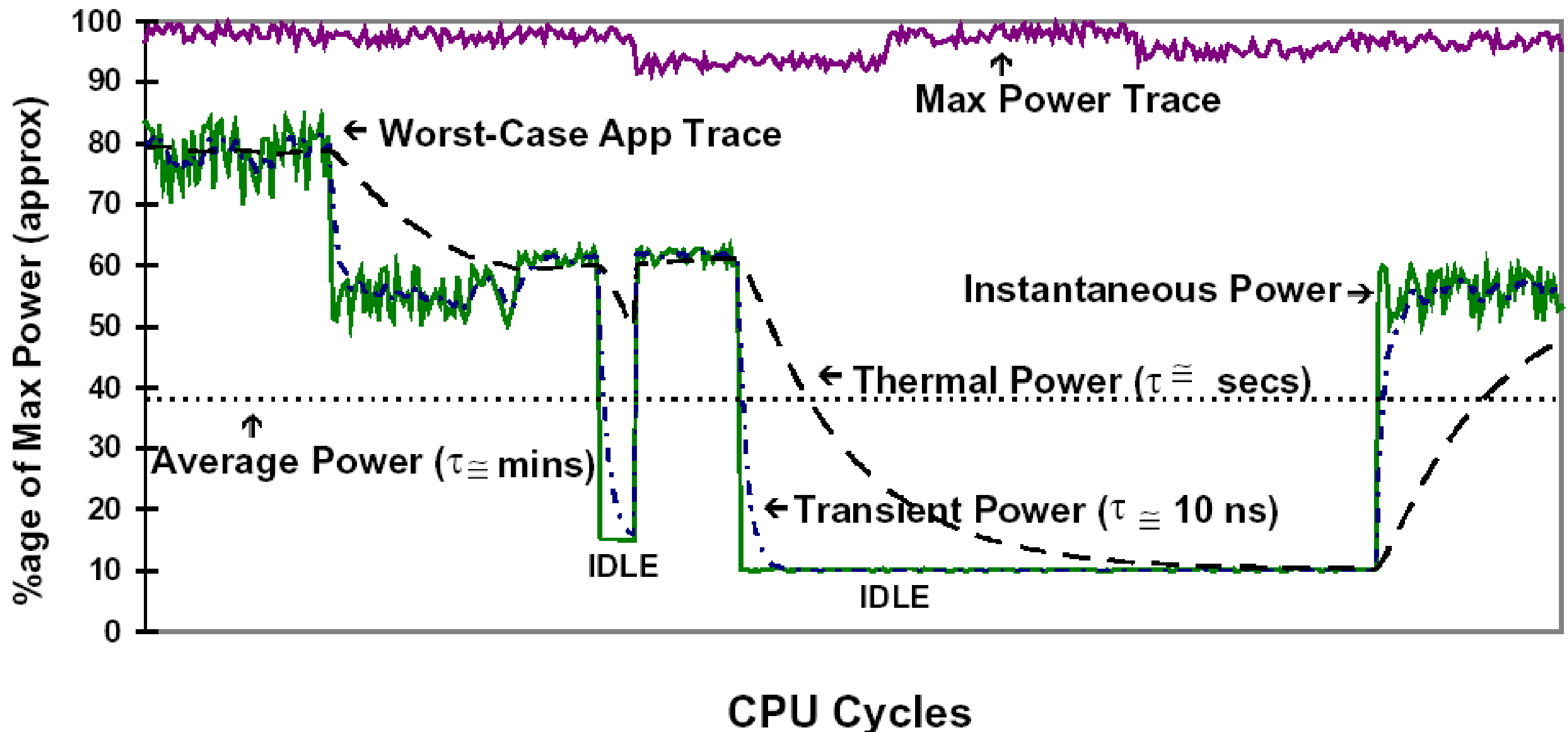
Subthreshold leakage

- $I_{subthreshold} = A_S \, W/L \, v_T^2 \, (1 - \exp(-V_{DS}/v_T)) \cdot$
  $\exp((V_{GS} - V_{th}) / n \, v_T)$
- where A_s is a technology-dependent constant,
- V_{th} is the threshold voltage,
- L and W are the device effective channel length and width,
- V_{GS} is the gate-to-source voltage,
- n is the subthreshold swing coefficient for the transistor,
- V_{DS} is the drain-to-source voltage, and
- v_T is the thermal voltage.

Power, temperature, performance, and reliability



Power time series



- **Max Power:** Artificial code generating max CPU activity
- **Worst-case App Trace:** *Practical* applications worst-case
- **Thermal Power:** Running average of worst-case app power
- over a time period corresponding to thermal time constant
- **Average Power:** Long-term average of typical apps (minutes)
- **Transient Power:** Variability in power consumption for supply net

Energy

- Power integrated over time.
- Average power multipled by time.
- J (mA-h for batteries, multiplies by V).rin

State-based power modeling

- For each component.
  - For each state.
    - Sum time spent in state × average power for state.
- Time-dependent state transitions are central.
- Big eaters
  - Displays.
    - Fluorescent tubes.
    - OLEDs.
  - Wireless interfaces.
    - Cellular.
    - WiFi.
    - Bluetooth.
  - CPU.

State-based power modeling

	Component		
	CPU	Wireless	Motor
Power state	DFVS max 12W / 1%	Transmit 12W / 0.5%	On 20W / 2%
	DVFS min 1W / 4%	Receive 10W / 10%	Off 0 W / 98%
	Sleep 1uW / 95%	Standby 1W / 39.5%	
	Off 0W / 0%	Off 0W / 50%	

$A_{ps,\ dev}$ is the proportion of time *dev* spends in *ps*.
$P_{ps,dev}$ is the power consumption of *dev* when in state *ps*.
$P_{tot} = \sum_{ps\ \epsilon\ power\ states} \sum_{dev\ \epsilon\ devices} P_{ps,\ dev} \times A_{ps,\ dev}$

This is extraordinarily useful, and of shocking simplicity.

Outline

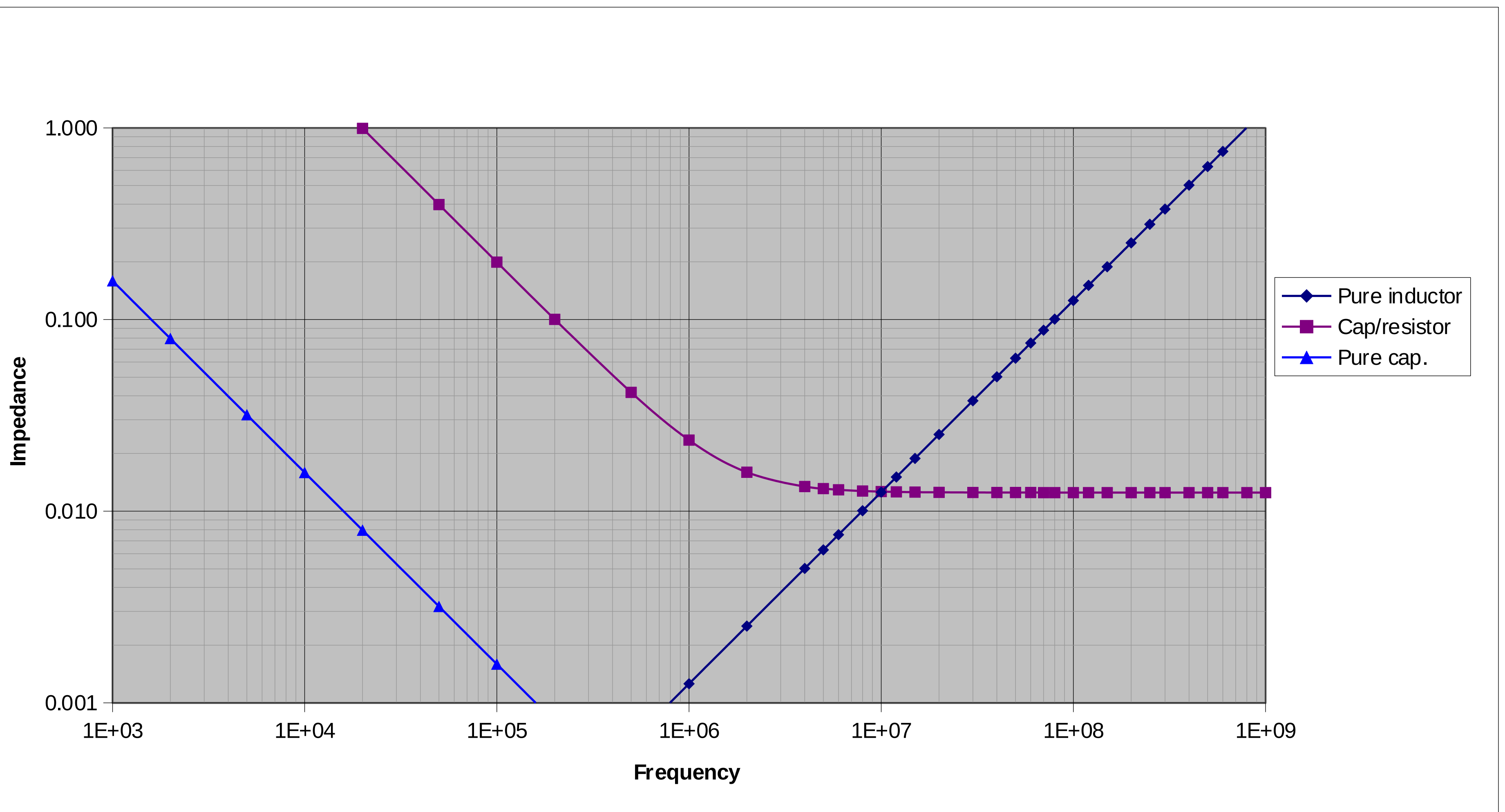
- Power and energy
- **Power integrity**

Power integrity

- Why? Get it wrong and board resets itself or worse for no apparent reason.

A look at impedance

(with capacitors, inductors and resistors vs. frequency)



Notice the log scales!

Power integrity related faults

- Even short “power droops” cause failure.
- Stable power = power Integrity.
- Does C fix?
  - No: parasitics.

Non-ideal devices

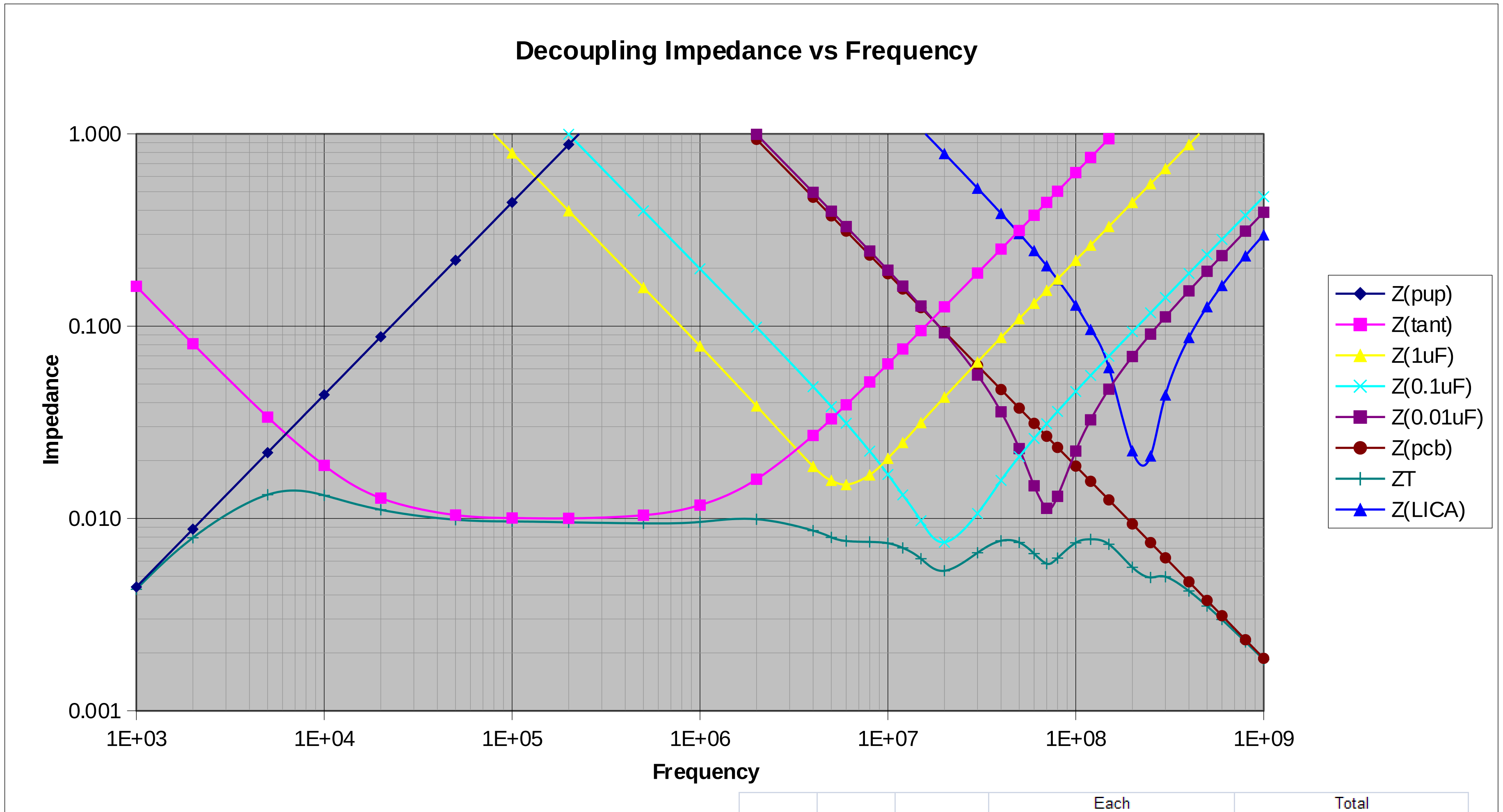
			Each			Total		
Device		Quantity	Cap	ESR	ESL	Ceff	ESR	ESL
DC/DC Converter		1		1.00E-04	7.00E-07		1.00E-04	7.00E-07
Tantalum Capacitors		3	3.30E-04	3.00E-02	3.00E-09	9.90E-04	1.00E-02	1.00E-09
0603 Ceramic Caps.		2	1.00E-06	3.00E-02	7.00E-10	2.00E-06	1.50E-02	3.50E-10
0603 Ceramic Caps.		8	1.00E-07	6.00E-02	6.00E-10	8.00E-07	7.50E-03	7.50E-11
0603 Ceramic Caps.		8	1.00E-08	9.00E-02	5.00E-10	8.00E-08	1.13E-02	6.25E-11
0603 Ceramic Caps.		10	1.00E-09	1.50E-01	5.00E-10	1.00E-08	1.50E-02	5.00E-11
PC Board		1	8.50E-08			8.50E-08		

- ESR is Effective Series Resistance
- ESL is Effective Series Inductance
- Ceff is the effective capacitance.
  - How does quantity effect these values?
- Obviously impendence will be varying by frequency.

ESR/ESL contributors

- Bad solder jobs make ESR/ESL worse.
- Bad solder jobs make everything worse.
- **Everything.**
- Packaging has an impact.
- SMT eliminate wire parasitics.
- Pads can have an impact

Given the previous table



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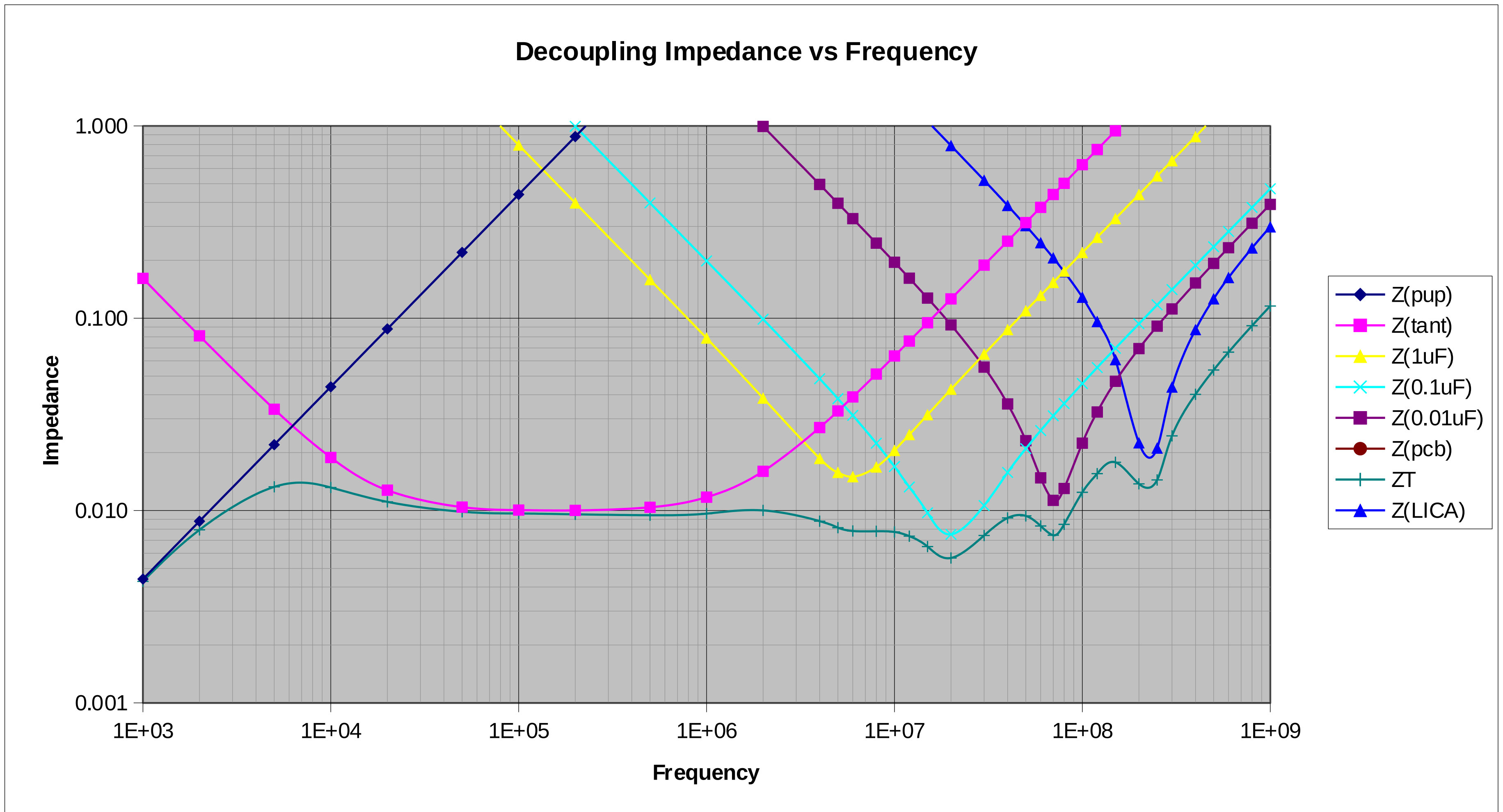
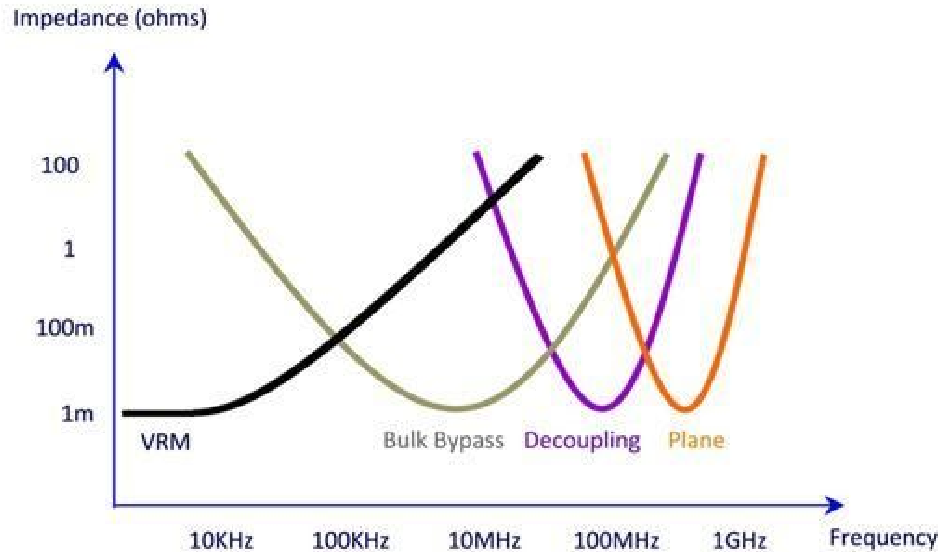
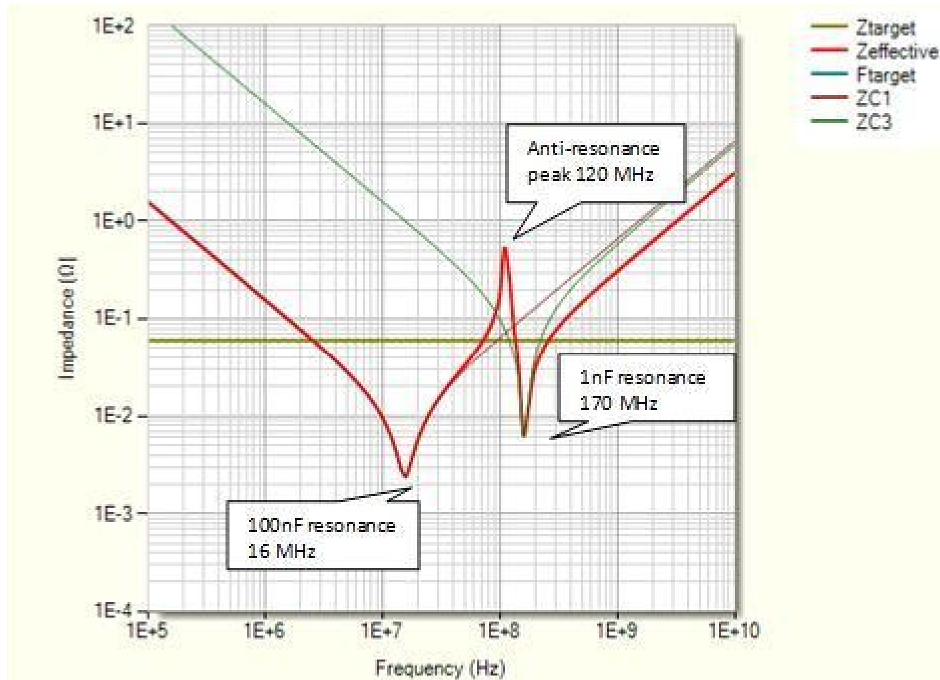
Removing the PCB



Staged capacitors

- Voltage regulator module
- Bulk bypass (tantalum) and decoupling capacitors (ceramic).
  - Instantaneous current.
  - Different frequencies.
- However sets of different capacitors cause problems!





Power integrity summary

- Use range of C values.
- Model frequency response.
  - Consider parasitics.
- SPICE works.

Other sources of information

- http://alternatezone.com/electronics/files/PCBDesignTutorialRevA.pdf
  - **Very** nice tutorial/overview
  - Seems to have strong viewpoint
- http://www.goldengategraphics.com/pcgloss.htm
  - Some definitions taken verbatim.

Done.